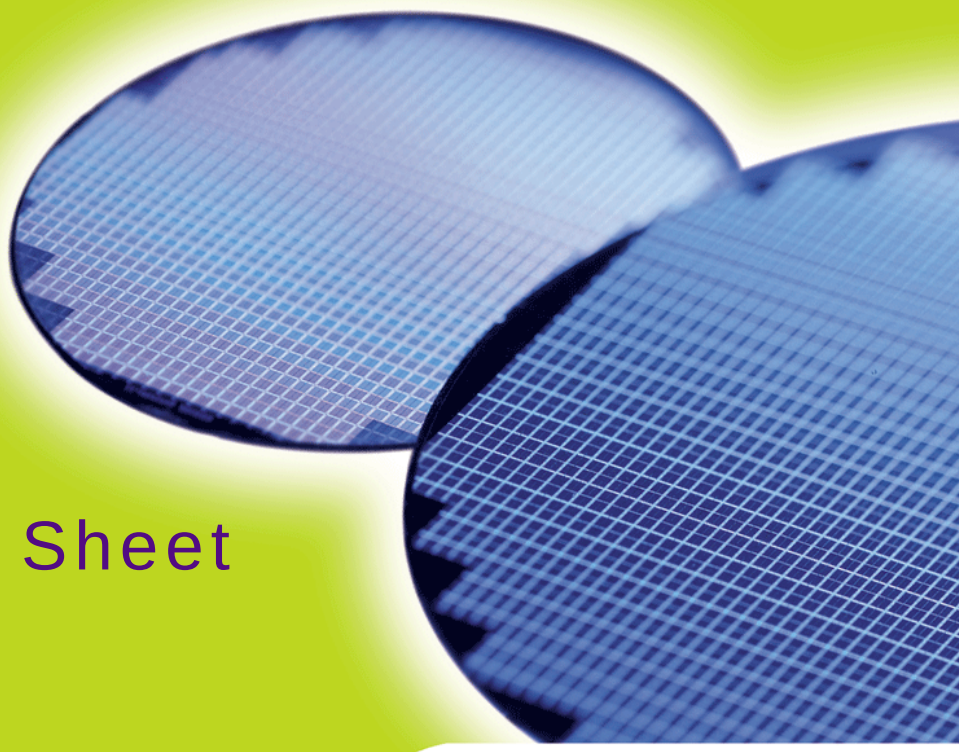
May 2008

HYS64D32301EU–[5/6]–D
HYS[64/72]D64300EU–[5/6]–D
HYS[64/72]D128320EU–[5/6]–D

184-Pin Unbuffered Double-Data-Rate Memory Modules
UDIMM SDRAM
DDR SDRAM



Advance

Internet Data Sheet

Rev. 0.60

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HYS64D32301EU–[5/6]–D, HYS[64/72]D64300EU–[5/6]–D **Revision History: 2008-05, Rev. 0.60**	
Page	**Subjects (major changes since last revision)**
All	Added Product type HYS64D[64/128]3x0-6-D and HYS64D32301EU-[5/6]-D and adapted to internet edition.
Previous Revision: 2008-04, Rev. 0.53	
16, 17	Added IDD values.
Previous Revision: 2008-02, Rev. 0.52	
21 - 24	SPD codes updated.
Previous Revision: 2007-10, Rev. 0.51	
All	Added products HYS72D[64/128]3x0EU-[5/6]-D
Previous Revision: 2007-09, Rev. 0.50	
All	New Document.

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1 Overview

This chapter contains features and the description.

1.1 Features

- 184-Pin Unbuffered Double-Data-Rate Memory Modules (ECC and non-parity) for PC and Workstation main memory applications
- One rank 64M x 64, 64M x 72, 32Mx64 and two ranks 128M × 64, 128M × 72 module organization
- Standard Double Data Rate Synchronous DRAMs (DDR SDRAM)
- Single +2.5V (±0.2V) power supply
- Built with 512-Mbit in P-TSOPII-66 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Standard reference layout
- Gold plated contacts
- DDR400 speed grade supported
- Lead-free

TABLE 1
Performance for –5 and –6

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333B	—
	Module		PC3200-3033	PC2700-2533	
Max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	166	MHz
	@CL2	f_{CK2}	133	133	MHz

1.2 Description

The Qimonda HYS64D[64/128]3x0EU-5-D are industry standard 184-Pin Unbuffered Double-Data-Rate Memory Modules (UDIMM) organized as 32Mx64 (256MB), 64M ×64 (512 MB), 64M ×72 (512 MB), 128M ×72 (1 GB) and 128M ×64 (1 GB) for non-parity and main memory applications. The memory array is designed with 512Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E^2PROM device using the 2-pin I2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

green Product

TABLE 2
Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL=3.0)			
HYS64D32301EU–5–D	PC3200U–30331–C2	one rank 256MB DIMM	512 Mbit (×16)
HYS64D64300EU–5–D	PC3200U–30331–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300EU–5–D	PC3200U–30331–A0	one rank 512 MB DIMM ECC	512 Mbit (×8)
HYS64D128320EU–5–D	PC3200U–30331–B0	two rank 1GB DIMM	512 Mbit (×8)
HYS72D128320EU–5–D	PC3200U–30331–B0	two rank 1GB DIMM ECC	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D32301EU–6–D	PC3200U–30331–C2	one rank 256MB DIMM	512 Mbit (×16)
HYS64D64300EU–6–D	PC2700U–25331–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300EU–6–D	PC2700U–25331–A0	one rank 512 MB DIMM ECC	512 Mbit (×8)
HYS64D128320EU–6–D	PC2700U–25331–B0	two rank 1GB DIMM	512 Mbit (×8)
HYS72D128320EU–6–D	PC2700U–25331–B0	two rank 1GB DIMM ECC	512 Mbit (×8)

Note: All product type numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D64300EU-5-D, indicating rev. D dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC3200"), the latencies and SPD code definition (for example "30331" means CAS latency of 3.0 clocks, RCD (Row-Column-Delay) latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 1), and the Raw Card used for this module.

TABLE 3
Address Format

Density	Organization	Memory Ranks	SDRAM Organization	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M ×64	1	512M ×16	4	13/2/10	8K	64 ms	7.8 ms
512 MB	64M ×64	1	512M ×8	8	13/2/11	8K	64 ms	7.8 ms
512 MB	64M ×72	1	512M ×8	8	13/2/11	8K	64 ms	7.8 ms
1 GB	128M ×64	2	512M ×8	16	13/2/11	8K	64 ms	7.8 ms
1 GB	128M ×72	2	512M ×8	16	13/2/11	8K	64 ms	7.8 ms

2 Configuration

2.1 Pin Configuration

The pin configuration of the Unbuffered DDR SDRAM DIMM is listed by function in **Table 4** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 5** and **Table 6** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 4
Pin Configuration of UDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
137	CK0	I	SSTL	**Clock Signals 2:0**
	NC	NC	–	*Note: For clock net loading see block diagram, CK0 is NC on 1R ×16*
16	CK1	I	SSTL	
76	CK2	I	SSTL	
138	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 2:0**
	NC	NC	–	*Note: For clock net loading see block diagram, CK0 is NC on 1R ×16*
17	$\overline{CK1}$	I	SSTL	
75	$\overline{CK2}$	I	SSTL	
21	CKE0	I	SSTL	**Clock Enable Rank 0**
111	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
Control Signals				
157	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
158	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
154	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
65	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
63	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
59	BA0	I	SSTL	**Bank Address Bus 2:0**
52	BA1	I	SSTL	

Pin#	Name	Pin Type	Buffer Type	Function
48	A0	I	SSTL	**Address Bus 11:0**
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	
32	A5	I	SSTL	
125	A6	I	SSTL	
29	A7	I	SSTL	
122	A8	I	SSTL	**Address Bus 11:0**
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	
118	A11	I	SSTL	
115	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
	NC	NC	–	*Note: 128 Mbit based module*
167	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	–	*Note: Module based on 512 Mbit or smaller dies*
Data Signals				
2	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	
106	DQ13	I/O	SSTL	
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	

Pin#	Name	Pin Type	Buffer Type	Function
114	DQ20	I/O	SSTL	**Data Bus 63:0**
117	DQ21	I/O	SSTL	
121	DQ22	I/O	SSTL	
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	
150	DQ38	I/O	SSTL	
151	DQ39	I/O	SSTL	
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	
166	DQ53	I/O	SSTL	
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	

Pin#	Name	Pin Type	Buffer Type	Function
174	DQ60	I/O	SSTL	**Data Bus 63:0**
175	DQ61	I/O	SSTL	
178	DQ62	I/O	SSTL	
179	DQ63	I/O	SSTL	
Check Bit				
44	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
45	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
49	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
51	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
134	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
135	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
142	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
144	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
5	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
14	DQS1	I/O	SSTL	
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	
78	DQS6	I/O	SSTL	
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	**Data Strobe 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*

Pin#	Name	Pin Type	Buffer Type	Function
97	DM0	I	SSTL	**Data Mask Bus 7:0**
107	DM1	I	SSTL	
119	DM2	I	SSTL	
129	DM3	I	SSTL	
149	DM4	I	SSTL	
159	DM5	I	SSTL	
169	DM6	I	SSTL	
177	DM7	I	SSTL	
140	DM8	I	SSTL	**Data Mask 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
EEPROM				
92	SCL	I	CMOS	**Serial Bus Clock**
91	SDA	I/O	OD	**Serial Bus Data**
181	SA0	I	CMOS	Slave Address Select Bus 2:0
182	SA1	I	CMOS	
183	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
184	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	PWRzp	–	**Power Supply**

Pin#	Name	Pin Type	Buffer Type	Function
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	GND	–	**Ground Plane**
Other Pins				
82	V_{DDID}	O	OD	V_{DD} Identification *Note: Pin in tristate, indicating V_{DD} and V_{DDQ} nets connected on PCB*
9, 10, 71, 90, 101, 102, 103, 113, 163, 173	NC	NC	–	**Not connected** Pins not connected on Qimonda UDIMMs

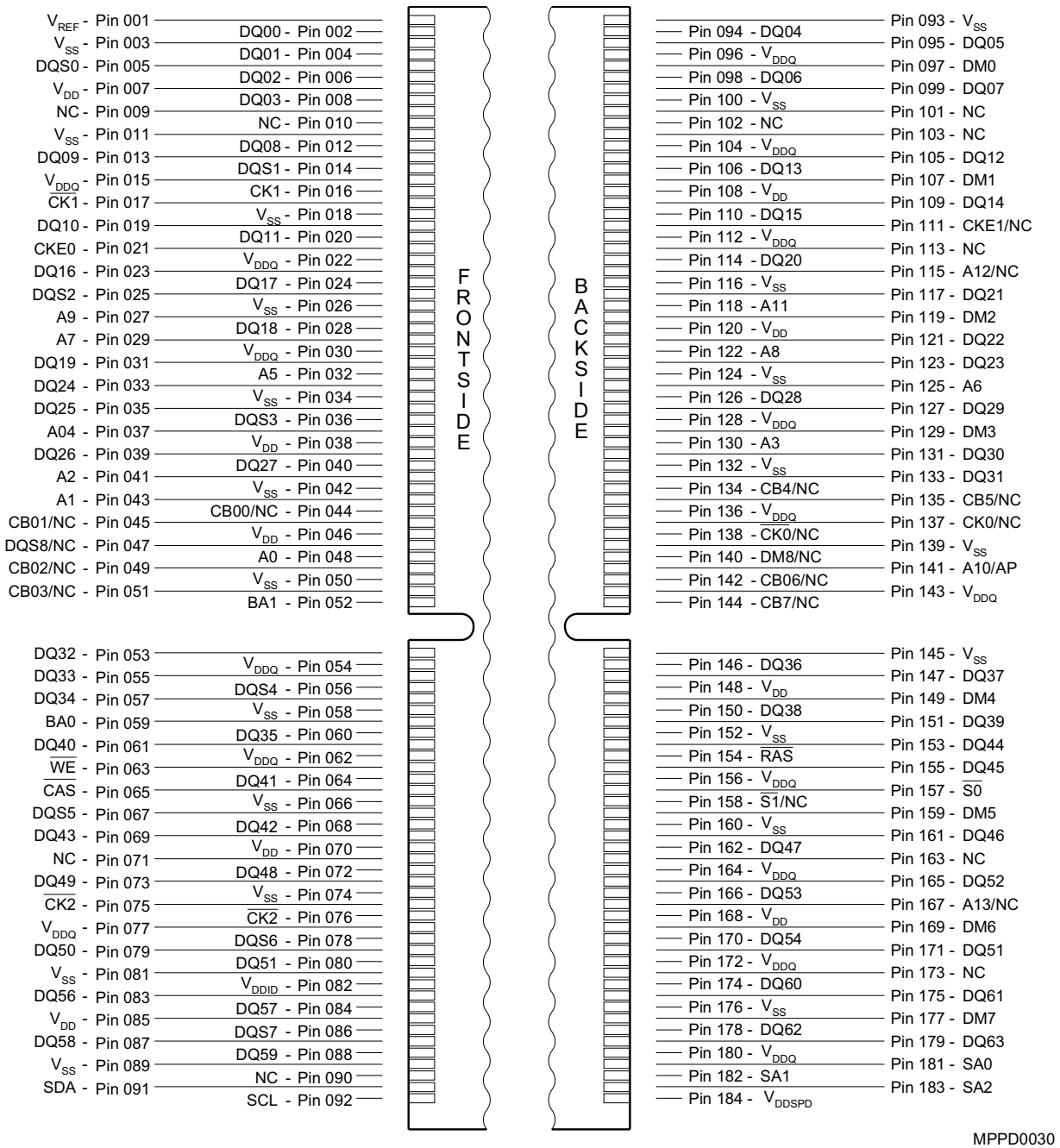
TABLE 5
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 6
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration 184-Pin, UDIMM



3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Operating Conditions

This chapter describes the operating conditions.

TABLE 7
Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	PD	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: ***Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.***

TABLE 8
Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	8)
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	8)
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	8)
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	8)6)
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	7)
Input Leakage Current	I_I	–2		2	µA	Any input 0 V ≤ V_{IN} ≤ V_{DD}; All other pins not under test = 0 V 8)9)
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V ≤ V_{OUT} ≤ V_{DDQ} 8)
Output High Current, Normal Strength Driver	I_{OH}	–16.2		—	mA	V_{OUT} = 1.95 V 8)
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V 8)

1) 0 °C ≤ T_A ≤ 70 °C
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% VREF (DC). VREF is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Inputs are not recognized as valid until V_{REF} stabilizes.
9) Values are shown per component

3.2 Current Conditions and Specification

This chapter describes the Conditions and Specification.

TABLE 9
I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

TABLE 10
I_{DD} Specification for HYS64D32301EU–[5/6]–D

Product Type	HYS64D32301EU–5–D		HYS64D32301EU–6–D		Unit	Note [1)2)]
Organization	256 MB		256 MB			
	×64		×64			
	1 Rank		1 Rank			
	–5		–6			
Symbol	Typ.	Max.	Typ.	Max.		
I_{DD0}	224	276	192	240	mA	3)
I_{DD1}	256	312	220	272	mA	3)4)
I_{DD2P}	4	18	4	18	mA	5)
I_{DD2F}	88	120	80	108	mA	5)
I_{DD2Q}	60	88	56	80	mA	5)
I_{DD3P}	32	56	32	56	mA	5)
I_{DD3N}	116	148	104	136	mA	5)
I_{DD4R}	292	352	252	308	mA	3)4)
I_{DD4W}	280	340	244	296	mA	3)
I_{DD5}	492	584	440	504	mA	5)
I_{DD6}	6	20	6	20	mA	5)
I_{DD7}	708	852	596	668	mA	3)4)

1) DRAM component currents only
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx}[component] + **n** × I_{DD2P}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

TABLE 11

I_{DD} Specification for HYS64D[64/128]3x0EU–[5/6]–D

Product Type	HYS64D64300EU–5–D		HYS64D64300EU–6–D		HYS64D128320EU–5–D		HYS64D128320EU–6–D		Unit	Note [1)2)]
Organization	512 MB		512 MB		1 GB		1 GB			
	×64		×64		×64		×64			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–5		–6		–5		–6			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	432	520	368	456	440	557	376	493	mA	3)
I_{DD1}	472	576	408	496	480	613	416	533	mA	3)4)
I_{DD2P}	8	37	8	37	16	74	16	74	mA	5)
I_{DD2F}	176	240	160	216	352	480	320	432	mA	5)
I_{DD2Q}	120	176	112	160	240	352	224	320	mA	5)
I_{DD3P}	64	112	64	112	128	224	128	224	mA	5)
I_{DD3N}	208	296	184	272	416	592	368	544	mA	5)
I_{DD4R}	456	552	392	512	464	589	400	549	mA	3)4)
I_{DD4W}	456	552	392	512	464	589	400	549	mA	3)
I_{DD5}	984	1168	880	1008	992	1205	888	1045	mA	5)
I_{DD6}	12	40	12	40	24	80	24	80	mA	5)
I_{DD7}	1328	1584	1112	1424	1336	1621	1120	1461	mA	3)4)

1) DRAM component currents only
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx}[component] + **n** × I_{DD2P}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

TABLE 12

I_{DD} Specification for HYS72D[64/128]3x0EU–[5/6]–D

Product Type	HYS72D64300EU–5–D		HYS72D64300EU–6–D		HYS72D128320EU–5–D		HYS72D128320EU–6–D		Unit	Note [1)2)]
Organization	512 MB		512 MB		1 GB		1 GB			
	×72		×72		×72		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–5		–6		–5		–6			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	486	585	414	513	495	626	423	554	mA	3)
I_{DD1}	531	648	459	558	540	689	468	599	mA	3)4)
I_{DD2P}	9	41	9	41	18	83	18	83	mA	5)
I_{DD2F}	198	270	180	243	396	540	360	486	mA	5)
I_{DD2Q}	135	198	126	180	270	396	252	360	mA	5)
I_{DD3P}	72	126	72	126	144	252	144	252	mA	5)
I_{DD3N}	234	333	207	306	468	666	414	612	mA	5)
I_{DD4R}	513	621	441	576	522	662	450	617	mA	3)4)
I_{DD4W}	513	621	441	576	522	662	450	617	mA	3)
I_{DD5}	1107	1314	990	1134	1116	1355	999	1175	mA	5)
I_{DD6}	14	45	14	45	27	90	27	90	mA	5)
I_{DD7}	1494	1782	1251	1602	1503	1823	1260	1643	mA	3)4)

1) DRAM component currents only
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx}[component] + **n** × I_{DD2P}[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx}[component]

3.3 AC Characteristics

This chapter describes the AC characteristics.

TABLE 13
AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition[1)]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK}	5	12	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	Min. (t_{CL}, t_{CH})	—	Min. (t_{CL}, t_{CH})	—	ns	2)3)4)5)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}		+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	Fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	Slow slew rate 3)4)5)6)10)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)8)

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition[1)]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	Fast slew rate 3)4)5)6)9)
		0.7	—	0.8	—	ns	Slow slew rate 3)4)5)6)10)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	t_{RCD}	—	t_{RCD}	—	ns	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)10)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	70	—	72	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)11)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)12)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)
2) Input slew rate ≥ 1 V/ns for DDR400, DDR333
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.
6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) These parameters guarantee device timing, but they are not necessarily tested on each device.
9) Fast slew rate ≥ 1.0 V/ns, slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.
10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 14
HYS[64/72]D[64/128]3x0-5-D

Product Type		**HYS64D64300EU–5–D**	**HYS72D64300EU–5–D**	**HYS64D128320EU–5–D**	**HYS72D128320EU–5–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82

Product Type		**HYS64D64300EU–5–D**	**HYS72D64300EU–5–D**	**HYS64D128320EU–5–D**	**HYS72D128320EU–5–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	75	75	75
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	70	70	70	70
27	t_{RPmin} [ns]	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28
31	Module Density per Rank	80	80	80	80
32	$t_{AS,}$ t_{CS} [ns]	60	60	60	60
33	$t_{AH,}$ t_{CH} [ns]	60	60	60	60
34	t_{DS} [ns]	40	40	40	40
35	t_{DH} [ns]	40	40	40	40
36 - 40	Not used	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37
42	t_{RFCmin} [ns]	41	41	41	41

Product Type		HYS64D64300EU–5–D	HYS72D64300EU–5–D	HYS64D128320EU–5–D	HYS72D128320EU–5–D
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U–30331	PC3200U–30331	PC3200U–30331	PC3200U–30331
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
43	t_{CKmax} [ns]	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	01	01	01	01
48 - 61	Not used	00	00	00	00
62	SPD Revision	10	10	10	10
63	Checksum of Byte 0-62	AF	C1	B0	C2
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	45	45	30	30

Product Type		**HYS64D64300EU–5–D**	**HYS72D64300EU–5–D**	**HYS64D128320EU–5–D**	**HYS72D128320EU–5–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**	**PC3200U–30331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
82	Part Number, Char 10	55	55	45	45
83	Part Number, Char 11	35	35	55	55
84	Part Number, Char 12	44	44	35	35
85	Part Number, Char 13	20	20	44	44
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

TABLE 15
HYS[64/72]D[64/128]3x0-6-D

Product Type		**HYS64D64300EU–6–D**	**HYS72D64300EU–6–D**	**HYS64D128320EU–6–D**	**HYS72D128320EU–6–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1

Product Type		**HYS64D64300EU–6–D**	**HYS72D64300EU–6–D**	**HYS64D128320EU–6–D**	**HYS72D128320EU–6–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	80	80
32	$t_{AS,}$ t_{CS} [ns]	75	75	75	75
33	$t_{AH,}$ t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	Not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D
45	t_{QHSmax} [ns]	55	55	55	55
46	not used	00	00	00	00
47	DIMM PCB Height	01	01	01	01
48 - 61	Not used	00	00	00	00
62	SPD Revision	10	10	10	10
63	Checksum of Byte 0-62	53	65	54	66
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F

Product Type		**HYS64D64300EU–6–D**	**HYS72D64300EU–6–D**	**HYS64D128320EU–6–D**	**HYS72D128320EU–6–D**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**	**PC2700U–25331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	45	45	30	30
82	Part Number, Char 10	55	55	45	45
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	44	44	36	36
85	Part Number, Char 13	20	20	44	44
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x

Product Type		HYS64D64300EU–6–D	HYS72D64300EU–6–D	HYS64D128320EU–6–D	HYS72D128320EU–6–D
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25331	PC2700U–25331	PC2700U–25331	PC2700U–25331
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0	Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX	HEX	HEX
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

TABLE 16
HYS64D32301EU-[5/6]-D

Product Type		HYS64D32301EU–5–D	HYS64D32301EU–6–D
Organization		256MB	256MB
		×64	×64
		1 Rank (×16)	1 Rank (×16)
Label Code		PC3200U–30331	PC2700U–25331
JEDEC SPD Revision		Rev. 1.0	Rev. 1.0
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80
1	Total number of Bytes in E2PROM	08	08
2	Memory Type (DDR = 07h)	07	07
3	Number of Row Addresses	0D	0D
4	Number of Column Addresses	0A	0A
5	Number of DIMM Ranks	01	01
6	Data Width (LSB)	40	40
7	Data Width (MSB)	00	00
8	Interface Voltage Levels	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70
11	Error Correction Support	00	00
12	Refresh Rate	82	82
13	Primary SDRAM Width	10	10
14	Error Checking SDRAM Width	00	00
15	t_{CCD} [cycles]	01	01
16	Burst Length Supported	0E	0E
17	Number of Banks on SDRAM Device	04	04
18	CAS Latency	1C	0C
19	CS Latency	01	01
20	Write Latency	02	02
21	DIMM Attributes	20	20
22	Component Attributes	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	70	00
27	t_{RPmin} [ns]	3C	48
28	t_{RRDmin} [ns]	28	30
29	t_{RCDmin} [ns]	3C	48

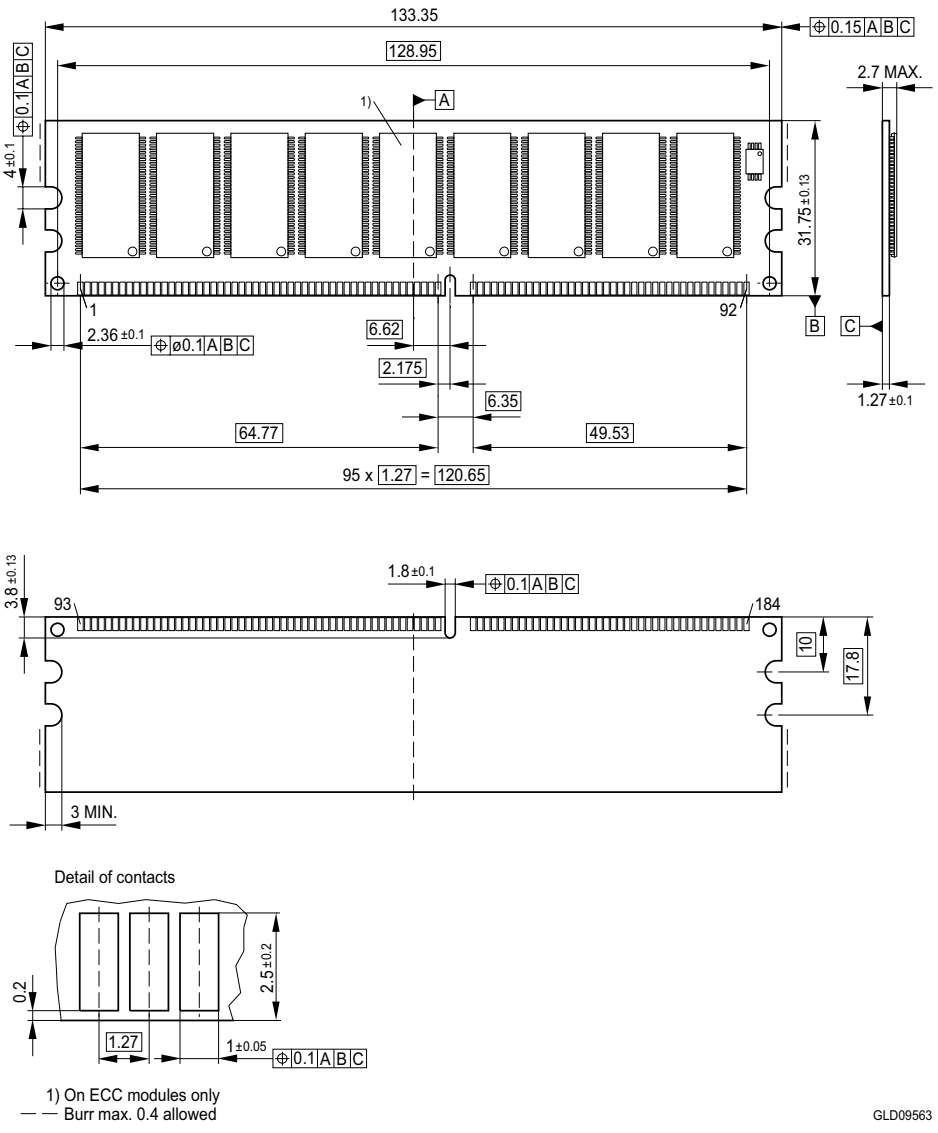
Product Type		**HYS64D32301EU–5–D**	**HYS64D32301EU–6–D**
Organization		**256MB**	**256MB**
		×64	**×64**
		1 Rank (×16)	**1 Rank (×16)**
Label Code		**PC3200U–30331**	**PC2700U–25331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**
30	t_{RASmin} [ns]	28	2A
31	Module Density per Rank	40	40
32	$t_{AS,}$ t_{CS} [ns]	60	75
33	$t_{AH,}$ t_{CH} [ns]	60	75
34	t_{DS} [ns]	40	45
35	t_{DH} [ns]	40	45
36 - 40	Not used	00	00
41	t_{RCmin} [ns]	37	3C
42	t_{RFCmin} [ns]	41	48
43	t_{CKmax} [ns]	28	30
44	$t_{DQSQmax}$ [ns]	28	2D
45	t_{QHSmax} [ns]	50	55
46	not used	00	00
47	DIMM PCB Height	01	01
48 - 61	Not used	00	00
62	SPD Revision	10	10
63	Checksum of Byte 0-62	76	1A
64	Manufacturer’s JEDEC ID Code (1)	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Part Number, Char 1	36	36
74	Part Number, Char 2	34	34
75	Part Number, Char 3	44	44
76	Part Number, Char 4	33	33
77	Part Number, Char 5	32	32
78	Part Number, Char 6	33	33
79	Part Number, Char 7	30	30

Product Type		**HYS64D32301EU–5–D**	**HYS64D32301EU–6–D**
Organization		**256MB**	**256MB**
		×64	**×64**
		1 Rank (×16)	**1 Rank (×16)**
Label Code		**PC3200U–30331**	**PC2700U–25331**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 1.0**
Byte#	**Description**	**HEX**	**HEX**
80	Part Number, Char 8	31	31
81	Part Number, Char 9	45	45
82	Part Number, Char 10	55	55
83	Part Number, Char 11	35	36
84	Part Number, Char 12	44	44
85	Part Number, Char 13	20	20
86	Part Number, Char 14	20	20
87	Part Number, Char 15	20	20
88	Part Number, Char 16	20	20
89	Part Number, Char 17	20	20
90	Part Number, Char 18	20	20
91	Module Revision Code	0x	0x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx
99 - 127	Not used	00	00

5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 2
Package Outline UDIMM Raw Card A (L-DIM-184-30)



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 3
Package Outline UDIMM Raw Card B (L-DIM-184-31)

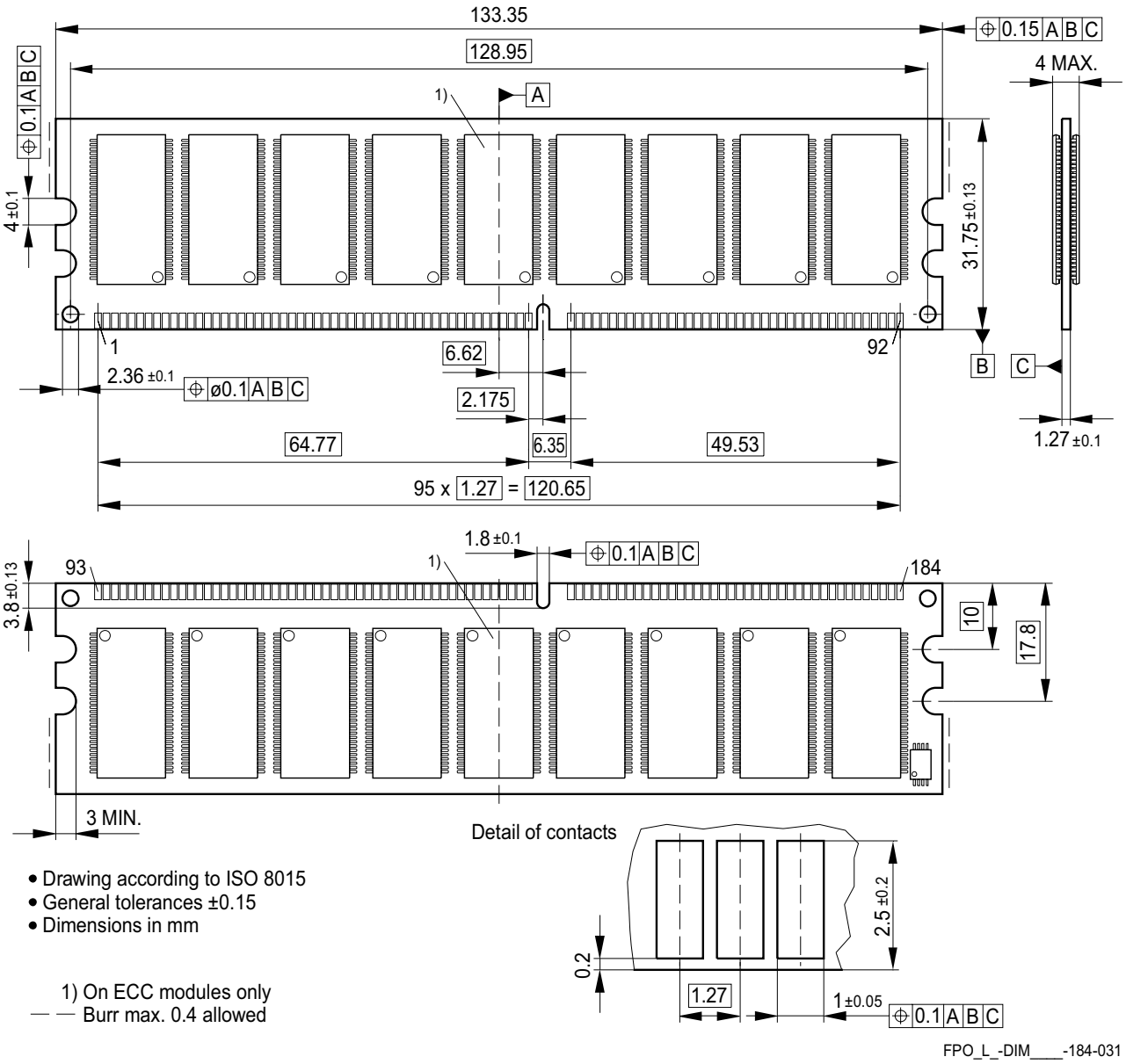
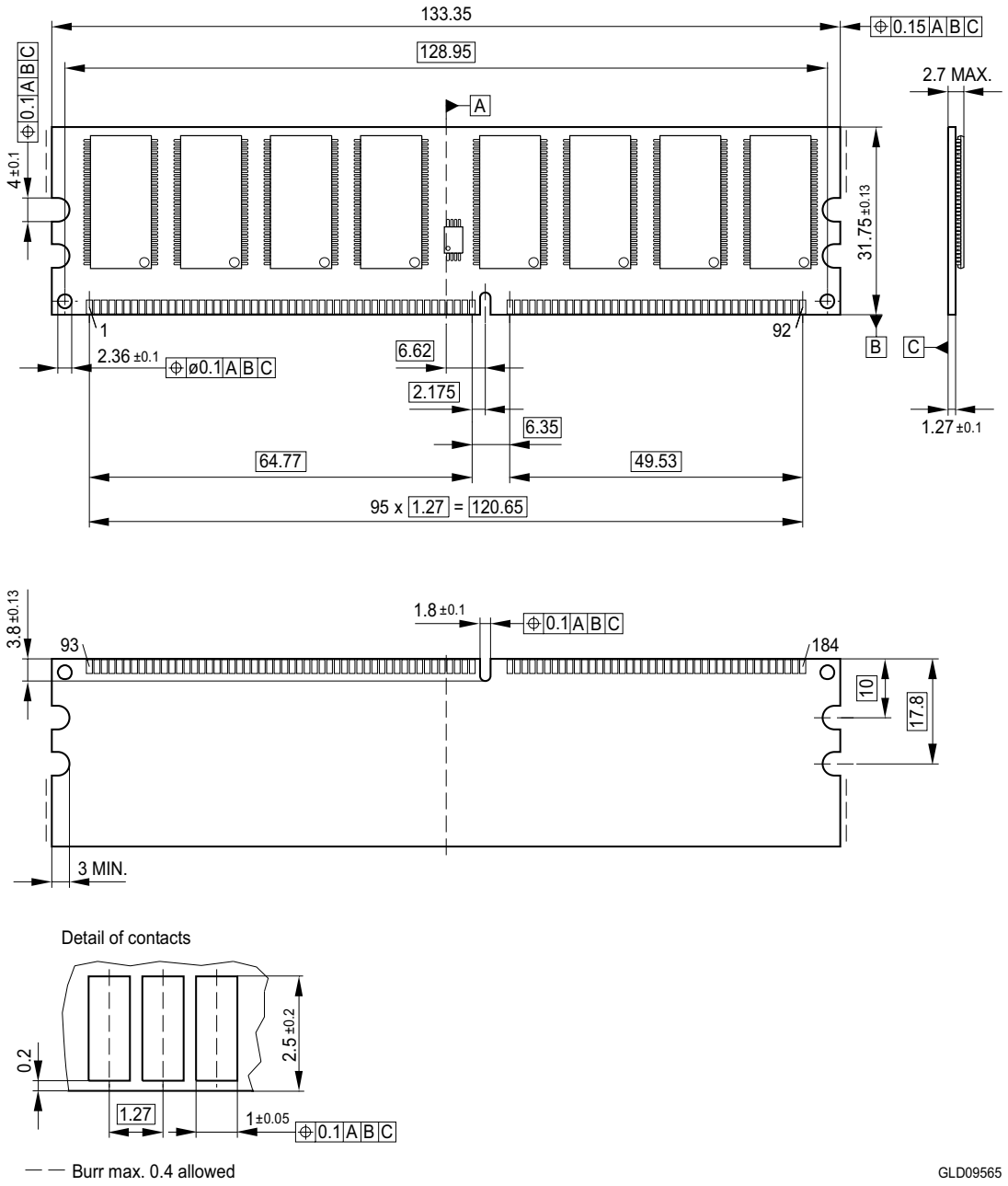


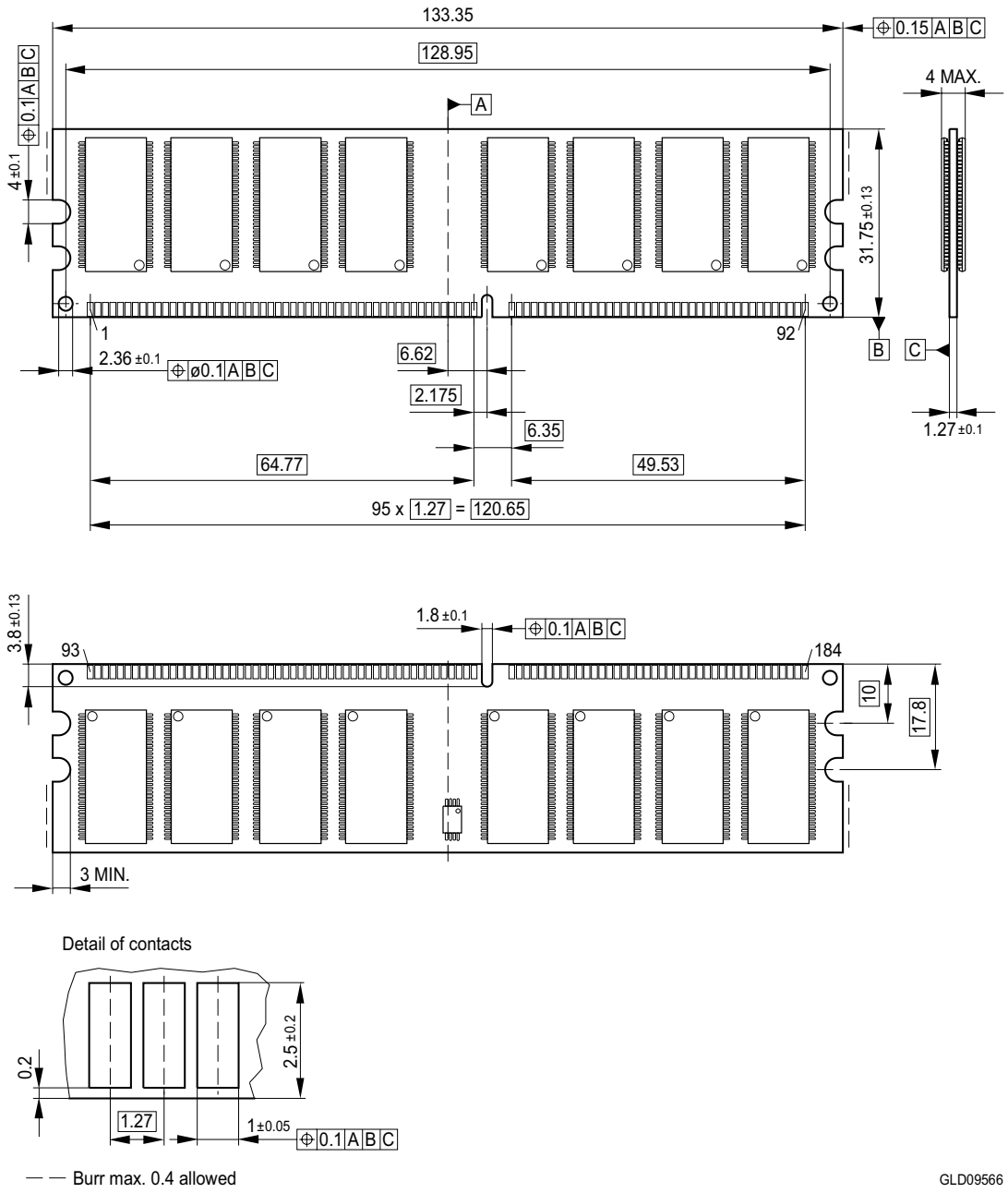
FIGURE 4
Package Outline UDIMM Raw Card A (L-DIM-184-32)



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

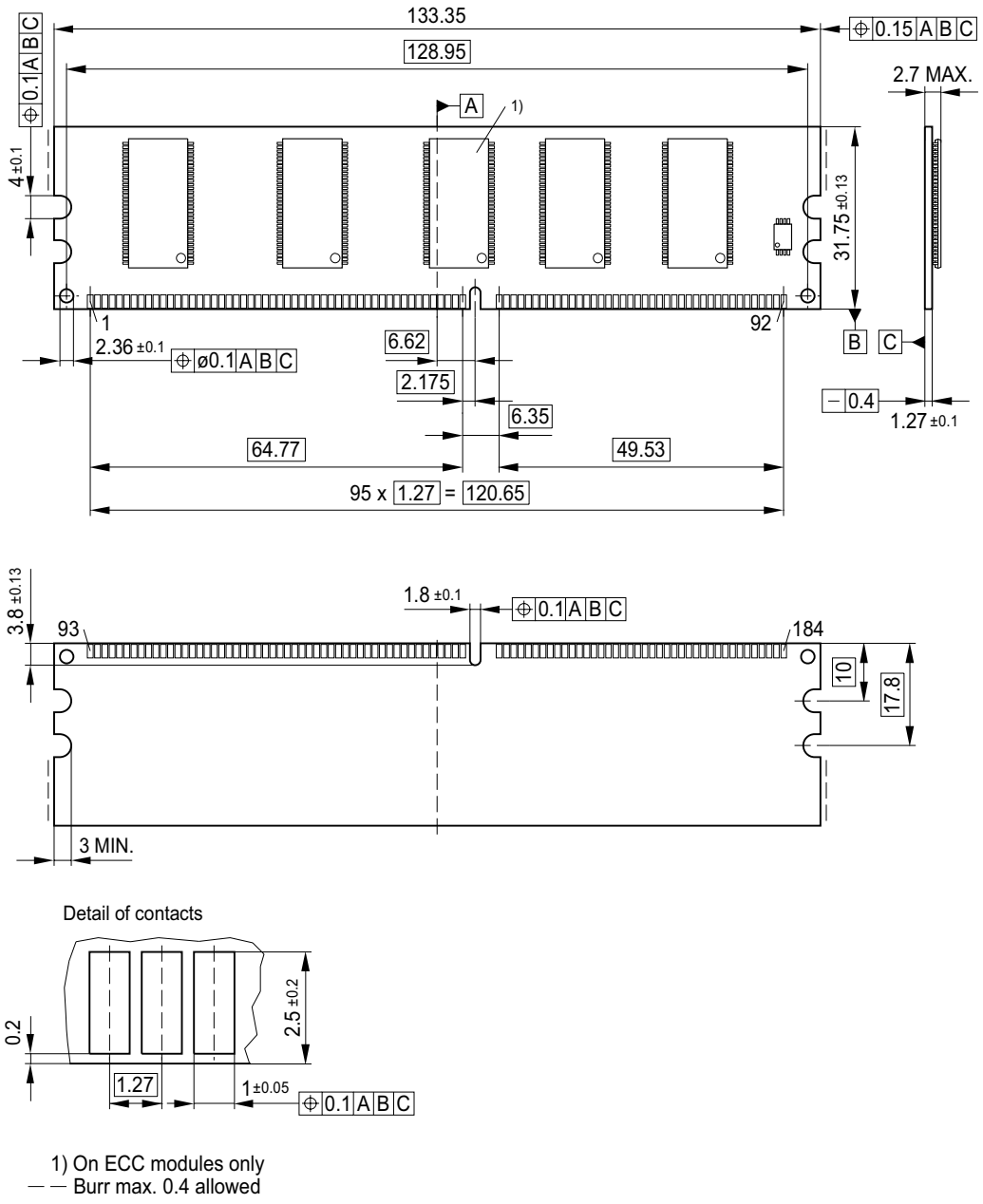
FIGURE 5
Package Outline UDIMM Raw Card B (L-DIM-184-33)



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 6
Package Outline UDIMM Raw Card C (L-DIM-184-18)



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

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Edition 2008-05
Published by Qimonda AG
Gustav-Heinemann-Ring 212
D-81739 München, Germany

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