FAIRCHILD
A Schlumberger Company

F1600
65,536 x 1-Bit Static RAM

Description

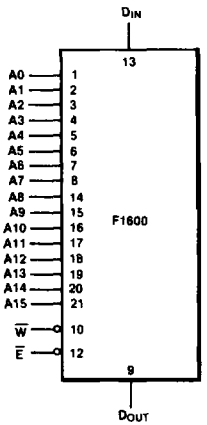
The F1600 is a 65,536-bit fully static asynchronous random access memory, organized as 65,536 words by 1-bit, using high-performance CMOS technology. The F1600 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

- **Single +5V Operation (±10%)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Fast Access Time: 45 ns/55 ns/70 ns (Maximum)**
- **Low Power Dissipation:**
  - **70 mA Maximum (Active)**
  - **20 mA Maximum (Standby — TTL Input Levels)**
  - **5 mA Maximum (Standby — CMOS Input Levels)**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Three-State Output**
- **Available in a 22-Pin DIP or LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

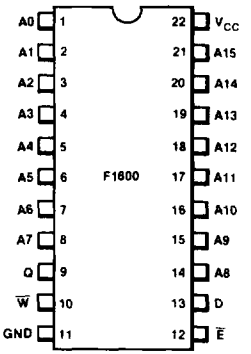
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Logic Symbol



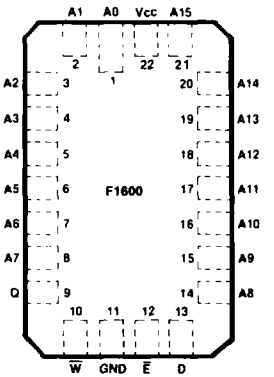
Connection Diagrams

22-Pin DIP (Top View)



22-Pin LCC (Top View)

F1600 LCC



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Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to GND	– 2.0 V to 7.0 V
Storage Temperature	-55° C to +150° C
Operating Temperature	0° C to +70° C
Power Dissipation	1.0 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions: T_C = 0° C to +70° C

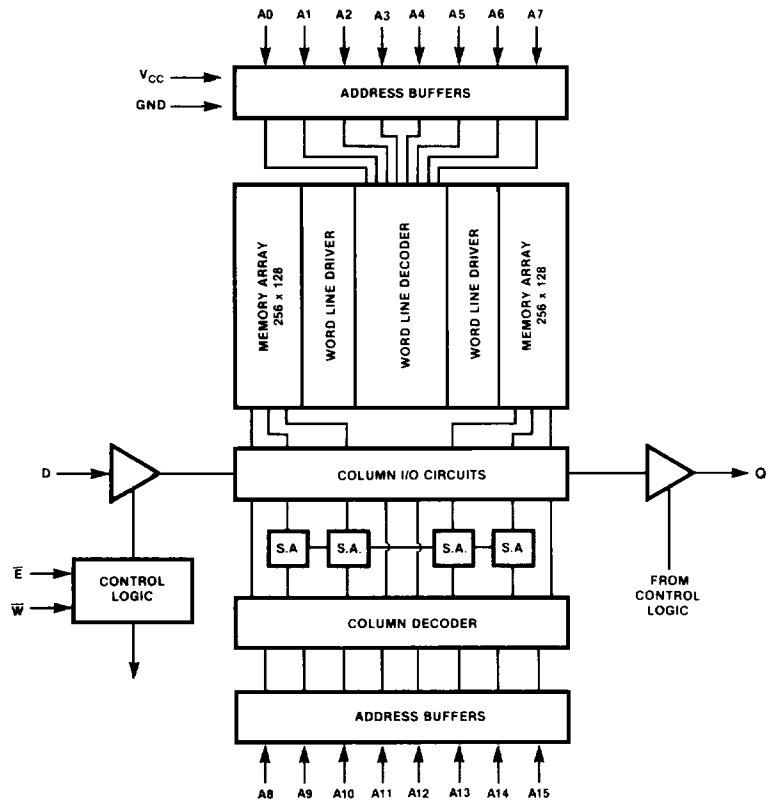
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		6.0	V
V_{IL}	Input LOW Voltage	-0.5*		0.8	V

All voltages are referenced to GND pin = 0 V.

*The device will withstand undershoots to -3.0 V of 20 ns duration. This is guaranteed by bench simulation in a DC mode, not 100% tested.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



DC Operating Characteristics: T_C = 0° C to +70° C, V_{CC} = 5.0V ±10%

Symbol	Characteristic	F1600-45			F1600-55			F1600-70			Unit	Condition
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max		
I_{IN}	Input Leakage Current (All inputs)			±2			±2			±2	μA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
I_{OUT}	Output Leakage Current (on Q)			±2			±2			±2	μA	$\overline{E}$ = V_{IH} V_{OUT} = 0 V to V_{CC}
I_{CC1}	Operating Power Supply Current		40	70		40	70		40	70	mA	$\overline{E}$ = V_{IL}, Output Open
I_{CC2}	Dynamic Operating Supply Current		40	70		40	70		40	70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current		5	20		5	20		5	20	mA	$\overline{E} \geq V_{IH}$, see *note 1*
I_{SB2}	Full Standby Supply Current		0.02	5.0		0.02	5.0		0.02	5.0	mA	see *note 2*
I_{OS}	Output Current Short Circuit to Ground			-125			-125			-125	mA	V_{CC} = 5.5 V Duration not to Exceed 1 Second
V_{OL}	Output LOW Voltage			0.4			0.4			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output HIGH Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0 mA

AC Test Conditions[3]

Input Pulse Levels ..... GND to 3.0 V
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 V
Output Load ..... *See Figures 1 and 2*

Capacitance[4] T_C = +25° C, f = 1.0 MHz

Symbol	Parameter	Max.	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0 V

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where Δ V = 3 V.

Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

Figure 1 Output Load

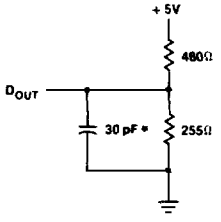
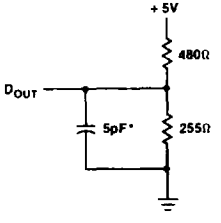


Figure 2 Output Load (for t_{EHQZ}, t_{ELQX}, t_{WLQZ}, t_{WHQX})



*Including scope and jig.

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AC Operating Conditions and Characteristics: Read Cycle T_C = 0° C to +70° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
1	t_{AVAV}	t_{RC}	Address Valid to Address Valid (Read Cycle Time)	45		55		70		ns	5,6,9
2	t_{AVQV}	t_{AA}	Address Valid to Output Valid (Address Access Time)		45		55		70	ns	5
3	t_{AXQX}	t_{OH}	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns	
4	t_{ELEH}	t_{RC}	Chip Enable LOW to Chip Enable HIGH (Read Cycle Time)	45		55		70		ns	6,9
5	t_{ELQV}	t_{ACS}	Chip Enable LOW to Output Valid (Chip Enable Access Time)		45		55		70	ns	6
6	t_{ELQX}	t_{LZ}	Chip Enable LOW to Output Invaild (Chip Enable to Output Active)	0		0		0		ns	4
7	t_{EHQZ}	t_{HZ}	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	20	0	25	0	30	ns	4, 10
8	t_{ELICCH}	t_{PU}	Chip Enable LOW to Power Up	0		0		0		ns	4
9	t_{EHICCL}	t_{PD}	Chip Enable HIGH to Power Down		40		40		40	ns	4

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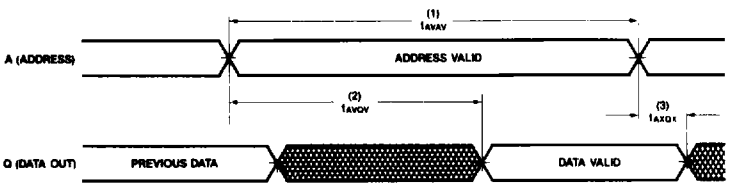
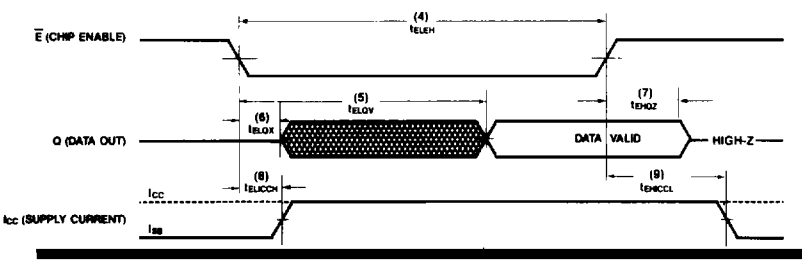
Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to address change. $\overline{W}$ = HIGH)



Read Cycle 2 (Where address is valid prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH)



AC Operating Conditions and Characteristics: Write Cycle 1 T_C = 0° C to +70° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
10	t_{AVAV}	t_{WC}	Address Valid to Address Valid (Write Cycle Time)	45		55		70		ns	7,8,9
11	t_{ELWH}	t_{CW}	Chip Enable to Write HIGH (Chip Enable to End of Write)	40		45		55		ns	11
12	t_{AVWH}	t_{AW}	Address Valid to Write HIGH (Address Setup to End of Write)	40		45		55		ns	11
13	t_{WHAX}	t_{WR}	Write HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	11
14	t_{WLWH}	t_{WP}	Write LOW to Write HIGH (Write Pulse Width)	20		25		40		ns	11
15	t_{AVWL}	t_{AS}	Address Valid to Write LOW (Address Setup to Beginning of Write)	5		5		5		ns	11
16	t_{DVWH}	t_{DW}	Data Valid to Write HIGH (Data Setup to End of Write)	15		20		30		ns	11
17	t_{WHDX}	t_{DH}	Write HIGH to Data Don't Care (Data Hold After End of Write)	0		0		0		ns	11
18	t_{WLQZ}	t_{WZ}	Write LOW to Output High Z (Write Enable to Output Disable)	0	20	0	25	0	30	ns	4, 10
19	t_{WHQX}	t_{OW}	Write HIGH to Output Don't Care (Output Active After End of Write)	0		0		0		ns	4

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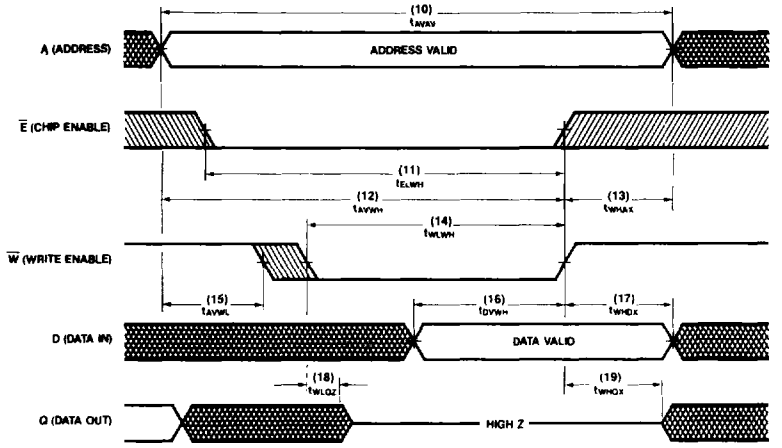
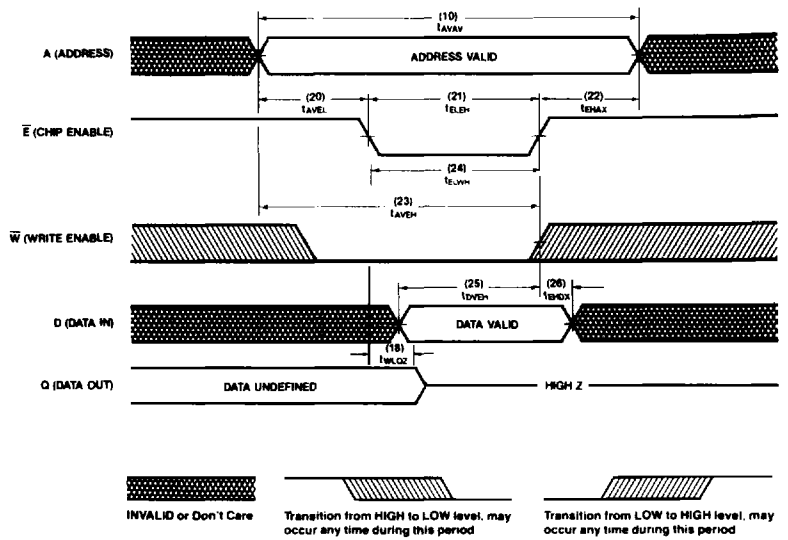
Write Cycle 1 ($\overline{W}$ controlled, where $\overline{E}$ is active prior to $\overline{W}$ becoming active.)



AC Operating Conditions and Characteristics: Write Cycle 2 $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
20	t_{AVEL}	t_{AS}	Address Valid to Chip Enable LOW (Address Set Up)	0		0		0		ns	
21	t_{ELEH}	t_{CW}	Chip Enable LOW to Chip Enable HIGH (Write Cycle Time)	45		55		70		ns	11
22	t_{EHAX}	t_{WR}	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	
23	t_{AVEH}	t_{AW}	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	40		45		55		ns	
24	t_{ELWH}	t_{WP}	Chip Enable LOW to Write HIGH (Write Pulse Width)	30		35		40		ns	11
25	t_{DVEH}	t_{DW}	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	15		20		30		ns	
26	t_{EHDX}	t_{DH}	Chip Enable HIGH to Data Don't Care (Data Hold)	0		0		0		ns	

Write Cycle 2 ($\overline{E}$ controlled, where $\overline{W}$ is active prior to $\overline{E}$ becoming active. *See Note 9.*)



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Notes

1. This parameter is measured with $\overline{E}$ HIGH (chip deselected) and inputs at valid TTL levels.
2. This parameter is measured with input levels either $\geq V_{CC} - 0.2$ V or ≤ 0.2 V, including $\overline{E}$ which must be $\geq V_{CC} - 0.2$ V. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} applied.
4. This parameter is sampled and not 100% tested.
5. Read Cycle 1 assumes that Chip Enable (E) occurs before the addresses are valid. Timing considerations are referenced to the edges of Address Valid.
6. Read Cycle 2 assumes that Address Valid occurs prior to Chip Enable ($\overline{E}$). Timing considerations are referenced to the edges of Chip Enable.
7. Since a write cycle can only occur during intervals where both $\overline{E}$ and $\overline{W}$ are LOW, Write Cycle 1 assumes that $\overline{W}$ is the latter of the two signals to go LOW (active) and is also the first of the two signals to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{W}$ rather than $\overline{E}$.
8. Write Cycle 2 assumes that, of the two control signals, $\overline{E}$ and $\overline{W}$, $\overline{E}$ is the latter of the two to go LOW (active) and is also the first of the two to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{E}$ rather than $\overline{W}$.
9. All READ and WRITE cycle timings are referenced from the last bit to become valid address to the first transitioning address.
10. Transition to high impedance state is measured ±500 mV from steady state voltage with specified loading in *Figure 2*. This parameter is sampled, not 100% tested.
11. Since Write Enable ($\overline{W}$) is gated internally with Chip Enable ($\overline{E}$), the value of $\overline{W}$ during periods where $\overline{E}$ is HIGH is irrelevant (i.e., don't care). Thus, whenever $\overline{W}$ transitions to the LOW state prior to $\overline{E}$, all timing references will be to the falling edge of $\overline{E}$ rather than $\overline{W}$. Similarly, whenever $\overline{E}$ transitions to the HIGH state prior to $\overline{W}$, all timing references will be to the rising edge of $\overline{E}$ rather than $\overline{W}$.
12. Input pulse levels 0 to 3.0 Volts.
13. Input rise and fall times are assumed to be 5 ns. Timing measurement reference levels are 1.5 Volts.
14. Rise and fall times should not exceed 45 ns.

Ordering Information

Part Number	Access Time	Temperature Range	Package	Order Code
F1600-45	45 ns	0°C to + 70°C	Side-brazed	1600DC45
F1600-45	45 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC45
F1600-45	45 ns	0°C to + 70°C	Plastic DIP	1600PC45
F1600-55	55 ns	0°C to + 70°C	Side-brazed	1600DC55
F1600-55	55 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC55
F1600-55	55 ns	0°C to + 70°C	Plastic DIP	1600PC55
F1600-70	70 ns	0°C to + 70°C	Side-brazed	1600DC70
F1600-70	70 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC70
F1600-70	70 ns	0°C to + 70°C	Plastic DIP	1600PC70