

Electrical Characteristics: $-30^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; $-30^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$; All Parameters after V_{CC} Power-up $> 100\text{ms}$;
 $V_{BAT} = 14\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	16 Lead SO Wide			Flip Chip			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
■ Input, Current, Delay								
Positive Threshold	$V_{BAT} = 6\text{V}$		56.2	66		56.2	66	% of V_{BAT}
	$V_{BAT} = 16\text{V}$		56.2	66		56.2	66	% of V_{BAT}
Hysteresis	$V_{BAT} = 6\text{V}$	8	20.2		9	20.2		% of V_{BAT}
	$V_{BAT} = 16\text{V}$	8	20.2		9	20.2		% of V_{BAT}
I_{CC}	$V_{BAT} = 6\text{V}$	1	2.75	4.5	1	2.75	4.5	mA
	$V_{BAT} = 16\text{V}$	5	12	19	5	12	19	mA
Input Impedance	@10 μA	70	170	400				k Ω
	@0.1mA				70	170	400	k Ω
IC Process Delay				15			15	μs
■ Output								
Output Current	$V_{BAT} = 6\text{V}$, 2.1V output load	40	52.5	65	40	52.5	65	mA
Output SOA Current	$V_{BAT} = 22\text{V}$ (Note 1)	40	52.5	65	40	52.5	65	mA
Output Leakage Current	$V_{BAT} = 25\text{V}$ (Note 1)		0	100		0	100	μA
Output Clamp Voltage	@ 10mA	13.7	15.35	17	13.7	15.35	17	V
Output Clamp Impedance	@ 10mA	10	42.5	80	10	42.5	80	Ω
■ Regulation Voltage								
VS Regulation Voltage	$V_{BAT} = 7.8\text{V}$	165	200	235	165	200	235	mV
VS Supply Rejection	$V_{BAT} = 6\text{V} \sim 22\text{V}$ (Note 1)	0	0	14	0	0	14	%
	$V_{BAT} = 7.8\text{V} \sim 22\text{V}$ (Note 1)	0	0	13	0	0	13	%
■ Stall & Protection								
Stall Shutdown VS	$V_{BAT} = 6\text{V}$	-5	0	5	-1	0	1	mV
Stall Shutdown Frequency	$V_{BAT} = 14\text{V}$.4			.4			Hz
	$V_{BAT} = 5.5\text{V}$		1.4	1.47		1.4	1.47	Hz
Stall Shutdown Time	$V_{BAT} = 6\text{V}$	19	28	37	19	28	37	ms
Stall to Spark Output Delay		4.6	6.7	9.5	4.6	6.7	9.5	ms
I/O Signal Relationship	@ 80% Input	79.0	80.5	82.0	79.0	80.0	81.0	%
	@ 50% Input	49.0	50.5	52.0	49.0	50.0	51.0	%
	@ 30% Input	29.0	30.5	32.0	29.0	30.0	31.0	%
Battery Interrupt Time		25		750	25		750	ms
Battery Interrupt Recovery Time	@ 200Hz			800			800	ms
High Voltage Shutdown		25	28	32	25	28	31	V
High Frequency Cut off		1	2.5	5	1	2.5	5	kHz
Negative Threshold	$V_{BAT} = 6\text{V}$	28	36		30	36		% of V_{BAT}
	$V_{BAT} = 16\text{V}$	28	36		30	36		% of V_{BAT}

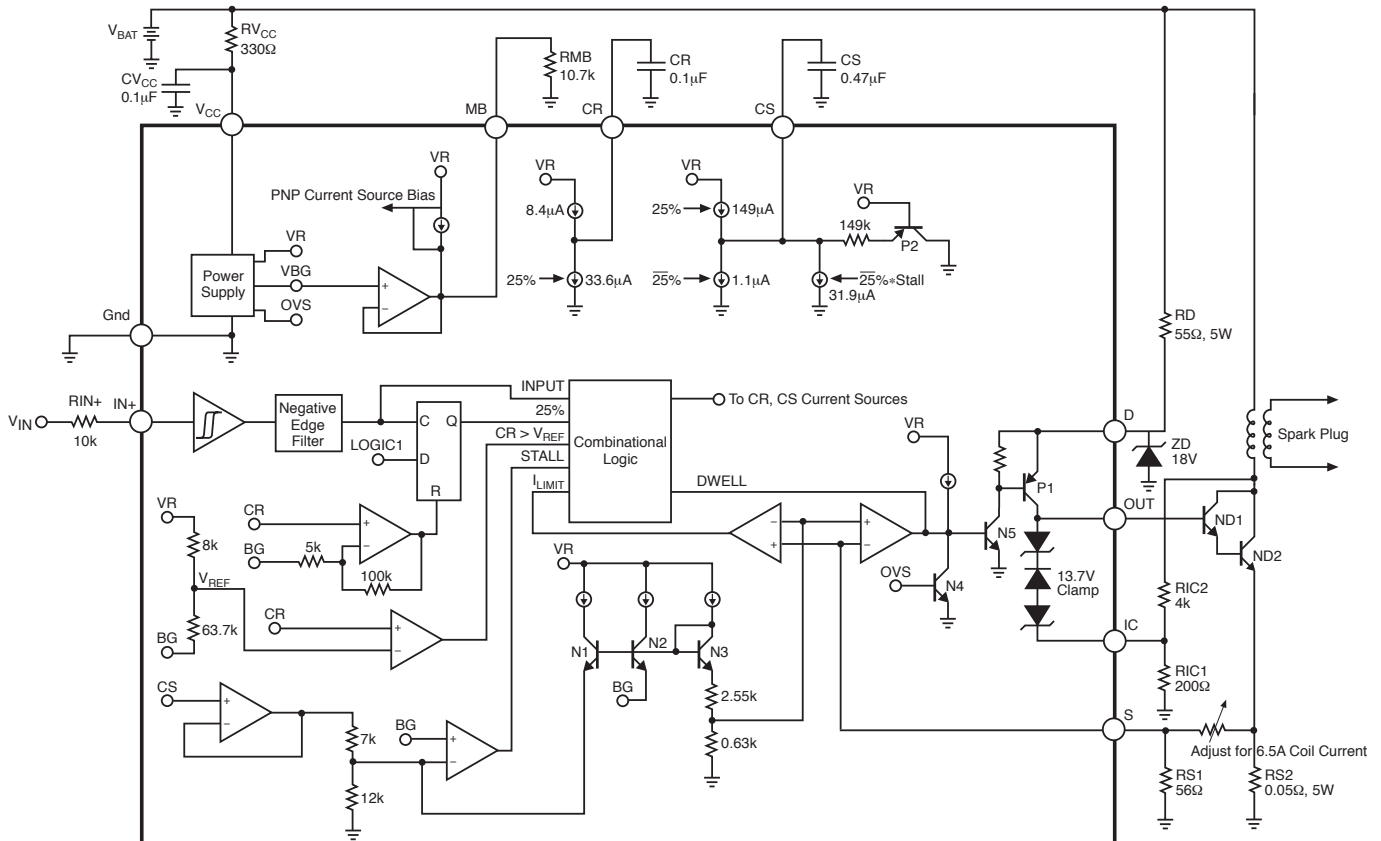
Note 1: Voltage extremes are for testing purposes only. Part in continuous operation should conform to absolute max table.

Package Pin Description

CS464

PACKAGE PIN #	PIN SYMBOL	FUNCTION	
Flip-Chip (Bump #)	16 Lead SO Wide		
1	13	OUT	Output control of darlington driver.
2	15	S	Current sense feedback input.
3	16	CS	Stall timer capacitor.
4	1	MB	Master current bias resistor.
5	2,3,6,7,10,14	NC	No connection.
6	4	CR	Reset capacitor.
7	5	IN+	Input control.
8		IN-	Negative input control (grounded in 16 Lead SO package).
9	8	Gnd	Ground.
10	9	V _{CC}	Input supply voltage.
11	11	D	Darlington drive supply input.
12	12	IC	Input collector voltage sense.
13		TEST	Test bump, grounded.

Block Diagram



Package Specification

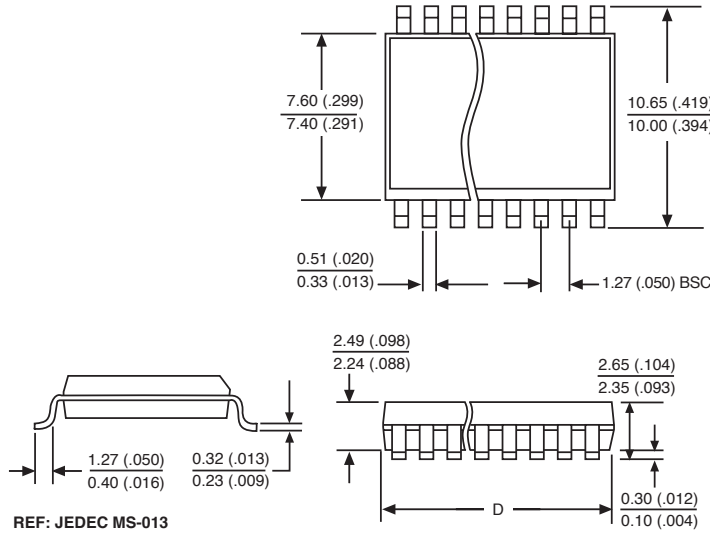
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead SO Wide	10.50	10.10	.413	.398

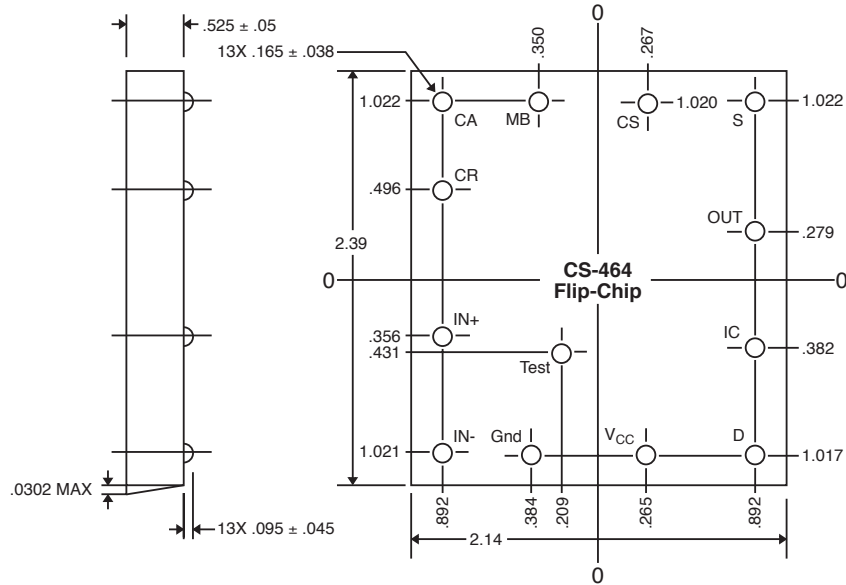
PACKAGE THERMAL DATA

Thermal Data	16 Lead SO Wide		
R _{θJC}	typ	23	°C/W
R _{θJA}	typ	105	°C/W

Surface Mount Wide Body (DW); 300 mil wide



Flip-Chip



Note: All dimensions in millimeters.

Bump Locations, Bump Side Up

Ordering Information

Part Number	Description
CS464	Flip-Chip
CS464YDW16	16 Lead SO Wide
CS464YDWR16	16 Lead SO Wide (tape & reel)

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.