OAT1041x-V5-z-yy(for 12km)

OC-192/STM-64 SERDES Transceiver Module

Document Number: QPS-0302-020
Revision: DRAFT 0.5
DATE: Oct.17.2002
Author: *T.ITOU*
Project Manager: *T. ITOU*

Modification History

Rev.	Date	Originator	Comment
DRAFT0.1	**Aug.16.2002**	***T.Itou***	
DRAFT0.2	**Sep.05.2002**	***T.Itou***	
DRAFT0.3	**Sep.25.2002**	***T.Itou***	Revision of Absolute maximum of VEE
DRAFT0.4	**Oct.2.2002**	***T.Itou***	Additional of I2C diagnostic monitor
DRAFT0.4	**Oct.17.2002**	***T.Itou***	Change of Distance

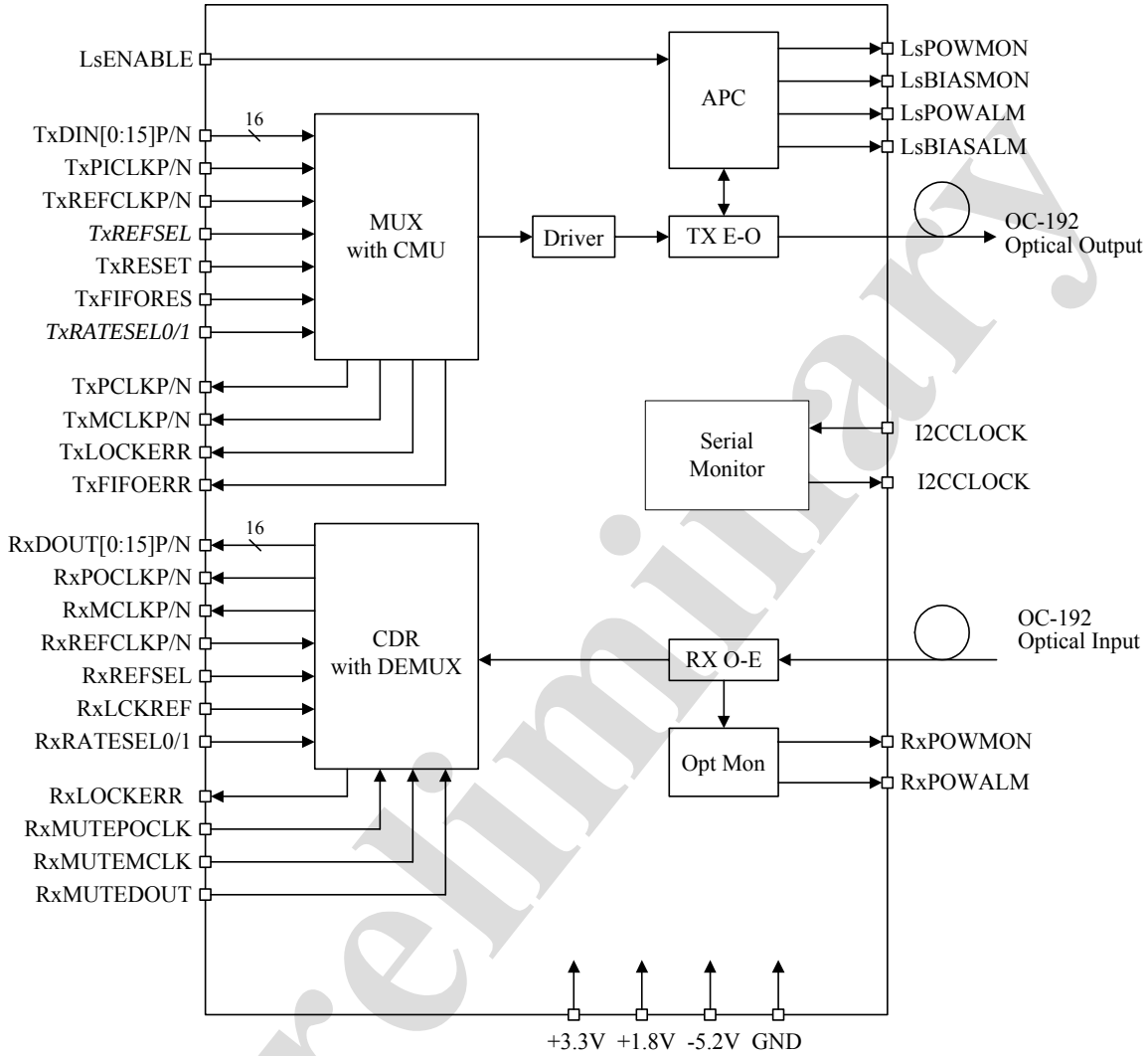
Features ;

- 10G SFF Transceiver
- SONET/SDH 9.953Gbps operation
  · SR-1/I64.1 @ OAT1041x-V5-A-yy
- Support 10.3Gbps(10GbE), 10.66Gbps(FEC) and 10.7Gbps(OTN) rate
- Wavelength : 1310nm band
- Transmission Distance :
  ·12km(40ps/nm) @OAT1041x-V5-A-yy
- Dispersion Penalty : <1dB
- 16-bit parallel 622.08Mbps(equivalent FEC rate) LVDS data interface
- SERDES Timing compliant with OIF1999.102.8 SFI-4 interface
- Jitter filter built-in (OAT1041x-V5-C-yy, Multi-rate type removes)
- TxREFCLK frequency of 622MHz is standard. (OAT1041x-V5-C-yy, Multi-rate type removes)
- Compact size: 50.8 x 76.2 x 11.5 (mm)
- Supply voltage : +3.3V , +1.8V and -5.2V
- Low power consumption: <4.8W max.(3.8W typ.)
- I2C compatible bus for simple status data monitor

Application ;

- Metro network SONET/SDH system
- 10 Gigabit Ethernet system
- Forward Error Correction system
- Optical Transport Network (OTN) System

1.Block diagram



∗ *TxREFSEL,TxRATESEL0/1* are available for multi-rate type, OAT1041x-V5-C-yy.

Figure 1 Block diagram

2.Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD1}	-0.5	3.6	V
	V_{DD2}	-0.5	2.0	V
	V_{EE}	-6.0	+0.5	V
LVDS input pin	—	0	2.7	V
LVTTL input pin	—	0	3.6	V
LVTTL output sink current	—	—	50	mA
LVTTL output source current	—	—	-50	mA
Optical Input Power	Pin_max	—	3	dBm
Tension of fiber	—	—	500	g
Fiber Bend Radius	—	30	—	mm
Storage Temperature	Tstg	-40	85	degC

3.Operating Environment

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 3 Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD1}	3.13	3.3	3.46	V
	V_{DD2}	1.71	1.8	1.89	
	V_{EE}	-4.94	-5.2	-5.46	
Supply Current	I_{DD1}			0.4	A
	I_{DD2}			1.2	
	I_{EE}			0.5	
Case Temperature	Tc	0		70	degC
Power consumption		—	3.8	4.8	W

4.Specifications

4-1 Optical interface specifications

Table 4.1 Optical interface specifications

Parts Number		**1041x-V5-A-yy**			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Note**
Bit rate		9.95328		Gbit/s	
Transmitter					
Optical output power	Po	-6	-1	dBm	
Optical waveform		OC-192/STM-64 Unamplified Mask standard			Figure 4.1 G.693
Center wavelength	λc	1290	1330	nm	
Extinction ratio	Er	6.0	—	dB	
Spectral maximum –20dB Width	$\Delta\lambda_{20}$	—	1.0	nm	
Side mode suppression ratio	SMSR	30	—	dB	
Receiver					
Minimum sensitivity	Pin	—	-14	dBm	BER@1x10^{-12}
Minimum overload	Pin	-1	—	dBm	
Input wavelength	λc_rx	1280	1580	nm	
Rx Return loss		27		dB	
Jitter performance					
Jitter Generation		—	0.1	UIp-p	Bandpass filter; 50k to 80MHz
Jitter Tolerance and Transfer		Compliant with GR-253			Figure 4.2,4.3
Optical path					
Dispersion	D_{Lrmax}	—	40	ps/nm	
Optical Path Penalty		—	1	dB	

Condition; Case temperature: 0 to 70degC, NRZ,PRBS2^{31}-1, Mark ratio: 1/2,
Supply voltage:+3.3V,+1.8V,-5.2V each +/-5%

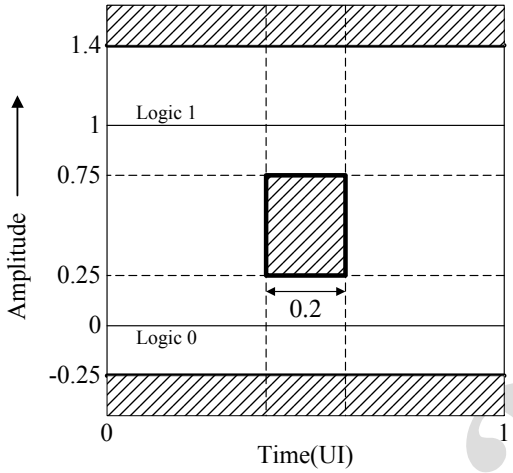


Figure 4.1 Eye pattern mask

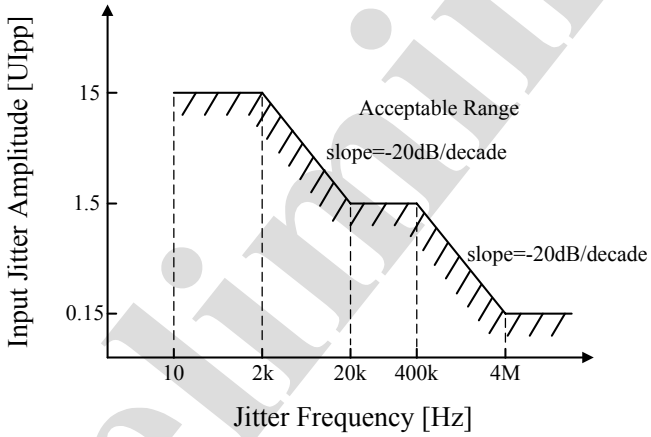


Figure 4.2 Jitter Tolerance mask

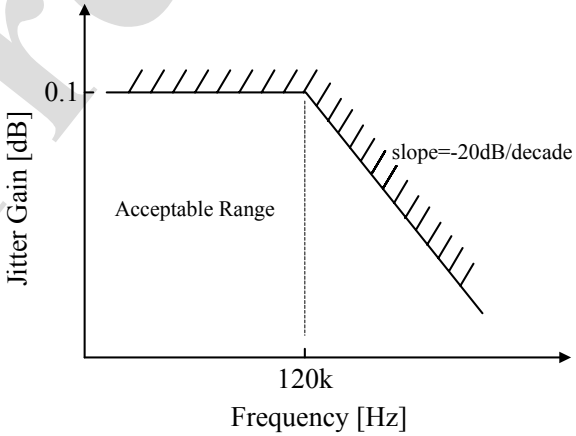


Figure 4.3 Jitter Transfer mask

4-2 Electrical Interface

Table 4.2.1 Reference clock characteristics

Symbol	Parameter	Min.	Typ	Max.	Units	Interface	Notes
Tx Reference Clock							
TxREFCLKP/N[a]	Frequency		622.08		MHz	AC Coupled (Internally has capacitor)	OC-192/STM-64
			155.52				
			644.53				10GbE(10.3Gbps)
			161.13				
			666.51				FEC
			166.63				
			669.32				OTN
			167.33				
			155.52/161.13/166.63/167.33 or 622.08/644.53/666.51/669.32				Multi-rate type.
	Frequency tolelance	-20	—	+20	ppm		OC-192/STM-64
		-100	—	+100			10GbE(10.3Gbps)
	Duty cycle	40	—	60	%		
	Input levels	400	—	900	mV p-p		Single-ended voltage swing
Rx Reference Clock							
RxREFCLKP/N	Frequency		155.52 or 622.08		MHz	AC Coupled (Internally has capacitor)	OC-192/STM-64
			161.13 or 644.53				10GbE(10.3Gbps)
			166.63 or 666.51				FEC
			167.33 or 669.32				OTN
			155.52/161.13/166.63/167.33 or 622.08/644.53/666.51/669.32				Multi-rate type.
	Frequency tolelance	-20	—	+20	ppm		OC-192/STM-64
		-100	—	+100			10GbE(10.3Gbps)
	Duty cycle	40	—	60	%		
	Input levels	400	—	900	mV p-p		Single-ended voltage swing

a. 600MHz operation of TxREFCLK is a standard. Moreover, we can prepare TxREFCLK by *150MHz*.
And only TxREFCLK frequency of multi-rate type, OAT1041x-V5-C-yy, is available to select 150MHz or 600MHz.

Table 4.2.2 Transmitter/Receiver Parallel Data/Clock Interface

	Function	**I/O**	**Interface**	**Note**
Transmitter				
TxDin[0:15]P/N	Transmitter 16-bit parallel Date Input	I	LVDS	TxDin0:LSB, TxDin15:MSB
TxPICLKP/N	Transmitter Source synchronous Parallel Input Clock	I	LVDS	
TxPCLKP/N	Transmitter Counter Clock	O	LVDS	
Receiver				
RxDout[0:15]P/N	Receiver 16-bit parallel Date Output	O	LVDS	RxDout0:LSB, RxDout15:MSB
RxPOCLKP/N	Receiver Source synchronous Parallel Output Clock	O	LVDS	

Table 4.2.3 Transmitter/Receiver Parallel Data/Clock Timing

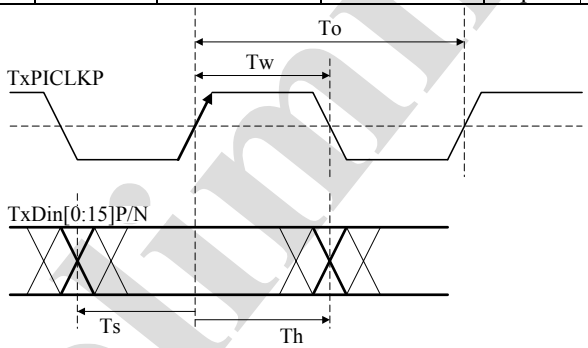
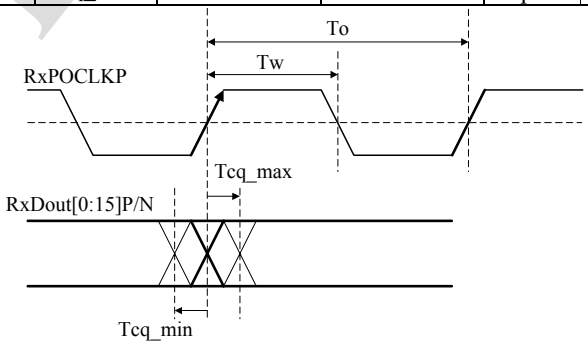
Parameter		**Symbol**	**Min.**	**Max.**	**Units**	**Note**
Transmitter Data/CLK Input Timing						
TxPICLK	Duty cycle	Tw/To	40	60	%	
	Rise time	Tr	—	300	ps	20 – 80%
	Fall time	Tf	—	300	ps	80 – 20%
TxDin	setup time	Ts	300	—	ps	
	hold time	Th	300	—	ps	
						
Receiver Data/CLK Output Timing						
RxPOCLK	Duty cycle	Tw/To	45	55	%	
	Rise time	Tr	—	250	ps	20 – 80%
	Fall time	Tf	—	250	ps	80 – 20%
RxDout	Data/Clock skew	Tcq_min,	—	200	ps	
		Tcq_max	—	200	ps	
						

Table 4.2.4 Monitor Clock

	Function	I/O	Interface	Note
Transmitter				
TxMCLKP/N	Transmitter monitor clock	O	LVDS	f=TxREFCLK frequency
Receiver				
RxMCLKP/N	Receiver monitor clock	O	LVDS	f=RxREFCLK frequency

Table 4.2.5 Transmitter Data Rate select

TxRATESEL0	TxRATESEL1	Function		Note
		Serial Data rate	Parallel Data rate	
H	H	9.95328Gbps	622.08Mbps	LVTTL interface Internal 100 kΩ pull up to V_{DD1}
L	L	10.3125Gbps	644.54Mbps	
H	L	10.664 to 10.709Gbps	666.51 to 669.32Mbps	
L	H			

Table 4.2.6 Receiver Data Rate select

RxRATESEL0	RxRATESEL1	Function		Note
		Serial Data rate	Parallel Data rate	
H	H	9.95328Gbps	622.08Mbps	LVTTL interface Internal 100kΩ pull up to V_{DD1}
L	L	10.3125Gbps	644.54Mbps	
H	L	10.664 to 10.709Gbps	666.51 to 669.32Mbps	
L	H			

Table 4.2.7 Digital control signals

Symbol	Function	Interface		Description	Note
Transmitter					
TxREFSEL[a]	Selects Tx 155MHz or 622MHz Reference Clock	LVTTL	L	Selects 155MHz	Internal 100 kΩ pull up to V_{DD1}
			H	Selects 622MHz	
TxRESET	Asynchronous system reset	LVTTL	L	MUX reset	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	
TxFIFORES	MUX FIFO reset	LVTTL	L	MUX FIFO reset	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	
LsENABLE	Enable/Disables Laser	LVTTL	L	Normal operation	Internal 100 kΩ pull down to GND
			H	Laser disabled	
Receiver					
RxREFSEL	Selects Rx 155MHz or 622MHz Reference Clock	LVTTL	L	Selects 155/161/166/167MHz	Internal 100 kΩ pull down to GND
			H	Selects 622/644/666/669MHz	
RxLCKREF	Locks RxPOCLK to RxREFCLK	LVTTL	L	Locks to RxREFCLK	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	
RxMUTEDOUT	Mutes the RxDOUT[0:15] to logical zero	LVTTL	L	Mutes the RxDOUT[0:15]	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	
RxMUTEPOCLK	Mutes the RxPOCLK to logical zero	LVTTL	L	Mutes the RxPOCLK	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	
RxMUTEMCLK	Mutes the RxMCLK to logical zero	LVTTL	L	Mutes the RxMCLK	Internal 100 kΩ pull up to V_{DD1}
			H	Normal operation	

a. *TxREFSEL* is available for multi-rate type, OAT1041x-V5-C-yy.

Table 4.2.8 Alarms

Symbol	Function	Interface		Description	Note
Transmitter					
TxLOCKERR	Loss of TxPLL lock	LVTTL	L	Alarm active	
			H	Normal operation	
TxFIFOERR	MUX FIFO error	LVTTL	L	Alarm active	
			H	Normal operation	
LsBIASALM	Laser bias out of range	LVTTL	L	Alarm active	Ib> 120mA (typ.)
			H	Normal operation	
LsPOWALM	Laser output power out of range	LVTTL	L	Alarm active	Output power degrades 3dB below the Po (BOL)
			H	Normal operation	
Receiver					
RxLOCKERR	Loss of RxPLL lock	LVTTL	L	Alarm active	
			H	Normal operation	
RxPOWALM	Loss of receiver average power alarm	LVTTL	L	Alarm active	Pin<-19dBm (typ.)
			H	Normal operation	

Table 4.2.9 Monitor signals

Symbol	Function	Min.	Typ.	Max.	Unit
Transmitter					
LsPOWMON	Normalized Laser power monitor voltage BOL	0.44	0.5	0.56	V
LsBIASMON	Laser bias monitor voltage slope	17.8	20	22.5	mV/mA
Receiver					
RxPOWMON	Input optical power monitor voltage slope	0.8		1.26	V/mW

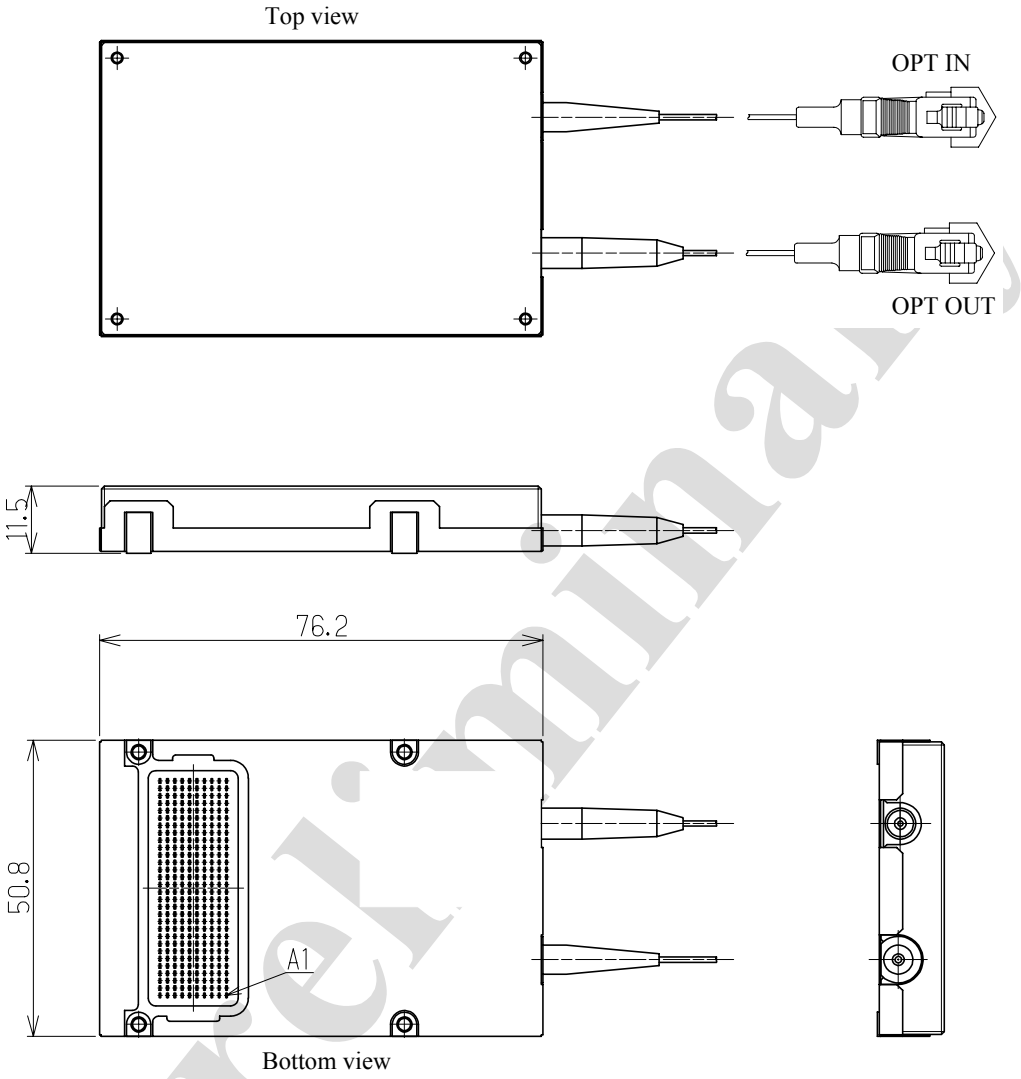
Table 4.2.10 LVDS interface

	Symbol	Min	Typ	Max	Unit
Single-ended Input Swing		100	—	—	mVp-p
Common mode input voltage		850	—	2200	mV
Input voltage range		800	—	2400	mV
Input Differential impedance		80	100	120	Ω
Single-ended Output Swing		250	—	400	mVp-p
Common mode output voltage		1100	1200	1300	mV

Table 4.2.11 LVTTL interface

	Symbol	Min	Typ	Max	Unit
Input High voltage	V_{IH}	2.0	—	V_{DD1}	V
Input Low voltage	V_{IL}	GND	—	0.6	V
Output High voltage	V_{OH}	2.4	—	V_{DD1}	V
Output Low voltage	V_{OL}	GND	—	0.4	V

5. Mechanical Information



The back side of the transceiver is recess area without mechanical bolt holes.

Users can use this domain as trace area on users PCB.

Note: Pigtail fiber length have to be specified between OKI and Users.

Figure 5 Package Outline(Units:mm)

Table 5 Connector

Optical	SC/PC type standard Other connectors are available@FC,LC,MU
Electrical	300pin BERG MegArray@84501-10X

6. Connector Pin Assignment

Table 6 Pin Assignments

	K	J	H	G	F	E	D	C	B	A
1	NUC	NUC	GND	RxDout12P	+1.8V	RxDout8P	GND	RxDout4P	GND	RxDout0P
2	NUC	NUC	GND	RxDout12N	+1.8V	RxDout8N	GND	RxDout4N	GND	RxDout0N
3	RxRATESEL0	RxRATESEL1	NUC	GND	RxPOWMON	GND	NUC	GND	NUC	GND
4	+3.3V	NUC	GND	RxDout13P	+3.3V	RxDout9P	GND	RxDout5P	GND	RxDout1P
5	+3.3V	NUC	GND	RxDout13N	+3.3V	RxDout9N	GND	RxDout5N	GND	RxDout1N
6	NUC	NUC	NUC	GND	RxPOWALM	GND	NUC	GND	RxMUTE Dout	GND
7	+3.3V	NUC	GND	RxDout14P	+3.3V	RxDout10P	GND	RxDout6P	GND	RxDout2P
8	+3.3V	NUC	GND	RxDout14N	+3.3V	RxDout10N	GND	RxDout6N	GND	RxDout2N
9	RxMUTEPOCLK	NUC	NUC	GND	NUC	GND	NUC	GND	RxLCKREF	GND
10	-5.2V	NUC	GND	RxDout15P	-5.2V	RxDout11P	GND	RxDout7P	GND	RxDout3P
11	-5.2V	NUC	GND	RxDout15N	-5.2V	RxDout11N	GND	RxDout7N	GND	RxDout3N
12	RxMUTEMCLK	NUC	NUC	GND	NUC	GND	NUC	GND	NUC	GND
13	-5.2V	NUC	GND	NUC	-5.2V	RxPOCLKP	GND	RxMCLKP	GND	RxREFCLKP
14	-5.2V	NUC	GND	NUC	-5.2V	RxPOCLKN	GND	RxMCLKN	GND	RxREFCLKN
15	I2CCLOCK	NUC	NUC	GND	RxREFSEL	GND	NUC	GND	RxLOCKERR	GND
16	NUC	NUC	GND	TxDin12P	+1.8V	TxDin8P	GND	TxDin4P	GND	TxDin0P
17	NUC	NUC	GND	TxDin12N	+1.8V	TxDin8N	GND	TxDin4N	GND	TxDin0N
18	I2CDATA	NUC	NUC	GND	LsBIASMON	GND	LsPOWMON	GND	NUC	GND
19	+3.3V	NUC	GND	TxDin13P	+3.3V	TxDin9P	GND	TxDin5P	GND	TxDin1P
20	+3.3V	NUC	GND	TxDin13N	+3.3V	TxDin9N	GND	TxDin5N	GND	TxDin1N
21	TxRATESEL0	TxRATESEL1	NUC	GND	LsENABLE	GND	NUC	GND	NUC	GND
22	+3.3V	NUC	GND	TxDin14P	+3.3V	TxDin10P	GND	TxDin6P	GND	TxDin2P
23	+3.3V	NUC	GND	TxDin14N	+3.3V	TxDin10N	GND	TxDin6N	GND	TxDin2N
24	TxRESET	NUC	NUC	GND	LsBIASALM	GND	NUC	GND	NUC	GND
25	-5.2V	NUC	GND	TxDin15P	-5.2V	TxDin11P	GND	TxDin7P	GND	TxDin3P
26	-5.2V	NUC	GND	TxDin15N	-5.2V	TxDin11N	GND	TxDin7N	GND	TxDin3N
27	TxFIFORES	NUC	NUC	GND	NUC	GND	NUC	GND	NUC	GND
28	-5.2V	NUC	GND	TxPICLKP	-5.2V	TxPCLKP	GND	TxMCLKP	GND	TxREFCLKP
29	-5.2V	NUC	GND	TxPICLKN	-5.2V	TxPCLKN	GND	TxMCLKN	GND	TxREFCLKN
30	TxFIFOERR	NUC	NUC	GND	*TxREFSEL*	GND	LsPOWALM	GND	TxLOCKERR	GND

NUC: No User Connect
Italics: *TxREFSEL* is available for multi-rate type, OAT1041x-V5-C-yy.

7. I2C diagnostic monitor (Optional function)

Memory access to the OAT1041 is through the I2C interface.The slave address defaults to A2h.The memory within the OAT1041 is 128 bytes.The following tables detail the memory contents. All conversions are updated every 13ms (nominal) or 20ms (max) in rotation.

Table 7 memory map

Table	00h-7Fh (128bytes)							
Address	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
00h	Reserved							
…								
…								
58h								
60h	–	–	–	–	LsBias MSB	LsBias LSB	LsPow MSB	LsPow LSB
68h	RxPow MSB	RxPow LSB	–	–	–	–	–	–
70h	–	–	–	–	–	–	–	–
78h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Laser Bias Current Monitor : LsBias MSB(64h), LsBias LSB(65h)

These bytes contain the MSB (64h) and the LSB (65h) of the measured the laser bias current. This Reads as an signed 16-bit quantity at 19.073uA LSB,with a maximum range of 125mA.The lower four bits should be ignored.

Normalized Laser Power Monitor : LsPow MSB(66h), LsPow LSB(67h)

These bytes contain the MSB (66h) and the LSB (67h) of the measured the normalized laser output power. This Reads as an signed 16-bit quantity at 0.000038147 LSB,with a maximum range of 2.5.The Normalized Laser Power Monitor (BOL) is typ. 0.5.The lower four bits should be ignored.

Received Average Optical Power Monitor : RxPow MSB(68h), RxPow LSB(69h)

These bytes contain the MSB (66h) and the LSB (67h) of the measured the average received optical power. This Reads as an signed 16-bit quantity at 38.147uW LSB,with a maximum range of 2.5mW.The lower four bits should be ignored.

8. Precautions for handling

The circuits of these modules operate at very small signal. In order to avoid the degradation of the optical sensitivity due to external noise, the bottom pattern of these modules on the PCB should be ground pattern with low impedance.

Do not mount/pattern device/circuits which generate high frequency noise close to the module.

In order to operate the module stable against the power noise, install the power supply noise reduction circuits.

The impedance between the power and ground pattern of the power circuit should be as low as possible. The elements around the module should be mounted close to the pins of the module.

If an optical power exceeding the absolute maximum ratings is fed to the module, the optical receiver may be damaged. Set the optical input power appropriately when in use of these modules.

9. Laser Safety

All version of transceiver are Class 1 Laser products FDA complies with 21 CFR 1040.10 and 1040.11 requirements. Also, all versions are Class 1 Laser products pre IEC 825-1.

10. Ordering Information

OAT1041x-V5-z-yy -[ ]

Note: In z = A, B, D, E, " -[ ] " is added when 150MHz is specified to be TxREFCLK frequency.

Table 9 Ordering Information

x		**z**		**yy**		**-[ ]**	
Optical connector		Bit rate(Gbps)		Fiber length		TxREFCLK frequency	
S	SC	A	9.95	10	1m	blank	600MHz
F	FC	B	10.3	05	0.5m	-L	150MHz
L	LC	C	9.95/10.3/10.6/10.7				
M	MU	D	10.7				
		E	10.6				