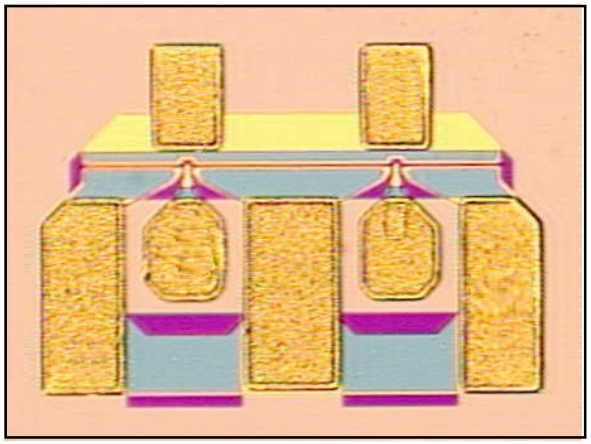
300um Discrete pHEMT TGF4350-EPU

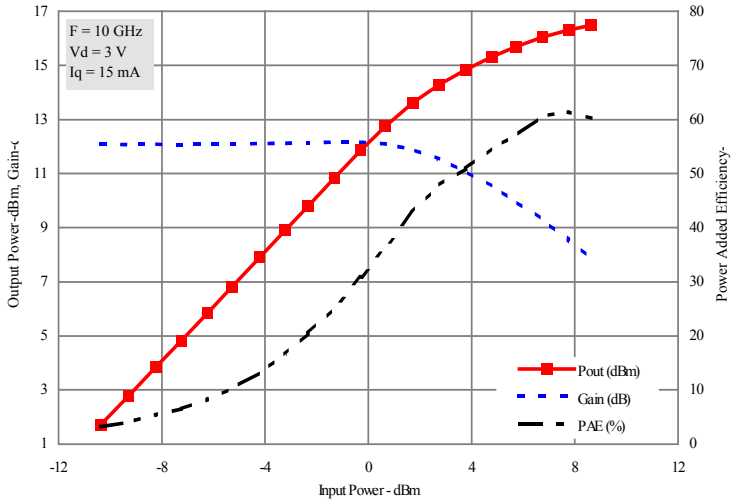


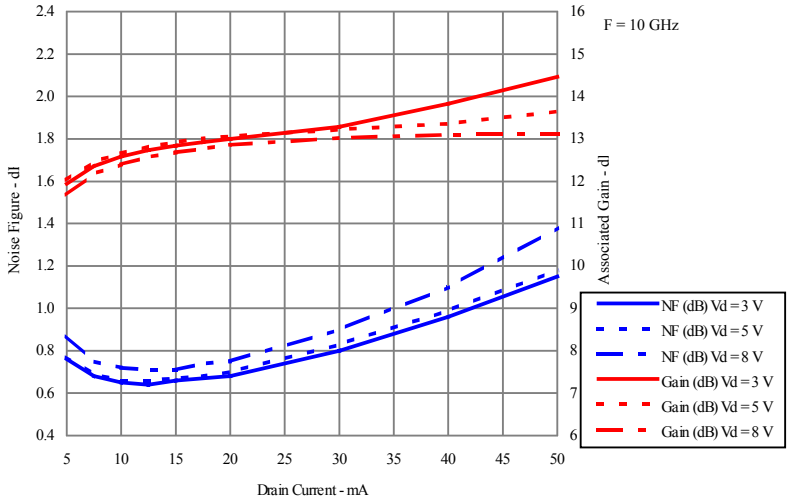
Key Features and Performance

- 0.25um pHEMT Technology
- DC 22 GHz Frequency Range
- 1.2 dB NF, 14.5 dB Associated Gain at 10 GHz, 3V Operation
- Floating Source Configuration
- Chip Dimensions 0.5080 mm x 0.4064 mm

Primary Applications

- Low Noise amplifiers





Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications subject to change without notice

Electrical Characteristics

RECOMMENDED MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V^+	Positive Supply Voltage	7 V	
I^+	Positive Supply Current	.085A	3/
P_D	Power Dissipation	0.6 W	
P_{IN}	Input Continuous Wave Power	20 dBm	
T_{CH}	Operating Channel Temperature	150 °C	1/, 2/
T_M	Mounting Temperature (30 seconds)	320 °C	
T_{STG}	Storage Temperature	-65 °C to 150 °C	

1/ These ratings apply to individual FET

2/ Junction operating temperature will directly affect the device mean time to failure (MTTF). For maximum life it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ Nominal value of Idss

DC PROBE TESTS
(T_A = 25 °C ± 5°C)

Symbol	Parameter	Minimum	Maximum	Value
Idss	Saturated Drain Current (info only)	30	141	mA
V_{P1-5}	Pinch-off Voltage	-1.5	-0.5	V
BV_{GS1}	Breakdown Voltage gate-source	-30	-8	V
BV_{GD1-5}	Breakdown Voltage gate-drain	-30	-8	V

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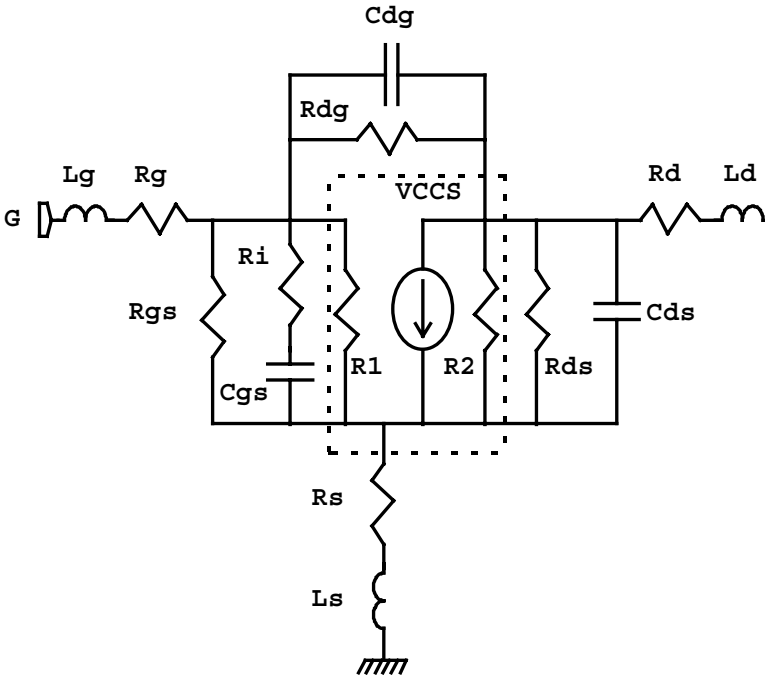
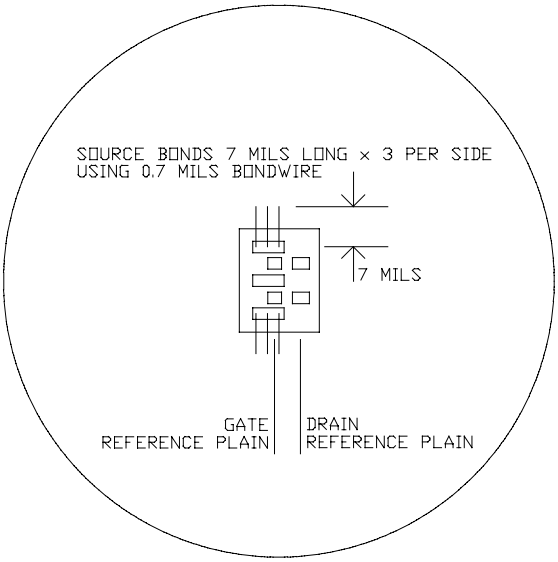
FET Elements

Lg = 0.040 nH
Rg = 0.525 Ohms
Rgs = 14500 Ohms
Ri = 4.924 Ohms
Cgs = 0.364 pF
Cdg = 0.042 pF
Rdg = 146000 Ohms
Rs = 0.300 Ohms
Ls = 0.041 nH
Rds = 253.858 Ohms
Cds = 0.080 pF
Rd = 0.833 Ohms
Ld = 0.028 nH
VCCS Parameters
M = 0.091 S
A = 0
R1 = 1E19 Ohms
R2 = 1E19 Ohms
F = 0
T = 4.000 pS

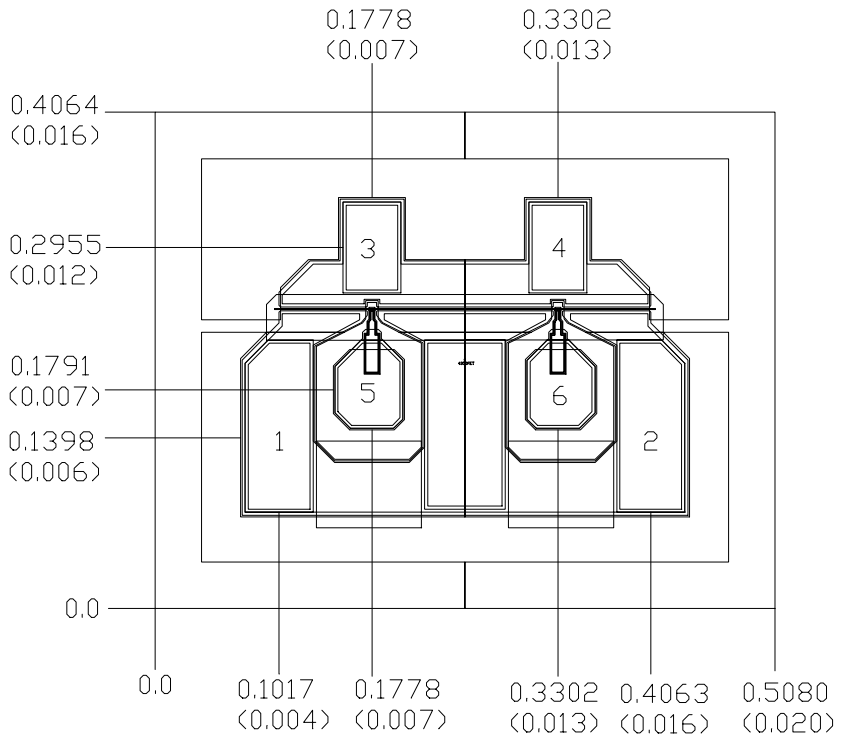


TGA4350EPU pHEMT Model (Vds = 3.0 V and 15mA at T = 25°C)

Device is mounted on a 20 mil high ledge. Source inductance includes that of source bondwires and ledge



Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.1016 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
chip size tolerance: +/- 0.051 (0.002)

Bond Pad #1,#2 (Source)	0.051 x 0.136 (0.002 x 0.005)
Bond Pad #3,#4 (Drain)	0.042 x 0.069 (0.002 x 0.003)
Bond Pad #5,#6 (Gate)	0.051 x 0.067 (0.002 x 0.003)

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Process and Assembly Notes

This device should be attached using conductive epoxy only. Contact factory for additional details as required.

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C