



---

## Features

- 128K x 36 or 256K x 18 Organizations
- CMOS Technology
- Synchronous Flow-Thru Mode Of Operation with Self-Timed Late Write
- Dual Differential Input and Output Clocks
- +3.3V Power Supply, 1.5V  $V_{DDQ}$ ,  $V_{REF}$  & Ground
- HSTL Input and Output levels
- Registered Addresses, Write Enables, Sync Select and Data Ins
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

---

## Description

The IBM041840QLAD and IBM043640QLAD 4Mb SRAMs are Synchronous Flow-Thru Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 4.5ns cycle time. Dual differential K clocks are used to initiate the read/write operation, and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered internally. Differential

clocks C and  $\bar{C}$  are used to control the Output Data hold time by allowing output data to change after the rising edge of the C clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a +3.3V power supply, output power supply compatible with 1.5V, and is also compatible with HSTL I/O interfaces.

### x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	SA5	SA7	NC	SA16	SA14	V <sub>DDQ</sub>
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V <sub>DD</sub>	SA10	SA15	NC
D	DQc18	DQc19	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQb10	DQb9
E	DQc20	DQc21	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	DQb12	DQb11
F	V <sub>DDQ</sub>	DQc22	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQb13	V <sub>DDQ</sub>
G	DQc23	DQc24	$\overline{SBWc}$	$\overline{C}$	$\overline{SBWb}$	DQb15	DQb14
H	DQc25	DQc26	V <sub>SS</sub>	C	V <sub>SS</sub>	DQb17	DQb16
J	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd34	DQd35	V <sub>SS</sub>	K	V <sub>SS</sub>	DQa8	DQa7
L	DQd32	DQd33	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQa6	DQa5
M	V <sub>DDQ</sub>	DQd31	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	DQa4	V <sub>DDQ</sub>
N	DQd29	DQd30	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQa3	DQa2
P	DQd27	DQd28	V <sub>SS</sub>	SA1	V <sub>SS</sub>	DQa1	DQa0
R	NC	SA4	M1*	V <sub>DD</sub>	M2*	SA12	NC
T	NC	NC	SA3	SA2	SA13	NC	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Note:** \* M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V<sub>DD</sub> and V<sub>DD</sub>, respectively.

### x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	SA5	SA7	NC	SA16	SA14	V <sub>DDQ</sub>
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V <sub>DD</sub>	SA10	SA15	NC
D	DQb9	NC	V <sub>SS</sub>	ZQ	V <sub>SS</sub>	DQa1	NC
E	NC	DQb12	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	NC	DQa2
F	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQa4	V <sub>DDQ</sub>
G	NC	DQb15	$\overline{SBWb}$	$\overline{C}$	V <sub>SS</sub>	NC	DQa5
H	DQb16	NC	V <sub>SS</sub>	C	V <sub>SS</sub>	DQa8	NC
J	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>REF</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
K	NC	DQb17	V <sub>SS</sub>	K	V <sub>SS</sub>	NC	DQa7
L	DQb14	NC	V <sub>SS</sub>	$\overline{K}$	$\overline{SBWa}$	DQa6	NC
M	V <sub>DDQ</sub>	DQb13	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
N	DQb11	NC	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQa3	NC
P	NC	DQb10	V <sub>SS</sub>	SA1	V <sub>SS</sub>	NC	DQa0
R	NC	SA4	M1	V <sub>DD</sub>	M2	SA13	NC
T	NC	SA2	SA3	NC	SA17	SA12	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

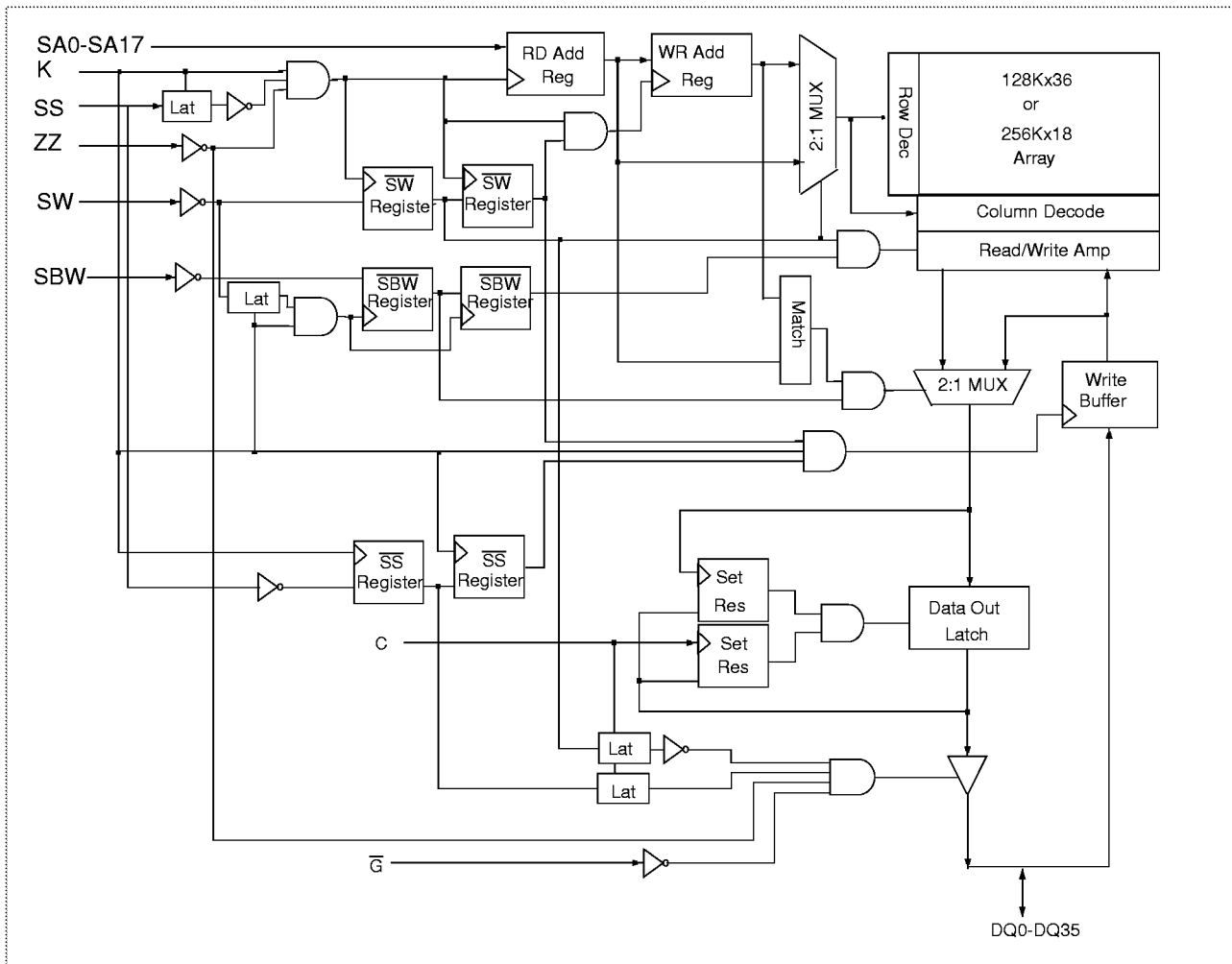
**Note:** \* M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V<sub>DD</sub> and V<sub>DD</sub> respectively.



### Pin Description

SA0-SA17	Address Input	$\bar{G}$	Asynchronous Output Enable
DQ0-DQ35	Data I/O	$\bar{SS}$	Synchronous Select
K, $\bar{K}$	Differential Input Register Clocks	M1, M2	Clock Mode Inputs - Selects Dual Clock Operation.
C, $\bar{C}$	Differential Output Data Hold Control Clocks	$V_{REF(2)}$	GTL/HSTL Input Reference Voltage
$\bar{SW}$	Write Enable, Global	$V_{DD}$	Power Supply (+3.3V)
$\bar{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	$V_{SS}$	Ground
$\bar{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	$V_{DDQ}$	Output Power Supply
$\bar{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	ZZ	Asynchronous Sleep Mode
$\bar{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZQ	Output Driver Impedance Control
TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTL levels)	NC	No Connect
TDO	IEEE 1149.1 Test Output (LVTTL level)		

### Block Diagram



## SRAM Features

### Late Write

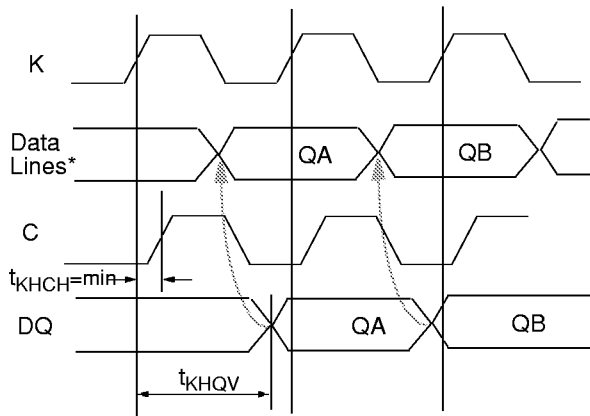
Late Write function allows for write data to be registered one cycle after addresses and controls. This feature will alleviate SRAM data bus contention going from a Read to Write cycle by eliminating one dead cycle. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In the case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with address and data in the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

### Dual Clock Operation

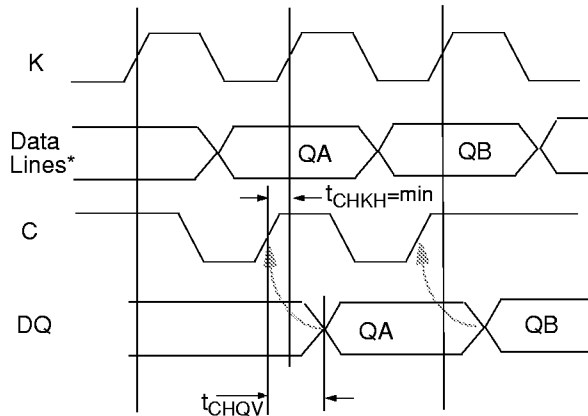
In Dual Clock Operation, the K Clocks are used to register all synchronous inputs and start the SRAM operation. The C Clocks are used to control the output data timings. During Write ( $\overline{SW}=L$ ) or Deselect ( $\overline{SS}=H$ ) operations, the rising edge of C Clock triggers the time to High-Z. During Read operations the location of the rising edge of the C Clock will determine the output data valid placement by allowing SRAM output data to flow through after the rising edge. When the rising edge of the C Clock occurs early in a Read cycle (e.g.  $t_{KHCH} = \text{Min.}$ ), data from the SRAM will become available at a  $t_{KHQV}$  time, as it would in a Flow-Through Read implementation (see Dual Clock Diagram #1 below). As the C Clock rising edge moves away from  $t_{KHCH} = \text{Min.}$ , towards a  $t_{CHKH} = \text{Min.}$ , of the next K Clock rising edge, the output data may become "gated" by the C Clock (see Dual Clock Diagram #2 below). The SRAM access time will then become referenced to the C Clock (i.e.  $t_{CHQV}$ ). This feature allows SRAM users to fully control the output data hold time over voltage, temperature and process variations, and provide minimum output data latency.

### Dual Clock Diagrams

**Dual Clock Diagram #1:** Output data becomes available as a result of internal data lines flowing through the output latch unrestrained by the C clock.



**Dual Clock Diagram #2:** Internal data lines await at the output latch for the rising edge of C clock. The C clock enables the output latch and allows output data to become available.



\*Data Lines refer to internal data lines connecting to Data Output Latch. See Block Diagram on page 3.



## Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM supports Dual Clock Flow-Through protocols (M1 =  $V_{DD}$ , M2 =  $V_{DD}$ ). This data sheet only describes Dual Clock Flow-Through functionality. Mode control inputs must be set with power up and must not change during SRAM operation.

## Power Down Mode

Power Down Mode or "Sleep" Mode is enabled by switching asynchronous signal ZZ High. When powering the SRAM down inputs should be dropped first followed by  $V_{REF}$  then  $V_{DDQ}$ ;  $V_{DD}$  must be dropped last.  $V_{DDQ}$  can be simultaneously dropped with  $V_{DD}$ .

## Programmable Impedance/Power Up Requirements

An external resistor,  $R_Q$ , must be connected between the ZQ pin on the SRAM and  $V_{SS}$  to allow for the SRAM to adjust its output driver impedance. The value of  $R_Q$  must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of  $R_Q$  to guarantee impedance matching with a tolerance of 15% is between 175 $\Omega$  and 350 $\Omega$ . Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time towards the optimum level. The output driver has 32 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore triggering an update. The user may choose to invoke asynchronous  $\bar{G}$  updates by providing a  $\bar{G}$  setup and hold about the K Clock to guarantee the proper update. Power up requirements for the SRAM are that  $V_{DD}$  must be powered before or simultaneously with  $V_{DDQ}$  followed by  $V_{REF}$ ; inputs should be powered last.  $V_{DDQ}$  must not exceed  $V_{DD}$  by more than 0.4V during power up. In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 4 $\mu$ s of power-up time after  $V_{DD}$  reaches its operating range. To guarantee optimum output driver impedance after power up, the SRAM needs 2080 clock cycles followed by a single Low-Z to High-Z transition at the end of 2080 cycles.

## Sleep Mode Operation

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin HIGH. During sleep mode, all other inputs are ignored and outputs are brought to a High-Z state. Sleep mode current and output High Z are guaranteed after the specified sleep mode enable time. During sleep mode, the array data contents are preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Sense amp data is lost. Normal operation can be resumed by bringing ZZ low, but only after specified sleep mode recovery time.



## Ordering Information

Part Number	Organization	Speed	Leads
IBM041840QLAD-4 (Rev D)	256K x 18	6.5ns Access / 4.5ns Cycle	7 x 17 BGA
IBM041840QLAD-5 (Rev D)	256K x 18	7.0ns Access / 5ns Cycle	7 x 17 BGA
IBM041840QLAD-6 (Rev D)	256K x 18	7.5ns Access / 6ns Cycle	7 x 17 BGA
IBM043640QLAD-4 (Rev D)	128K x 36	6.5ns Access / 4.5ns Cycle	7 x 17 BGA
IBM043640QLAD-5 (Rev D)	128K x 36	7.0ns Access / 5ns Cycle	7 x 17 BGA
IBM043640QLAD-6 (Rev D)	128K x 36	7.5ns Access / 6ns Cycle	7 x 17 BGA



### Output Enable Truth Table

Operation	$\overline{G}$	DQ
Read	L	D <sub>OUT</sub> 0-35
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write ( $\overline{SW}$ =L)	X	High-Z
Deselect ( $\overline{SS}$ =H)	X	High-Z

### Clock Truth Table

K, C CLK	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWA}$	$\overline{SBWB}$	$\overline{SBWC}$	$\overline{SBWD}$	DQ (n)	DQ (n+1)	Mode
L→H	L	L	H	X	X	X	X	D <sub>OUT</sub> 0-35	X	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	High-Z	D <sub>IN</sub> 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	High-Z	D <sub>IN</sub> 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	High-Z	D <sub>IN</sub> 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	High-Z	D <sub>IN</sub> 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	High-Z	D <sub>IN</sub> 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	High-Z	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	High-Z	X	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

### Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V <sub>DD</sub>	-0.5 to 3.9	V	1
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V	1
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V	1
Operating Temperature	T <sub>J</sub>	0 to +110	°C	1
Output Power Supply Voltage	V <sub>DDQ</sub>	V <sub>DD</sub>	V	1
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PBGA Thermal Characteristics

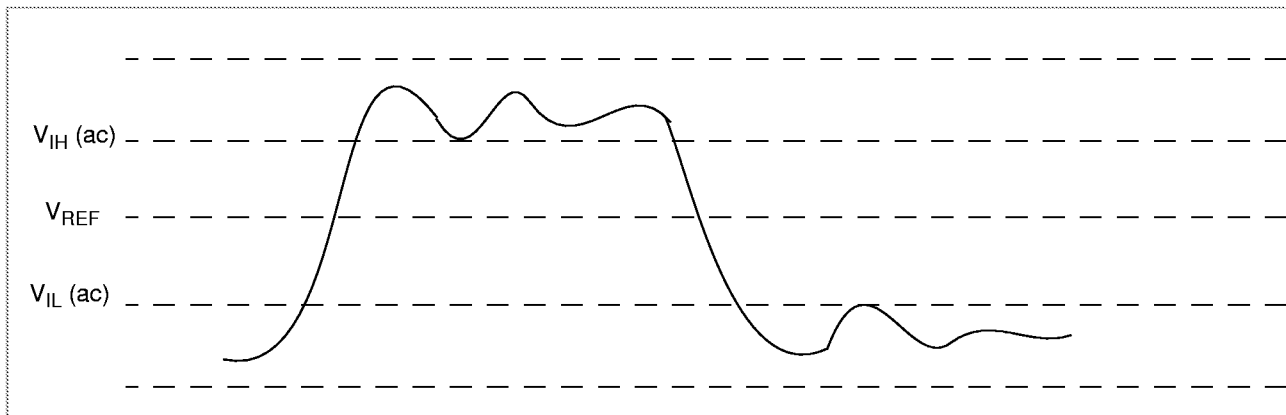
Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	R <sub>QJC</sub>	1	°C/W

## AC Input Characteristics

Item	Symbol	Min	Max	Notes
AC Input Logic High (Volts)	V <sub>IH</sub> (ac)	V <sub>REF</sub> +0.4		3
AC Input Logic Low (Volts)	V <sub>IL</sub> (ac)		V <sub>REF</sub> -0.4	3
Clock Input Differential Voltage (Volts)	V <sub>DIF</sub> (ac)	0.4		2
V <sub>REF</sub> Peak to Peak ac Voltage (Volts)	V <sub>REF</sub> (ac)		5% V <sub>REF</sub> (dc)	1

1. The peak to peak AC component superimposed on V<sub>REF</sub> may not exceed 5% of the DC component of V<sub>REF</sub>. Implies very stable signal. Sourcing from V<sub>ddq</sub> not recommended. Separate board plane recommended. Do not use noisy signal line.
2. Performance is a function on V<sub>IH</sub> and V<sub>IL</sub> levels to clock inputs.
3. See AC Input Definition figure on page 9.

## AC Input Definition





**Recommended DC Operating Conditions** ( $T_A=0$  to  $85^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{DD}$	3.135	3.3	3.465	V	1
Output Driver Supply Voltage	$V_{DDQ}$	1.4	1.5	1.6	V	1
Input High Voltage	$V_{IH}$	$V_{REF} + 0.1$	—	$V_{DDQ} + 0.3$	V	1, 2
Input Low Voltage	$V_{IL}$	-0.3	—	$V_{REF} - 0.1$	V	1, 3
Input Reference Voltage	$V_{REF}$	0.68	0.75	0.90	V	1
Clocks Signal Voltage	$V_{IN-CLK}$	-0.3	—	$V_{DDQ} + 0.3$	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF-CLK}$	0.1	—	$V_{DDQ} + 0.6$	V	1, 5
Clocks Common Mode Voltage	$V_{CM-CLK}$	0.55	—	0.90	V	1
Output Current	$I_{out}$	—	5	8	mA	

- All voltages referenced to  $V_{SS}$ . All  $V_{DD}$ ,  $V_{DDQ}$  and  $V_{SS}$  pins must be connected.
- $V_{IH}(\text{Max})\text{DC} = V_{DDQ} + 0.3$  V,  $V_{IH}(\text{Max})\text{AC} = V_{DD} + 1.5$  V (pulse width  $\leq 4.0\text{ns}$ ).
- $V_{IL}(\text{Min})\text{DC} = -0.3$  V,  $V_{IL}(\text{Min})\text{AC} = -1.5$  V (pulse width  $\leq 4.0\text{ns}$ ).
- $V_{IN-CLK}$  specifies the maximum allowable DC excursions of each differential clock (K,  $\bar{K}$ , C,  $\bar{C}$ ).
- $V_{DIF-CLK}$  specifies the minimum Clock differential voltage required for switching.

**Capacitance** ( $T_A=0$  to  $85^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	4	pF
Data I/O Capacitance (DQ0-DQ35)	$C_{OUT}$	$V_{OUT} = 0\text{V}$	5	pF

### DC Electrical Characteristics ( $T_A=0$ to $+85^\circ\text{C}$ , $V_{DD}=3.3\text{V} \pm 5\%$ )

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current- <b>x36</b> ( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $ZZ$ & $\overline{SS} = V_{IL}$ )	$I_{DD4.5}$ $I_{DD5}$ $I_{DD6}$	— — —	710 650 575	mA	1
Average Power Supply Operating Current - <b>x18</b> ( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $ZZ$ & $\overline{SS} = V_{IL}$ )	$I_{DD4.5}$ $I_{DD5}$ $I_{DD6}$	— — —	650 600 525	mA	1
Power Supply Standby Current ( $ZZ = V_{IH}$ , All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ )	$I_{SBZZ}$	—	150	mA	1
( $\overline{SS} = V_{IH}$ , $ZZ = V_{IL}$ , All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ )	$I_{SBSS}$	—	200	mA	1
Input Leakage Current, any input ( $V_{IN} = V_{SS}$ or $V_{DD}$ )	$I_{LI}$	—	+1	$\mu\text{A}$	
Output Leakage Current ( $V_{OUT} = V_{SS}$ or $V_{DD}$ , DQ in High-Z)	$I_{LO}$	—	+1	$\mu\text{A}$	
Output "High" Level Voltage ( $I_{OH} = -6\text{mA}$ @ $V_{DDQ}/2 + 0.3$ )	$V_{OH}$	$V_{DDQ} - 4$	$V_{DDQ}$	V	2
Output "Low" Level Voltage ( $I_{OL} = +6\text{mA}$ @ $V_{DDQ}/2 - 0.3$ )	$V_{OL}$	$V_{SS}$	$V_{SS} + 4$	V	2

1.  $I_{OUT}$  = Chip Output Current.  $I_{DD4.5}$  refers to operating current at 4.5ns cycle time, for example  
 2. Minimum Impedance Output Driver.

### Programmable Impedance Output Driver DC Electrical Characteristics ( $T_A=0$ to $+85^\circ\text{C}$ , $V_{DD}=3.3\text{V} \pm 5\%$ )

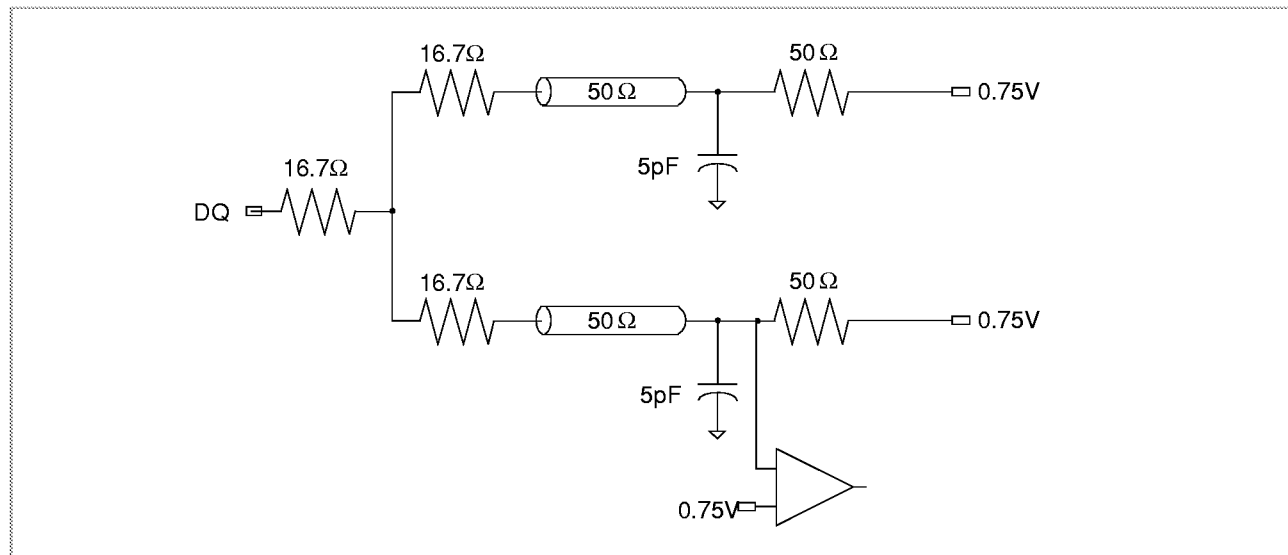
Parameter	Symbol	Min.	Max.	Units	Notes
Output "High" Level Voltage	$V_{OH}$	$V_{DDQ}/2$	$V_{DDQ}$	V	1
Output "Low" Level Voltage	$V_{OL}$	$V_{SS}$	$V_{DDQ}/2$	V	2

1.  $I_{OH} = (V_{DDQ}/2) / (RQ/5)$  15% @  $V_{OH} = V_{DDQ}/2$  For:  $150\Omega \leq RQ \leq 350\Omega$ .  
 2.  $I_{OL} = (V_{DDQ}/2) / (RQ/5)$  15% @  $V_{OL} = V_{DDQ}/2$  For:  $150\Omega \leq RQ \leq 350\Omega$ .

**AC Test Conditions** ( $T_A=0$  to  $85^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ ,  $V_{DDQ} = 1.5\text{V}$ )

Parameter	Symbol	Conditions	Units	Notes
Input High Level	$V_{IH}$	1.25	V	
Input Low Level	$V_{IL}$	0.25	V	
Input Reference Voltage	$V_{REF}$	0.75	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.75	V	
Clocks Common Mode Voltage	$V_{CM-CLK}$	0.75	V	
Input Rise Time	$T_R$	0.5	ns	
Input Fall Time	$T_F$	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.75	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1

1. See AC Test Loading figure on page 11.

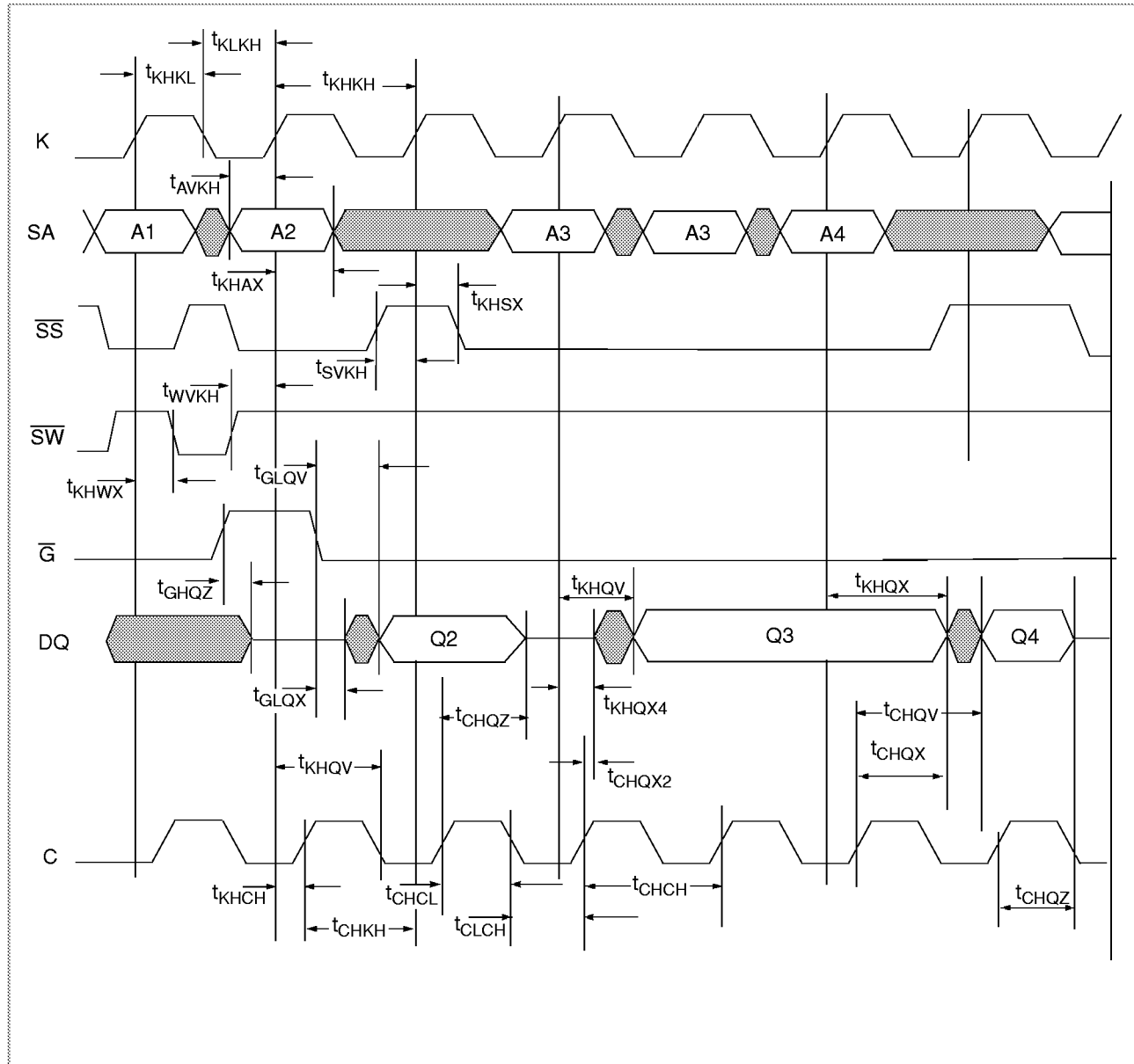
**AC Test Loading**


**AC Characteristics** ( $T_A=0$  to  $85^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ ,  $V_{DDQ}=1.5\text{V}$ ,  $V_{REF}=0.75\text{V}$ )

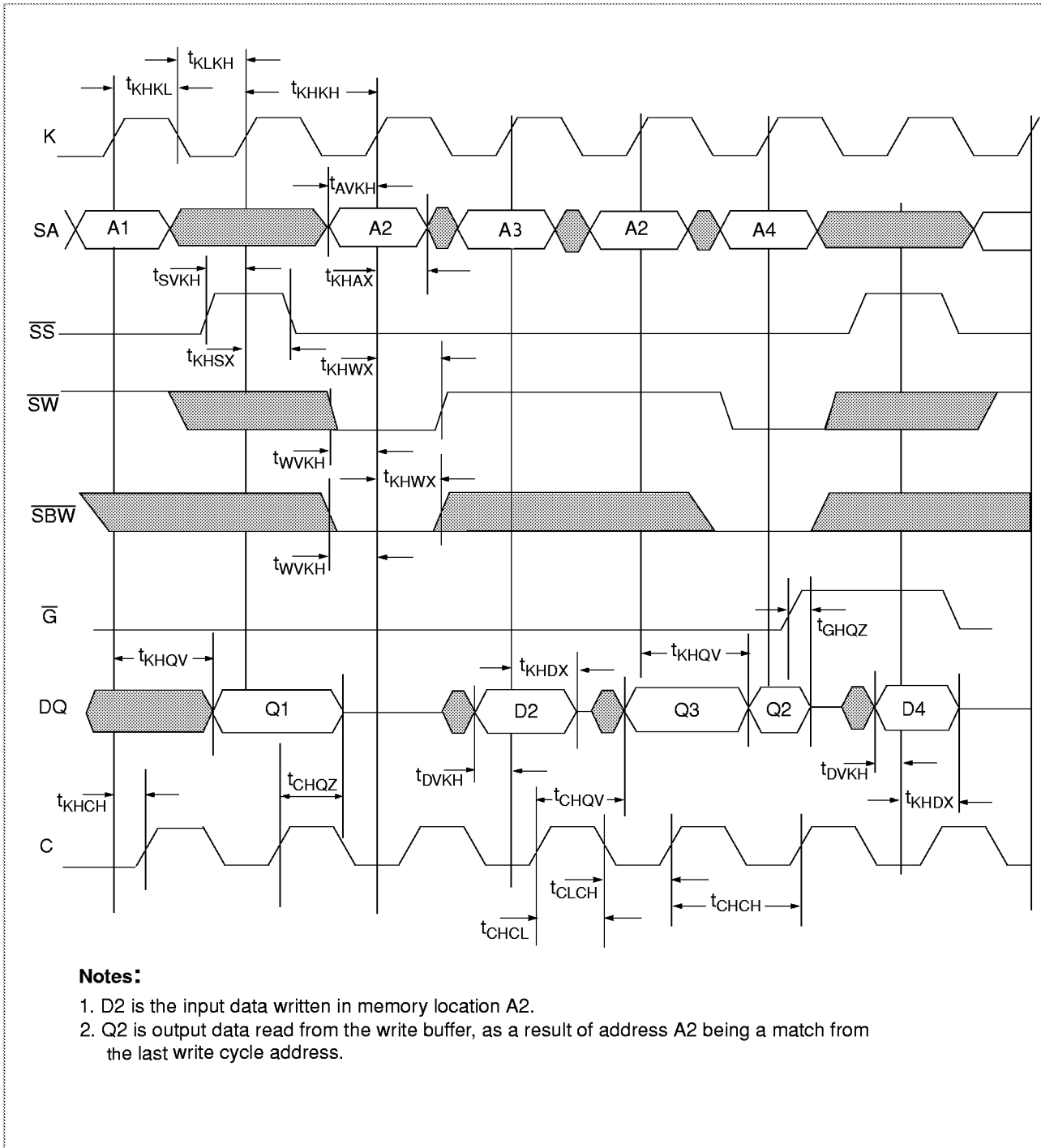
Parameter	Symbol	-4		-5		-6		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
K Clock Cycle Time	$t_{KHKH}$	4.5	—	5.0	—	6.0	—	ns	
K Clock High Pulse Width	$t_{KHKL}$	1.5	—	1.5	—	1.5	—	ns	
K Clock Low Pulse Width	$t_{KLKH}$	1.5	—	1.5	—	1.5	—	ns	
C Clock Cycle Time	$t_{CHCH}$	$t_{KHKH}$	—	$t_{KHKH}$	—	$t_{KHKH}$	—	ns	
C Clock High Pulse Width	$t_{CHCL}$	1.5	—	1.5	—	1.5	—	ns	
C Clock Low Pulse Width	$t_{CLCH}$	1.5	—	1.5	—	1.5	—	ns	
K to C Clock Delay	$t_{KHCH}$	1.5	—	1.5	—	1.5	—	ns	
C to K Clock Delay	$t_{CHKH}$	0.8	—	1.0	—	1.0	—	ns	
K Clock to Output Valid	$t_{KHQV}$	—	6.5	—	7.0	—	7.5	ns	1
Data Out Hold Time from K Clock	$t_{KHQX}$	2.0	—	2.5	—	3.0	—	ns	1, 2, 4
K Clock High to Output Active	$t_{KHQX4}$	2.5	—	3.0	—	3.5	—	ns	1, 2, 4
C Clock to Output Valid	$t_{CHQV}$	—	2.5	—	3.0	—	3.0	ns	1, 5
Data Out Hold Time from C clock	$t_{CHQX}$	0.5	—	0.5	—	0.5	—	ns	1, 2, 5
C Clock High to Output High-Z	$t_{CHQZ}$	—	2.5	—	3.0	—	3.0	ns	1, 2
C Clock High to Output Active	$t_{CHQX2}$	0.5	—	0.5	—	0.5	—	ns	1, 2, 5
Address Setup Time	$t_{AVKH}$	0.5	—	0.5	—	0.5	—	ns	6
Address Hold Time	$t_{KHAX}$	1.0	—	1.0	—	1.0	—	ns	6
Synchronous Select Setup Time	$t_{SVKH}$	0.5	—	0.5	—	0.5	—	ns	6
Synchronous Select Hold Time	$t_{KHSX}$	1.0	—	1.0	—	1.0	—	ns	6
Write Enables Setup Time	$t_{WVKH}$	0.5	—	0.5	—	0.5	—	ns	6
Write Enables Hold Time	$t_{KHWX}$	1.0	—	1.0	—	1.0	—	ns	6
Data In Setup Time	$t_{DVKH}$	0.5	—	0.5	—	0.5	—	ns	6
Data In Hold Time	$t_{KHDX}$	1.0	—	1.0	—	1.0	—	ns	6
Output Enable to Output Valid	$t_{GLQV}$	—	2.4	—	2.5	—	3.0	ns	1
Output Enable to Low-Z	$t_{GLQX}$	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable to High-Z	$t_{GHQZ}$	—	2.4	—	2.5	—	3.0	ns	1, 2
Output Enable Set-up Time	$t_{GHKH}$	0.5	—	0.5	—	0.5	—	ns	1, 3
Output Enable Hold Time	$t_{KHGX}$	1.5	—	1.5	—	1.5	—	ns	1, 3
Sleep Mode Recovery Time	$t_{ZZR}$	4.5	—	5	—	6	—	ns	
Sleep Mode Enable Time	$t_{ZZE}$	—	4.5	—	5	—	6	ns	

1. See AC Test Loading figure on page 11.
2. Verified by design and tested without guardband.
3. Output Driver Impedance update specifications for  $\bar{G}$  induced updates. Write and Deselect cycles will also induce Output Driver updates during High-Z.
4.  $t_{KHQX}$  and  $t_{KHQX4}$  are used in instances where  $t_{KHCH} = \text{Min.}$  and, therefore, the C Clock may not gate the output data.
5.  $t_{CHQV}$ ,  $t_{CHQX}$  and  $t_{CHQX2}$  are used in instances where the output data is gated by the C Clock.
6. In use conditions  $V_{IH}$ ,  $V_{IL}$ ,  $T_{rise}$ ,  $T_{fall}$  of inputs must be within 20% of  $V_{IH}$ ,  $V_{IL}$ ,  $T_{rise}$ ,  $T_{fall}$  of Clocks.

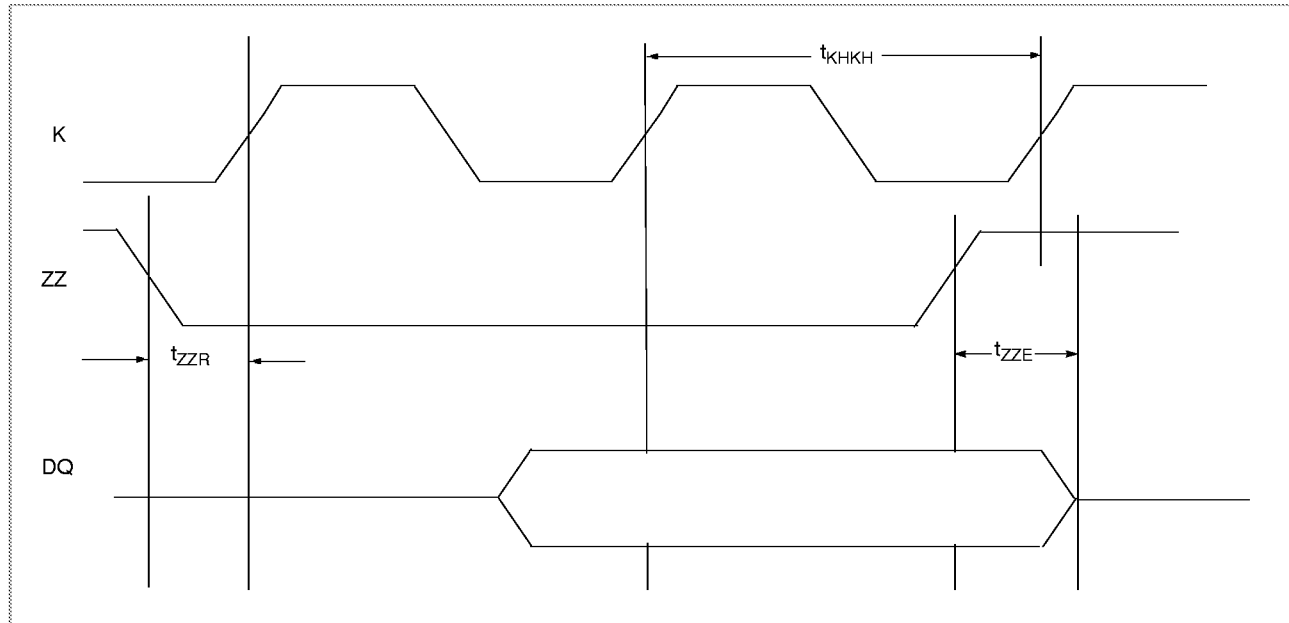
### Timing Diagram (Read and Deselect Cycles)



### Timing Diagram (Read Followed by Write)



### Timing Diagram (Sleep Mode)



## IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAMs contain a TAP controller, Instruction register, Boundary Scan register, Bypass register, and ID register.

The TAP controller has a standard 16-state state machine that resets internally upon power-up, therefore, TRST signal is not required.

### Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

**Caution:** TCK, TMS, TDI inputs must be biased down, even if JTAG is not used. TCK tied off will not allow any data to be clocked in, however.

### JTAG Recommended DC Operating Conditions (T<sub>A</sub>=0 to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V <sub>IH1</sub>	2.2	—	V <sub>DD</sub> +0.3	V	1
JTAG Input Low Voltage	V <sub>IL1</sub>	-0.3	—	0.8	V	1
JTAG Output High Level	V <sub>OH1</sub>	2.4	—	—	V	1, 2
JTAG Output Low Level	V <sub>OL1</sub>	—	—	0.4	V	1, 3

1. All JTAG Inputs and Outputs are LVTTTL Compatible only.  
 2. I<sub>OH1</sub> = -8mA at 2.4V.  
 3. I<sub>OL1</sub> = +8mA at 0.4V.

### JTAG AC Test Conditions (T<sub>A</sub>=0 to 85°C, V<sub>DD</sub>=3.3V ±5%)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V <sub>IH1</sub>	3.0	V	
Input Pulse Low Level	V <sub>IL1</sub>	0.0	V	
Input Rise Time	T <sub>R1</sub>	2.0	ns	
Input Fall Time	T <sub>F1</sub>	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

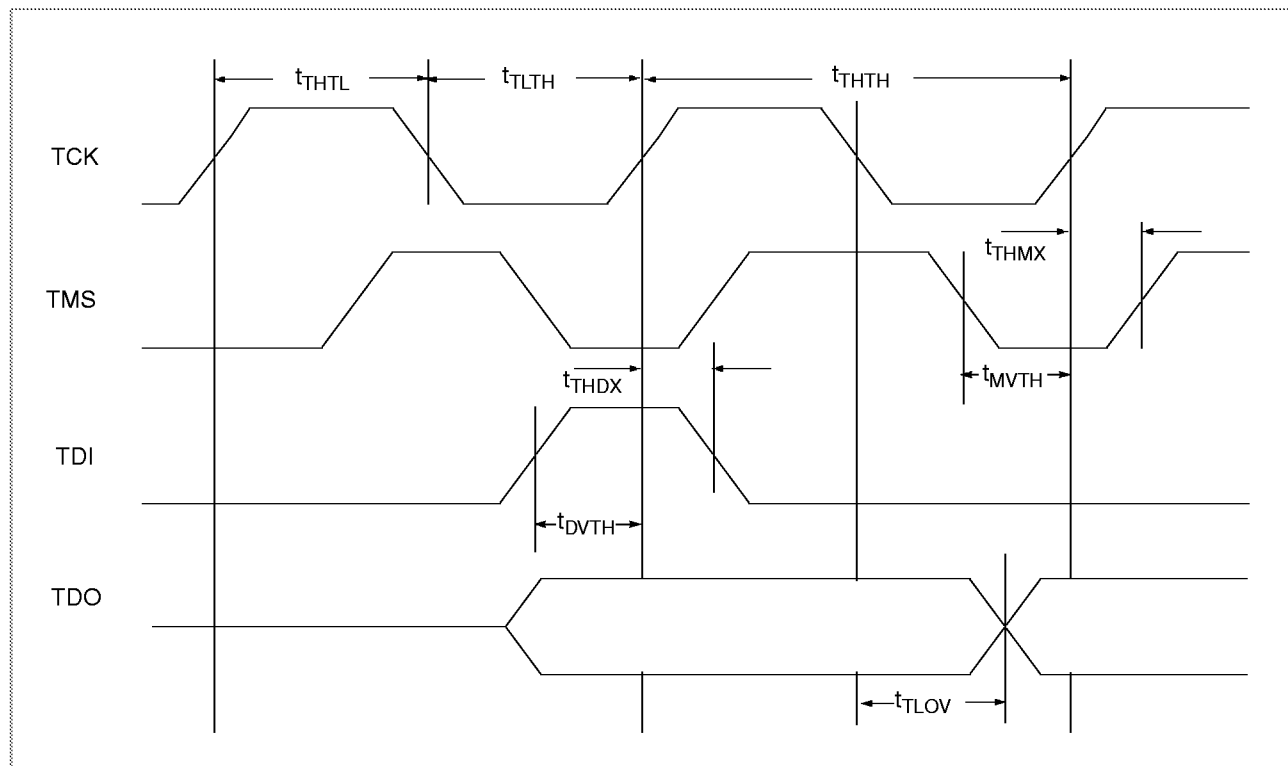
1. See AC Test Loading figure on page 11.



**JTAG AC Characteristics** ( $T_A=0$  to  $85^\circ\text{C}$ ,  $V_{DD}=3.3 \pm 5\%$ )

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	$t_{THTH}$	20	—	ns	
TCK High Pulse Width	$t_{THTL}$	7	—	ns	
TCK Low Pulse Width	$t_{TLTH}$	7	—	ns	
TMS Setup	$t_{MVTH}$	4	—	ns	
TMS Hold	$t_{THMX}$	4	—	ns	
TDI Setup	$t_{DVTH}$	4	—	ns	
TDI Hold	$t_{THDX}$	4	—	ns	
TCK Low to Valid Data	$t_{TLOV}$	—	7	ns	1

1. See AC Test Loading figure on page 11.

**JTAG Timing Diagram**




### Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

- \* The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs Depending on x18 or x36 Configuration
  - 17 bits for SA0 - SA16 for x36, 18 bits for SA0 - SA17 for x18
  - 4 bits for  $\overline{SBW}a$  -  $\overline{SBW}d$  in x36, 2 bits for  $\overline{SBW}a$  and  $\overline{SBW}b$  in x18
  - 11 bits for K,  $\overline{K}$ , C,  $\overline{C}$ , ZQ,  $\overline{SS}$ ,  $\overline{G}$ , SW, ZZ, M1 and M2
  - 2 bits for Place Holders

\* K,  $\overline{K}$ , C,  $\overline{C}$  clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

### ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit (0)
256K x 18	0001	011 100 1011	001000	000 101 001 00	1
128K x 36	0001	011 010 1100	001000	000 101 001 00	1

### Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1,5
001	IDCODE	2
010	SAMPLE-Z	1,5
011	PRIVATE	
100	SAMPLE	4,5
101	PRIVATE	
110	PRIVATE	
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to VSS when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. SRAM must not be in Sleep mode (ZZ = H) when SAMPLE-Z or SAMPLE instructions are invoked.

### List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d



**Boundary Scan Order (x36) (PH =Place Holder)**

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ13	6F	49	DQ26	2H
2	SA1	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ12	6E	51	$\overline{SBWc}$	3G
4	SA12	6R	28	DQ9	7D	52	ZQ	4D
5	SA13	5T	29	DQ10	6D	53	SS	4E
6	ZZ	7T	30	SA14	6A	54	C	4G
7	DQ1	6P	31	SA15	6C	55	C	4H
8	DQ0	7P	32	SA10	5C	56	SW	4M
9	DQ3	6N	33	SA16	5A	57	$\overline{SBWd}$	3L
10	DQ2	7N	34	PH <sup>1</sup>	6B	58	DQ34	1K
11	DQ4	6M	35	SA11	5B	59	DQ35	2K
12	DQ6	6L	36	SA8	3B	60	DQ32	1L
13	DQ5	7L	37	PH <sup>1</sup>	2B	61	DQ33	2L
14	DQ8	6K	38	SA7	3A	62	DQ31	2M
15	DQ7	7K	39	SA9	3C	63	DQ29	1N
16	$\overline{SBWa}$	5L	40	SA6	2C	64	DQ30	2N
17	$\overline{K}$	4L	41	SA5	2A	65	DQ27	1P
18	K	4K	42	DQ19	2D	66	DQ28	2P
19	G	4F	43	DQ18	1D	67	SA3	3T
20	$\overline{SBWb}$	56G	44	DQ21	2E	68	SA4	2R
21	DQ16	7H	45	DQ20	1E	69	SA0	4N
22	DQ17	6H	46	DQ22	2F	70	M1	3R
23	DQ14	7G	47	DQ24	2G			
24	DQ15	6G	48	DQ23	1G			

1. Input of PH register connected to V<sub>SS</sub>.

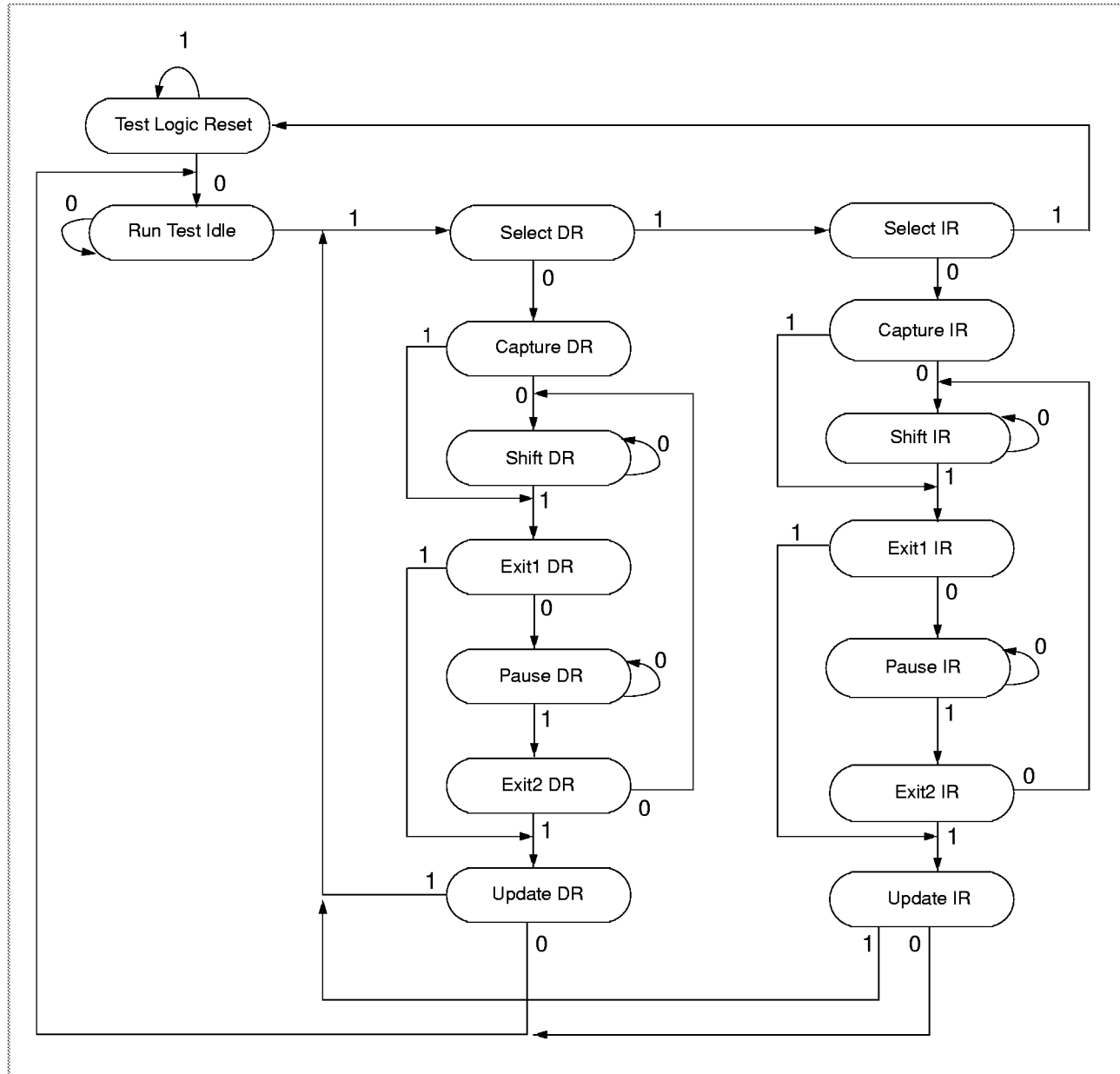


**Boundary Scan Order (x18) (PH =Place Holder)**

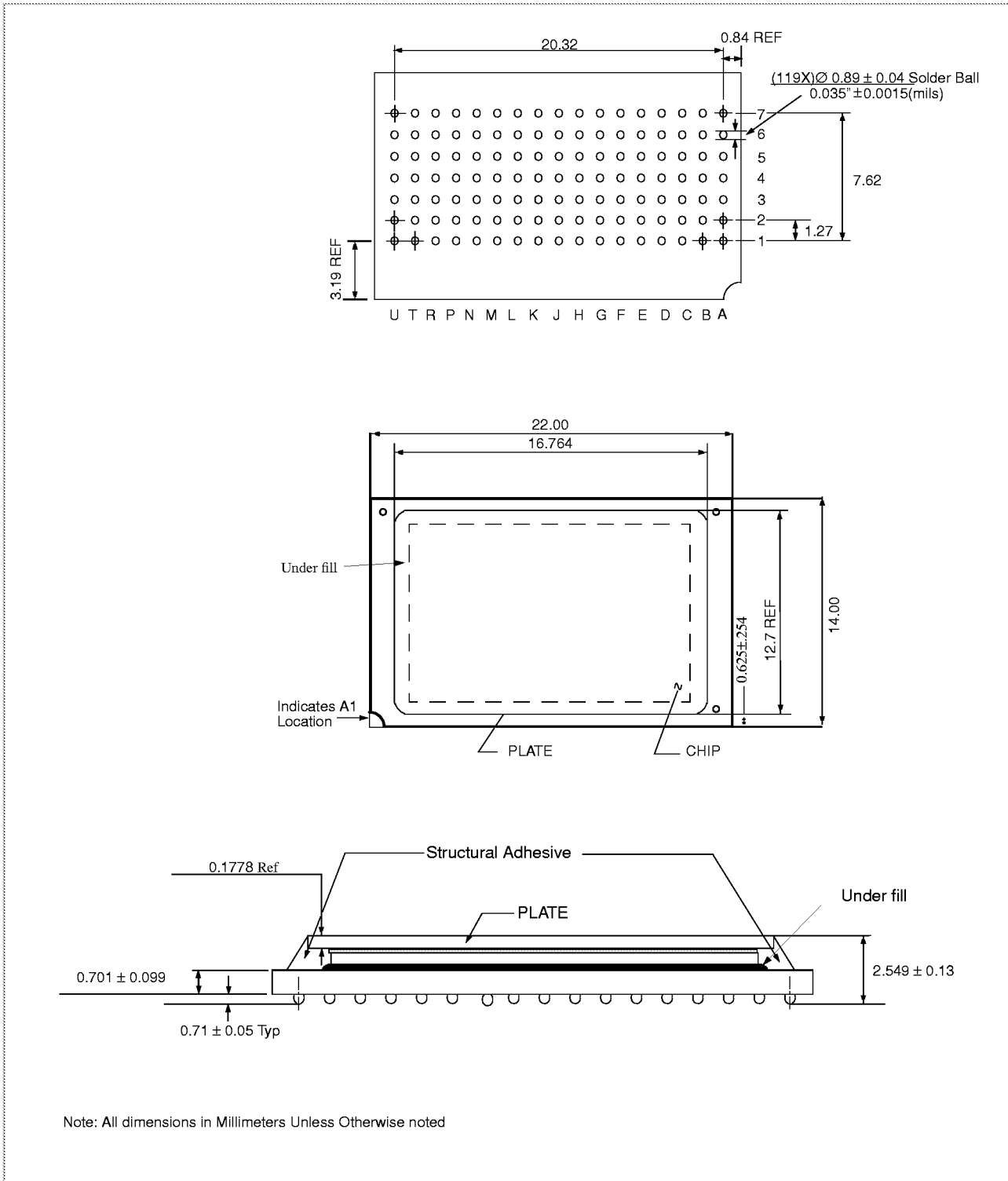
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH <sup>1</sup>	2B
2	SA12	6T	28	SA7	3A
3	SA1	4P	29	SA9	3C
4	SA13	6R	30	SA6	2C
5	SA17	5T	31	SA5	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ12	2E
8	DQ3	6N	34	DQ15	2G
9	DQ6	6L	35	DQ16	1H
10	DQ7	7K	36	SBW <sub>b</sub>	3G
11	SBW <sub>a</sub>	5L	37	ZQ	4D
12	K	4L	38	SS	4E
13	K	4K	39	C	4G
14	G	4F	40	C	4H
15	DQ8	6H	41	SW	4M
16	DQ5	7G	42	DQ17	2K
17	DQ4	6F	43	DQ14	1L
18	DQ2	7E	44	DQ13	2M
19	DQ1	6D	45	DQ11	1N
20	SA14	6A	46	DQ10	2P
21	SA15	6C	47	SA3	3T
22	SA10	5C	48	SA4	2R
23	SA16	5A	49	SA0	4N
24	PH <sup>1</sup>	6B	50	SA2	2T
25	SA11	5B	51	M1	3R
26	SA8	3B			

1. Input of PH register connected to V<sub>SS</sub>.

### TAP Controller State Machine



### 7 x 17 BGA Dimensions





---

## References Rev "D" - Last Character in Part Number (D)

The following documents give recommendations, restrictions and limitations for 2nd level attach process:

C4 SRAM Assembly Guide for Single Sided Assembly

Double Sided 4Meg Coupled Cap PBGA Card Assembly Guide

There is qualification information, including scope of application conditions qualified, available from your marketing representative.



## Revision Log

Rev	Contents of Modification
9/95	Initial Release of the 128K x 36 & 256K x 18, (5/6/7 cycle), HSTL, BGA, FLOW THRU Application Spec.
11/95	Update scan chain.
2/96	Updated part numbers, Updated package drawing.
5/13/96	Update part numbers.
7/15/96	Add Thermal resistance, update timings and currents.
10/03/96	Update timings
12/16/96	Update Timings (-4 bin: $T_{CHQV} = 2.5$ , $T_{CHQZ} = 2.5$ , $T_{CHKH} = 0.8$ )
1/97	Updated the package drawing.
2/97	Updated AC characteristics to reflect upgrade of part for 3.8ns & 4.2ns cycle time x36 parts.
8/20/97	Updated Test temps from Junction to Ambient.
5/98	Updated nomenclature on tristate tests.
6/98	Updated AC input data. Changed Programmable Impedance tolerance to $\pm 15\%$ and 2080 max cycle update. Changed Rev B to Rev D. Added references for Rev D and changed package diagram. Added Sleep mode statement.
2/99	Tightened the BGA ball diameter tolerance.





© International Business Machines Corp.1999

Printed in the United States of America  
All rights reserved

IBM and the IBM logo are registered trademarks of the IBM Corporation.

This document may contain preliminary information and is subject to change by IBM without notice. IBM assumes no responsibility or liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. The products described in this document are not intended for use in implantation or other direct life support applications where malfunction may result in direct physical harm or injury to persons. **NO WARRANTIES OF ANY KIND, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE OFFERED IN THIS DOCUMENT.**

For more information contact your IBM Microelectronics sales representative or visit us on World Wide Web at <http://www.chips.ibm.com>

IBM Microelectronics manufacturing is ISO 9000 compliant.