STK1390

nvTIME™ 8K x 8 Nonvolatile Static RAM with Real Time Clock

PRELIMINARY

FEATURES

- **Solid-state nonvolatile SRAM/RTC solution - no batteries required**
- **Ideal for metering applications**
- **25, 30, 35 and 45 ns SRAM read/write access**
- **Unlimited read/write cycles to SRAM**
- **NOVCEL™ technology - true nonvolatile RAM**
- **Software and hardware controlled nonvolatile cycles**
- **10 year data retention from each store cycle**
- **Full-featured Real Time Clock on-chip**
- **RTC operates from external capacitor - typical 1 month operation from 0.47F supercap**
- **Uses standard 32.768kHz Watch Crystal**
- **Commercial and industrial temperatures**
- **600 mil 32-pin DIP or 400 mil SOIC package**

DESCRIPTION

The Simtek STK1390 contains both an 8K fast static RAM with nonvolatile EEPROM shadow and a monolithic real time clock. The SRAM can be read and written an unlimited number of times while independent nonvolatile data resides in EEPROM. The RTC information consists of an additional 64 8-bit registers. The lower 12 registers are used for time and configuration information. The upper 52 registers are available for user information and are shadowed by EEPROM with each STORE cycle. The RTC registers are accessible through the SRAM I/O pins.

The STK1390 supports long-term, unpowered operation of the RTC from a capacitor. This eliminates the need for batteries without the need for complex alternate power sources.

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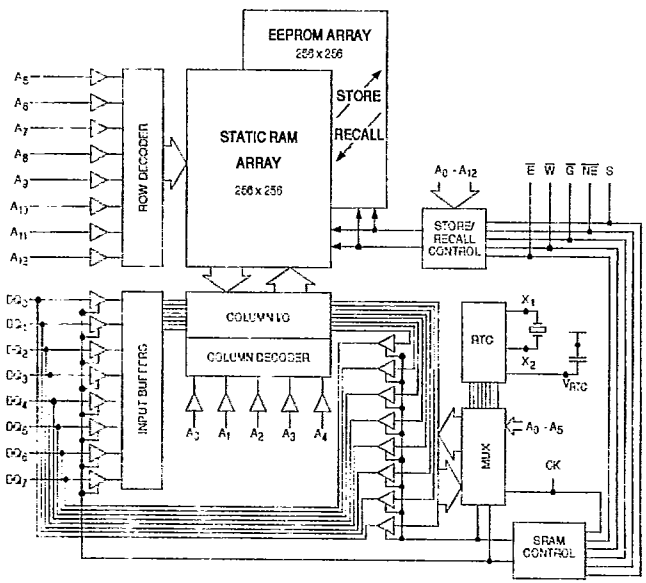
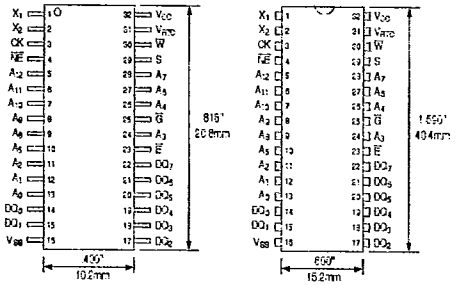
LOGIC BLOCK DIAGRAM



PINOUTS AND PACKAGES



A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{NE}$	Nonvolatile Enable
$\overline{G}$	Output Enable
CK	RTC Control
V_{CC}	Power (+5)
V_{SS}	Ground
V_{RTC}	Capacitor Input

STK1390

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} ..... -0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{G}$ ..... -0.5V to (V_{CC} + 0.5V)
Voltage on V_{RTC} relative to V_{CC} ..... +0.5V to -7.0V
Temperature under bias ..... -55°C to 125°C
Storage temperature ..... -65°C to 150°C
Power dissipation 1W
DC output current 15mA
(one output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average V_{CC} current		85 80 75 65		95 85 80 75	mA mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 30ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC2}[d]	Average V_{CC} current during *STORE* cycle		50		50	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB1}[c]	Average V_{CC} current (Standby, cycling TTL input levels)		30 27 23 20		34 30 27 23	mA mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 30ns t_{AVAV} = 35ns t_{AVAV} = 45ns $\overline{E} \geq V_{IH}$; all others cycling
I_{SB2}[c]	Average V_{CC} current (Standby, stable CMOS input levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{RTC}[e]	Average V_{RTC} current during backup mode		2		2	µA	V_{CC} = 0, V_{RTC} = -4V Typical current = 1µA
I_{ILK}	Input leakage current (any input except V_{RTC})		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-state output leakage current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input logic "1" voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All inputs
V_{IL}	Input logic "0" voltage	V_{SS} - .5	0.8	V_{SS} - .5	0.8	V	All inputs
V_{OH}	Output logic "1" voltage	2.4		2.4		V	I_{OUT} = -4mA
V_{OL}	Output logic "0" voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating temperature	0	70	-40	85	°C	

Note b: I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E} \geq V_{IH}$ or $S \leq V_{IL}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: I_{CC2} is the average current required for the duration of the *STORE* cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.
Note e: I_{RTC} is the average current draw from the capacitor. It does not flow through the V_{SS} pin.

AC TEST CONDITIONS

Input pulse levels ..... V_{SS} to 3V
Input rise and fall times ..... ≤ 5ns
Input and output timing reference levels 1.5V
Output load ..... See Figure 1

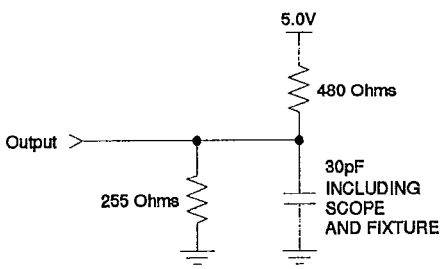


Figure 1: AC Output Loading

CAPACITANCE (T_A = 25C, f = 1.0MHz)[f]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

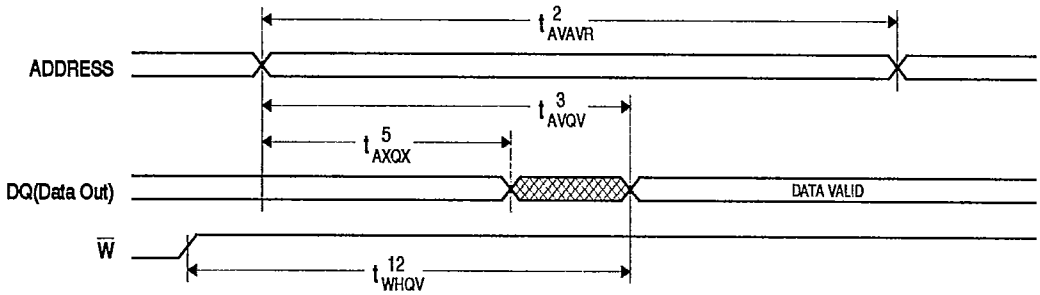
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

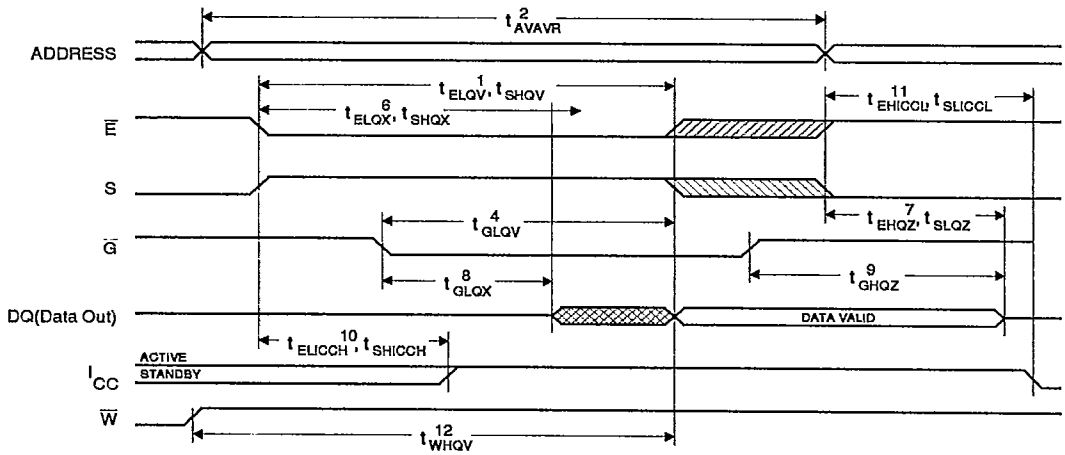
NO.	SYMBOLS		PARAMETER	STK1390-25		STK1390-30		STK1390-35		STK1390-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}, t_{SHQV}	t_{ACS}	Chip enable access time		25		30		35		45	ns
2	t_{AVAVR}[h]	t_{RC}	Read cycle time	25		30		35		45		ns
3	t_{AVQV}[j]	t_{AA}	Address access time		25		30		35		45	ns
4	t_{GLQV}	t_{OE}	Output enable to data valid		12		15		20		25	ns
5	t_{AXQX}[j]	t_{OH}	Output hold after address change	5		5		5		5		ns
6	t_{ELQX}, t_{SHQX}	t_{LZ}	Chip enable to output active	5		5		5		5		ns
7	t_{EHQZ}, t_{SLQZ}[j]	t_{HZ}	Chip disable to output inactive		13		15		17		20	ns
8	t_{GLQX}	t_{OLZ}	Output enable to output active	0		0		0		0		ns
9	t_{GHQZ}[j]	t_{OHZ}	Output disable to output inactive		13		15		17		20	ns
10	t_{ELICCH}, t_{SHICCH}[f]	t_{PA}	Chip enable to power active	0		0		0		0		ns
11	t_{EHICCL}, t_{SLICCL}[d, f]	t_{PS}	Chip disable to power standby		25		30		35		45	ns
12	t_{WHQV}	t_{WR}	Write recovery time		30		35		45		55	ns

Note g: $\overline{NE}$ must be high and CK must be low during entire cycle.
Note h: For READ CYCLES #1 and #2, $\overline{W}$ and $\overline{NE}$ must be high and CK must be low for entire cycle.
Note i: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low and S high
Note j: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1[g, h, i]



SRAM READ CYCLE #2[g, h]



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SRAM WRITE CYCLES #1 & #2; $\overline{G}$ high

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK1390-25		STK1390-30		STK1390-35		STK1390-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
13	t_{AVAW}	t_{AVAW}	t_{WC}	Write cycle time	25		30		35		45		ns
14	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write pulse width	20		25		30		35		ns
15	t_{ELWH}	t_{ELEH}, t_{SHSL}	t_{CW}	Chip enable to end of write	20		25		30		35		ns
16	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DW}	Data set-up to end of write	12		15		18		20		ns
17	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{DH}	Data hold after end of write	0		0		0		0		ns
18	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AW}	Address set-up to end of write	20		25		30		35		ns
19	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AS}	Address set-up to start of write	0		0		0		0		ns
20	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{WR}	Address hold after end of write	0		0		0		0		ns

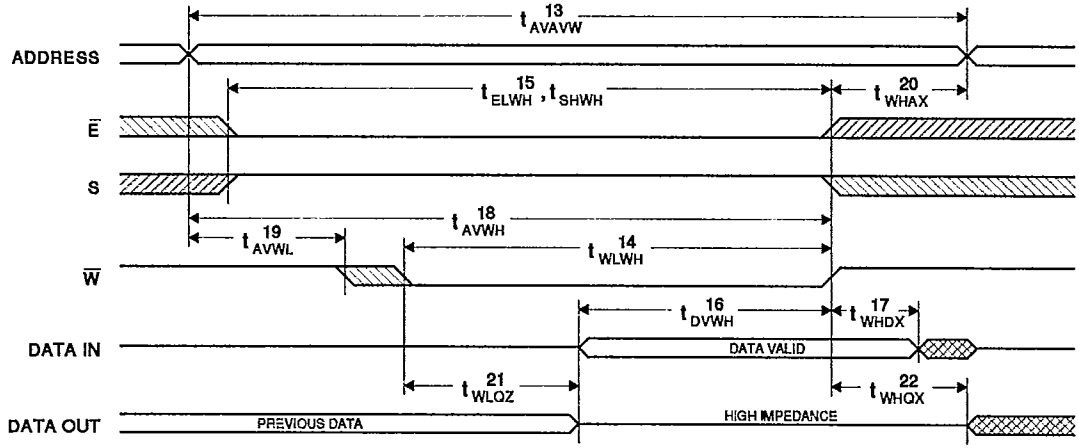
SRAM WRITE CYCLES #1 & #2; $\overline{G}$ low

(V_{CC} = 5.0V ± 10%)

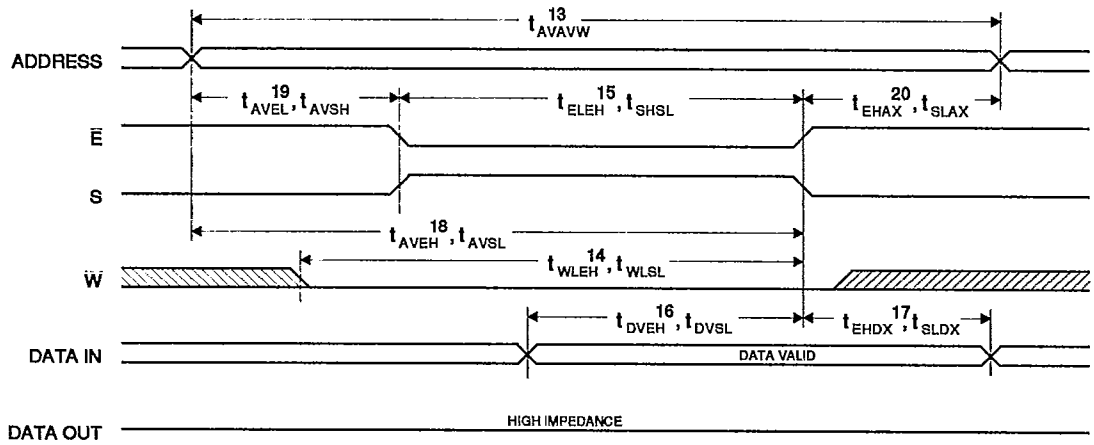
NO.	SYMBOLS			PARAMETER	STK1390-25		STK1390-30		STK1390-35		STK1390-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
13	t_{AVAW}	t_{AVAW}	t_{WC}	Write cycle time	45		45		45		45		ns
14	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write pulse width	35		35		35		35		ns
15	t_{ELWH}	t_{ELEH}, t_{SHSL}	t_{CW}	Chip enable to end of write	35		35		35		35		ns
16	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DW}	Data set-up to end of write	30		30		30		30		ns
17	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{DH}	Data hold after end of write	0		0		0		0		ns
18	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AW}	Address set-up to end of write	35		35		35		35		ns
19	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AS}	Address set-up to start of write	0		0		0		0		ns
20	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{WR}	Address hold after end of write	0		0		0		0		ns
21	t_{WLQZ}[l]		t_{WZ}	Write enable to output disable		35		35		35		35	ns
22	t_{WHQX}		t_{OW}	Output active after end of write	5		5		5		5		ns

Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} or S must be ≤ V_{IL} during address transitions.
Note l: If $\overline{W}$ is low when either $\overline{E}$ goes low or S goes high, the outputs remain in the high impedance state.

SRAM WRITE CYCLE #1: $\overline{W}$ CONTROLLED[g, k]



SRAM WRITE CYCLE #2: $\overline{E}$, S CONTROLLED[g, k]



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NONVOLATILE MEMORY OPERATION

HARDWARE MODE SELECTION

$\overline{E}$	S	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	L	X	X	X	Not selected	Standby
L	H	H	L	H	Read RAM	Active
L	H	L	X	H	Write RAM	Active
L	H	H	L	L	Nonvolatile *RECALL*[m]	Active
L	H	L	H	L	Nonvolatile *STORE*	I_{CC2}
L L	H H	L H	L H	L X	No operation	Active

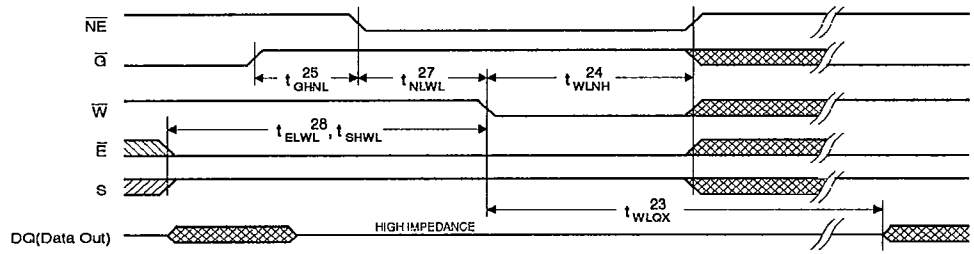
HARDWARE *STORE* CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

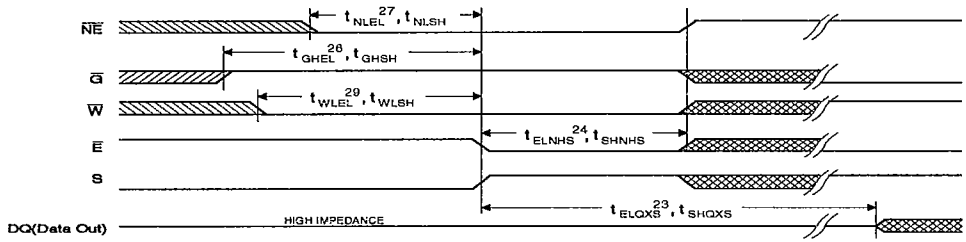
NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
23	t_{WLQX}[o]	t_{ELQXS}, t_{SHQXS}	t_{STORE}	*STORE* cycle time		10	ms
24	t_{WLNH}[p]	t_{ELNHS}, t_{SHNHS}	t_{WCS}	*STORE* initiation cycle time	25		ns
25	t_{GHNL}			Output disable set-up to $\overline{NE}$ fall	5		ns
26		t_{GHEL}, t_{GHSH}		Output disable set-up to $\overline{E}$ fall	5		ns
27	t_{NLWL}	t_{NLEL}, t_{NLSH}		$\overline{NE}$ set-up	5		ns
28	t_{ELWL}, t_{SHWL}			Chip enable set-up	5		ns
29		t_{WLEL}, t_{WLSH}		Write enable set-up	5		ns

Note m: An automatic *RECALL* also takes place at power-up, starting when V_{CC} exceeds 4.1V, and taking t_{RECALL} from the time at which V_{CC} exceeds 4.5V. V_{CC} must not drop below 4.1V once it has exceeded it for the *RECALL* to function properly.
Note n: If $\overline{E}$ is low and S is high for any period of time in which $\overline{W}$ is high while $\overline{G}$ and $\overline{NE}$ are low, then a *RECALL* cycle may be initiated.
Note o: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. Note that *STORE* cycles are inhibited/aborted by V_{CC} < 4.1V.
Note p: Once t_{WC} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$, S and $\overline{E}$, the *STORE* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, $\overline{W}$, S or $\overline{E}$ may be used to terminate the *STORE* initiation cycle.

HARDWARE *STORE* CYCLE #1: $\overline{W}$ CONTROLLED[n]



HARDWARE *STORE* CYCLE #2: $\overline{E}$ or S CONTROLLED[n]



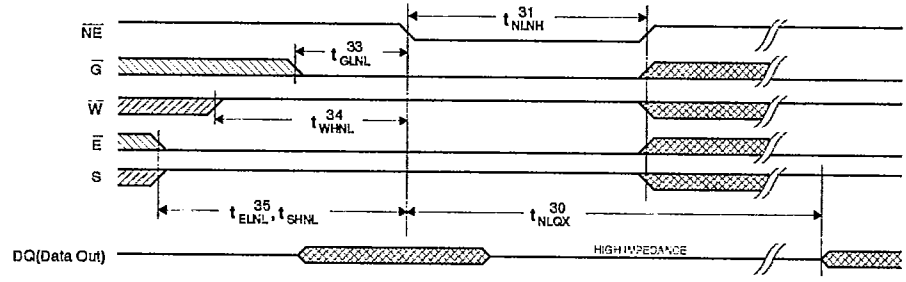
HARDWARE *RECALL* CYCLES #1, #2 & #3

(V_{CC} = 5.0V ± 10%)

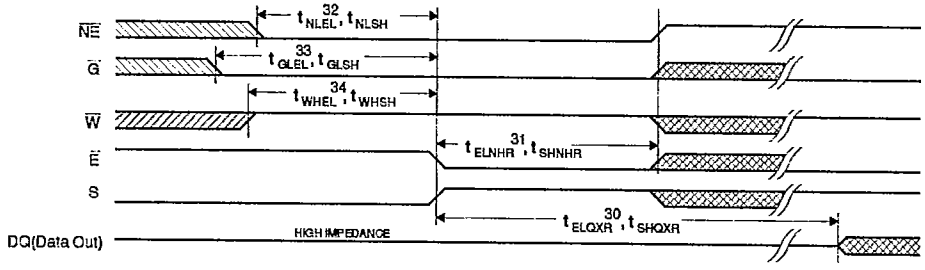
NO.	SYMBOLS				PARAMETER	MIN	MAX	UNITS
	#1	#2	#3	Alt.				
30	t_{NLQX}[q]	t_{ELQXR}, t_{SHQXR}	t_{GLQXR}	t_{RECALL}	*RECALL* cycle time		25	µs
31	t_{NLNH}[r]	t_{ELNHR}, t_{SHNHR}	t_{GLNH}	t_{RCS}	*RECALL* initiation cycle time	25		ns
32		t_{NLEL}, t_{NLSH}	t_{NLGL}		$\overline{NE}$ set-up	0		ns
33	t_{GLNL}	t_{GLEL}, t_{GLSH}			Output enable set-up	0		ns
34	t_{WHNL}	t_{WHEL}, t_{WHSH}	t_{WHGL}		Write enable set-up	5		ns
35	t_{ELNL}, t_{SHNL}		t_{ELGL}, t_{SHGL}		Chip enable set-up	0		ns

Note q: Measured with S, $\overline{W}$ and $\overline{NE}$ high, and $\overline{G}$ and $\overline{E}$ low.
Note r: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$, S and $\overline{E}$, the *RECALL* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, S or $\overline{E}$ may be used to terminate the *RECALL* initiation cycle.
Note s: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ and S are high, then a *STORE* cycle will be initiated instead of a *RECALL*.

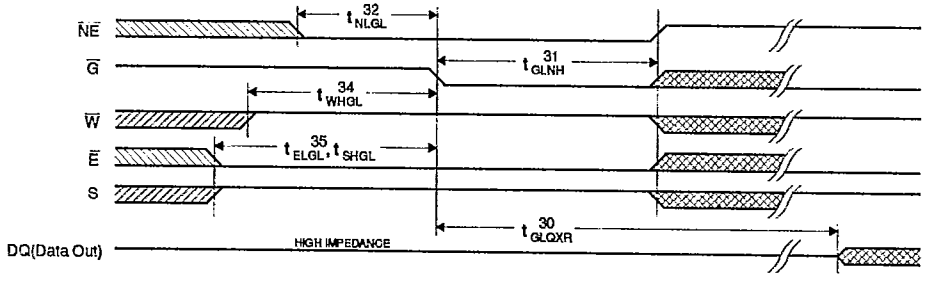
HARDWARE *RECALL* CYCLE #1: $\overline{NE}$ CONTROLLED[n]



HARDWARE *RECALL* CYCLE #2: $\overline{E}$ or S CONTROLLED[n]



HARDWARE *RECALL* CYCLE #3: $\overline{G}$ CONTROLLED[n, s]



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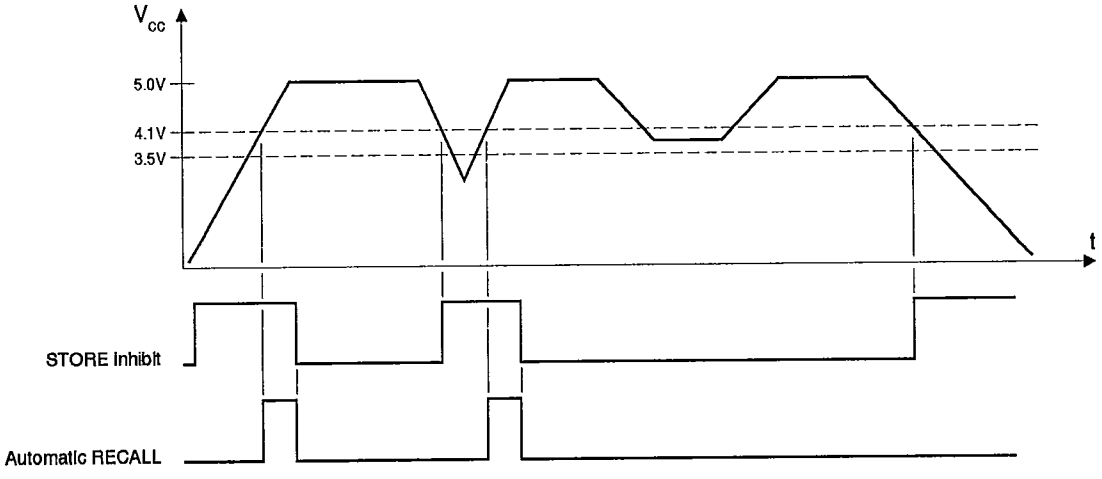
SOFTWARE MODE SELECTION

$\overline{E}$	S	$\overline{W}$	A_{12} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	L	X	X	Not selected	Output high Z	Standby	
L	H	H	X	Read SRAM	Output data	Active	u
L	H	L	X	Write SRAM	Input data	Active	
L	H	H	0000	Read SRAM	Output data	Active	t, u
			1555	Read SRAM	Output data		t, u
			0AAA	Read SRAM	Output data		t, u
			1FFF	Read SRAM	Output data		t, u
			10F0	Read SRAM	Output data		t, u
			0F0F	Nonvolatile *STORE*	Output high Z	I_{CC2}	t
L	H	L	0000	Read SRAM	Output data	Active	t, u
			1555	Read SRAM	Output data		t, u
			0AAA	Read SRAM	Output data		t, u
			1FFF	Read SRAM	Output data		t, u
			10F0	Read SRAM	Output data		t, u
			0F0E	Nonvolatile *RECALL*	Output high Z		t

Note t: The six consecutive addresses must be in the order listed—0000, 1555, 0AAA, 1FFF, 10F0, 0F0F for a *STORE* cycle, or 0000, 1555, 0AAA, 1FFF, 10F0, 0F0E for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note u: I/O state assumes that $\overline{G} \leq V_{IL}$. Initiation and operation of software nonvolatile cycles does not depend on the state of $\overline{G}$.

STORE CYCLE INHIBIT AND AUTOMATIC POWER-UP *RECALL*



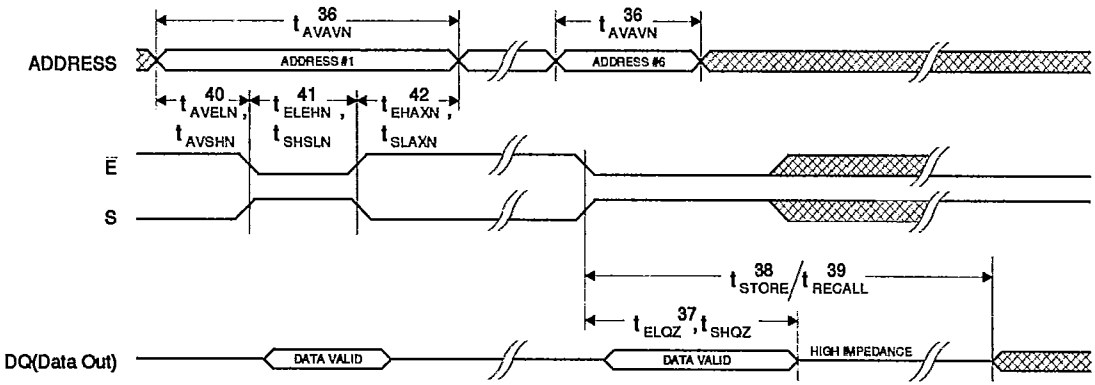
SOFTWARE *STORE/RECALL* CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK1390-25		STK1390-30		STK1390-35		STK1390-45		UNITS
	#1	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
36	t_{AVAVN}	t_{RC}	*STORE/RECALL* initiation cycle time	25		30		35		45		ns
37	t_{ELQZ}, t_{SHQZ}[v]		Chip enable to output inactive		65		85		85		85	ns
38	t_{ELQXS}, t_{SHQXS}	t_{STORE}[w]	STORE cycle time		10		10		10		10	ms
39	t_{ELQXR}, t_{SHQXR}	t_{RECALL}[x]	RECALL cycle time		20		20		20		20	µs
40	t_{AVELN}, t_{AVSHN}[y]	t_{AE}	Address set-up to chip enable	0		0		0		0		ns
41	t_{ELEHN}, t_{SHSLN}[y,z]	t_{EP}	Chip enable pulse width	15		20		25		35		ns
42	t_{EHAXN}, t_{SLAXN}[y]	t_{EA}	Chip disable to address change	0		0		0		0		ns

Note v: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.
Note w: Note that *STORE* cycles (but not *RECALL*s) are aborted by V_{CC} < 4.1V (*STORE* inhibit).
Note x: A *RECALL* cycle is initiated automatically at power-up when V_{CC} exceeds 4.1V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.
Note y: Noise on the $\overline{E}$ or S pins may trigger multiple read cycles from the same address and abort the address sequence.
Note z: If the chip enable pulse width is less than t_{ELQV} or t_{SHQV}(see READ CYCLE #2) but greater than or equal to t_{ELEHN} or t_{SHSLN}, then the data may not be valid at the end of the low pulse. However, the *STORE* or *RECALL* will still be initiated.
Note aa: $\overline{W}$ must be high when $\overline{E}$ is low and S is high during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either high or low throughout. Addresses #1 through #6 are found in the SOFTWARE MODE SELECTION table. Address #6 determines whether the STK1390 performs a *STORE* or *RECALL*.

SOFTWARE *STORE/RECALL* CYCLE[aa]



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REAL TIME CLOCK OPERATION

RTC READ CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	MIN	MAX	UNITS
	#1	Alt.				
43	t_{ELQVR}, t_{SHQVR}	t_{RTC}	RTC READ access time		50	ns
44	t_{ELELR}, t_{SHSHR}		RTC READ cycle time	50		ns
45	t_{CHEL}, t_{CHSH}		CK set-up to start of RTC READ	0		ns
46	t_{AVELR}, t_{AVSHR}[ab]		Address set-up to start of RTC READ	0		ns
47	t_{EHCL}, t_{SLCL}		CK hold from end of RTC READ	0		ns
48	t_{EHAXR}, t_{SLAXR}[ab]		Address hold from end of RTC READ	0		ns
49	t_{CLQV}		SRAM access time from end of RTC cycle		50	ns

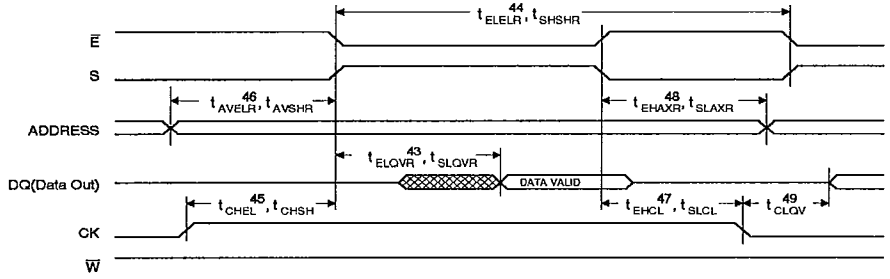
RTC WRITE CYCLE

(V_{CC} = 5.0V ± 10%)

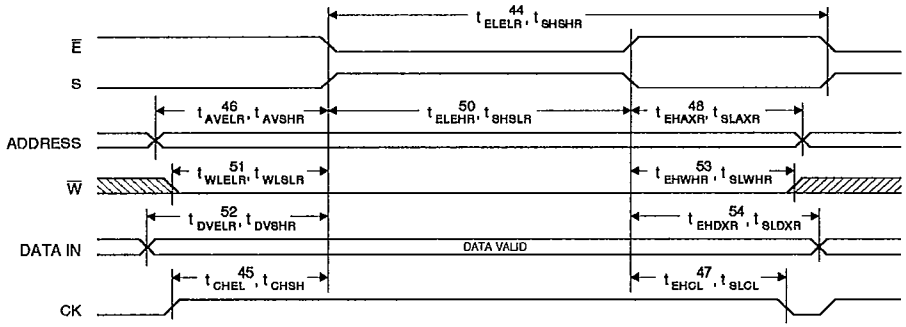
NO.	SYMBOLS		PARAMETER	MIN	MAX	UNITS
	#1	Alt.				
50	t_{ELEHR}, t_{SHSLR}		RTC WRITE pulse width	50		ns
51	t_{WLELR}, t_{WLSHR}		$\overline{W}$ set-up to start of RTC WRITE	0		ns
52	t_{DVELR}, t_{DVSHR}		Data set-up to start of RTC WRITE	0		ns
53	t_{EHWHR}, t_{SLWHR}		$\overline{W}$ hold from end of RTC WRITE	0		ns
54	t_{EHDXR}, t_{SLDXR}		Data hold from end of RTC WRITE	0		ns

Note ab: Addresses A_5 - A_0 only. All other addresses are ignored during RTC cycles

RTC READ CYCLE



RTC WRITE CYCLE



DEVICE OPERATION

The STK1390 has three modes of operation: SRAM mode, nonvolatile mode and real time clock mode. The mode is determined by the state of the $\overline{NE}$ and CK pin. When in SRAM mode, the memory operates as an ordinary static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In RTC mode the STK1390 provides access to the 64 bytes of RTC register memory.

SRAM READ

The STK1390 performs a READ cycle whenever $\overline{E}$, $\overline{G}$ and CK are low and $\overline{NE}$, $\overline{W}$ and S are high. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$, S or $\overline{G}$, the outputs will be valid at t_{ELQV}, t_{SHQV} or at t_{GLQV}, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or S is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$, $\overline{W}$ and CK are low and S and $\overline{NE}$ are high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high or S goes low at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} or t_{DVSL} before the end of an $\overline{E}$ or S controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

Keeping $\overline{G}$ high during WRITE cycles also enables use of the faster write specifications.

HARDWARE NONVOLATILE *STORE*

A hardware *STORE* cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are low and $\overline{G}$ and S are high. While any sequence to achieve this state will initiate a *STORE*, only $\overline{W}$ initiation (*STORE* CYCLE #1) and $\overline{E}$ or S initiation (*STORE* CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a *STORE* cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled and the DQ_{0-7} pins are tri-stated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$, S and $\overline{NE}$ are high at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the *STORE*.

SOFTWARE NONVOLATILE *STORE*

The STK1390 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK1390 offers two levels of protection to suppress inadvertent *STORE* cycles. If the control signals ($\overline{E}$, S, $\overline{G}$, $\overline{W}$ and $\overline{NE}$) remain in the *STORE* condition at the end of a *STORE* cycle, a second

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STORE cycle will *not* be started. The *STORE* (or *RECALL*) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK1390 offers hardware protection through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.1V. 4.1V is a typical, characterized value.

HARDWARE NONVOLATILE *RECALL*

A hardware *RECALL* cycle is performed when $\overline{E}$, $\overline{G}$ and $\overline{NE}$ are low and $\overline{W}$ and S are high. Like the *STORE* cycle, *RECALL* is initiated when the last of the five clock signals goes to the *RECALL* state. Once initiated, the *RECALL* cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the *RECALL* completes, any READ or WRITE state on the input pins will take effect.

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the *STORE* cycle, a transition must occur on a control pin to cause a hardware *RECALL*, preventing inadvertent multi-triggering. On power-up, once V_{CC} exceeds the V_{CC} Sense voltage of 4.1V, a *RECALL* cycle is automatically initiated. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{NLQX} after V_{CC} exceeds 4.1V.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate *RECALL* cycle

RTC ACCESSES

The internal real time clock of the STK1390 is accessed by executing READ or WRITE cycles while the CK pin is high. In this mode the DQ_{0-7} signals correspond to the state of the addressed RTC register. Only addresses A_5 - A_0 are used by the RTC. The other address pins are ignored during RTC cycles. The 64 RTC registers can be accessed in any order.

RTC ADDRESS MAP

The address map is shown in Figure 2. The RTC memory consists of 52 bytes of user RAM, 8 bytes of RTC time and calendar data and 4 control and status bytes. All 64 bytes can be directly written or read except the following:

- The 1/100 seconds byte is read only.
- Bit 7 and 6 of register A is read only.
- Register C is read only.
- The reset register is write only.

The contents of the three control registers (A-C) and the reset register are described in the RTC REGISTERS section.

TIME AND CALENDAR LOCATIONS

The time and calendar information is obtained by reading the appropriate register locations as shown in Figure 2. The time and calendar are set (or initialized) by writing the same locations. The contents of the eight time and calendar bytes can be encoded in either binary or binary-coded decimal (BCD) format.

Before initializing the internal time and calendar registers, the SET bit in Register B should be set to a '1' to prevent internal time/calendar updates while the registers are being written. Before writing the time and calendar registers, ensure that the data mode (DM) bit of Register B is set appropriately for either binary or BCD data. All registers must use the same data mode. After writing the time registers the SET bit must be cleared to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected data mode. The data mode cannot be changed without re-initializing the time registers.

The time and calandar mode table shows the binary and BCD formats of the eight time and calendar locations. The 24/12 bit in Register B establishes whether the hours location represents 1-to-12 or 0-to-24 hour format. The 24/12 bit cannot be changed without re-initializing the hours location. When the 12-hour format is selected a '1' in the high-order bit

of the hours byte represents PM and a '0' represents AM.

USER RAM

The 52 User RAM bytes shown in Figure 2 are not used for RTC function. They are general purpose memory and are available during the update cycle. These are nvSRAM memory bytes that are shadowed with EEPROM. During nvSRAM *STORE* cycles these bytes are transferred to EEPROM and during *RECALL* cycles and at power up they are copied to SRAM.

RTC UPDATE CYCLE

The STK1390 executes an update cycle once per 1/100 second, assuming that the SET bit in Register B is cleared. The SET bit in the '1' state will inhibit internal updates.

The function of the update cycle is to increment the 1/100 seconds byte, check for overflow, increment the seconds byte when appropriate and so forth through to the year byte.

Since this update cycle occurs asynchronously with the reading of the time and calendar registers, it is possible to read these bytes before the updates have propagated. This would result in invalid output. To ensure this does not occur the update-in-progress (UIP) bit of Register A should be used to determine when the internal update is in progress. The UIP bit is synchronized with the update cycle and will be set to '1' 244µs before the update begins. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data will be changed. The UIP bit is cleared after the internal update is complete.

RTC REGISTERS

The STK1390 has four control registers that are accessible at all times, even during the update cycle. The bits of each of the registers are mapped to DQ_{0-7} during and RTC read or write.

REGISTER A

REGISTER A FORMAT

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	NVV	TEST	0	0	0	0	0

UIP - The Update In Progress (UIP) bit is a status flag set and cleared by the internal circuitry. When the UIP bit is a '1' the update transfer will occur within 250µs. When UIP is a '0', the update transfer will not occur for at least 250µs. The UIP bit is read only and is not affected by RESET. Writing the SET bit in Register B to a '1' inhibits any update transfer and clears the UIP status bit.

NVV - The Non-Volatile Valid (NVV) bit is a status flag that indicates whether the 8K SRAM bytes or the 52 User RAM bytes have been written since the last nonvolatile cycle. This can be used to indicate whether a *STORE* is required to protect volatile data. A '0' indicates that the SRAM and nvSRAM contents may not be the same and a '1' indicates that they are identical. The NVV bit is read only and is not affected by RESET. It will be set by a nonvolatile cycle and cleared by a subsequent WRITE cycle.

TEST - A '1' written into this bit puts the device into test mode. This allows setting of the oscillator frequency and parallel testing of the clock counters. For normal operation the TEST bit must be a '0'. This bit is read/write and is not affected by RESET.

BIT4 TO BIT0 - These are unused bits and always read '0'.

REGISTER B

REGISTER B FORMAT

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	0	0	0	0	DM	24/12	DSE

SET - When the SET bit is a '0' the update cycle functions normally by advancing the time registers once per 1/100 second. When the SET bit is written to a '1', the 1/100 seconds byte is cleared to 0 and any update cycle is inhibited, allowing the time and calendar bytes to be written without any intervening update cycles. SET is a read/write bit that is not modified by RESET or internal functions of the device.

BIT6 TO BIT3 - These are unused bits that always read '0'.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit must be set by the user to the appropriate format and can be read as required.

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This bit is not modified by RESET or internal functions of the device. A '1' in DM signifies binary format, while a '0' in DM specifies Binary Coded Decimal (BCD).

24/12 - The 24/12 control bit establishes the format of the hours bytes. A '1' indicates the 24-hour mode and a '0' indicates the 12-hour mode. This is a read/write bit and is not affected by RESET or internal functions.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit that enables two special updates when DSE is '1'. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a '0'. This bit is not affected by RESET or internal functions.

REGISTER C

REGISTER C FORMAT

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the history of the crystal oscillator circuit. This bit is cleared to '0' when the crystal oscillator has stopped for longer than ~1 second. The most likely cause of this will be a drop in the V_{RTC} voltage to less than -2V during low power mode. This indicates that the contents of the time/calendar and control/status registers are questionable. The VRT bit is not modified by RESET and is set to '1' by reading Register C.

BIT6 TO BIT0 - These are unused bits that always read '0'.

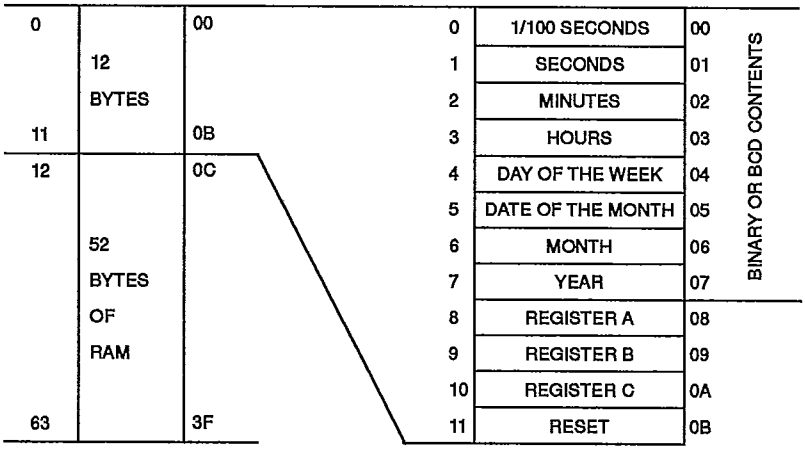
RESET REGISTER

Writing to RTC location 0BH causes the 1/100 seconds, seconds, minutes year registers to be reset to 0. The day of week, date of month and month registers are set to 1. The hour byte is cleared to 0 if the 24/12 bit is a '1', and is set to 1 if the 24/12 bit is a '0'.

V_{RTC} CAPACITOR

The V_{RTC} pin provides the "ground" connection for the STK1390. This pin can be connected to ground if clock operation is not required during a power loss. If clock operation is required during power loss a capacitor must be connected between V_{RTC} and V_{CC}. The size of the capacitor is determined by the maximum clock operating time required and the I_{RTC} current specification. For example a 0.47F capacitor, such as the NEC FS0H474Z Supercap will provide 30 days unpowered clock operation. The capacitor is connected between V_{RTC} and V_{CC}.

On power up, the STK1390 provides a time-out to allow the capacitor on the V_{RTC} pin to charge. When initially powered up, the V_{RTC} voltage will rise with V_{CC}. The STK1390 will pull the V_{RTC} pin back to ground, charging the capacitor in the process. Until the V_{RTC} pin reaches about 1V above V_{SS} the STK1390 will remain in a standby mode. This ensures proper operation of the clock. This charging time can be reduced by connecting a low-leakage diode between V_{RTC} and V_{SS}.



Note: Only addresses A_5 - A_0 are used. Addresses A_{12} - A_6 are ignored.

Figure 2: RTC ADDRESS MAP

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TIME AND CALENDAR DATA MODES TABLE

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	1/100 Seconds	0-99	00-63	00-99
1	Seconds	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Hours - 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours - 24-hr Mode	0-23	00-17	00-23
4	Day of the Week Sunday=1	1-7	01-07	01-07
5	Date of the Month	1-31	01-1F	01-31
6	Month	1-12	01-0C	01-12
7	Year	0-99	00-63	00-99

ORDERING INFORMATION

STK1390 - 5 C 30 I

Temperature Range
- blank = Commercial (0 to 70 degrees C)
- I = Industrial (–40 to 85 degrees C)

Access Time
- 25 = 25ns
- 30 = 30ns
- 35 = 35ns
- 45 = 45ns

Package
- W = Plastic 32-pin 600 mil DIP
- S = Plastic 32-pin 400 mil SOIC

Retention/Endurance
- blank = 10 years/10,000 cycles
- 5 = 10 years/100,000 cycles