FEDL7204-001DIGEST-01
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OKI Semiconductor

ML7204-001

VoIP CODEC

GENERAL DESCRIPTION

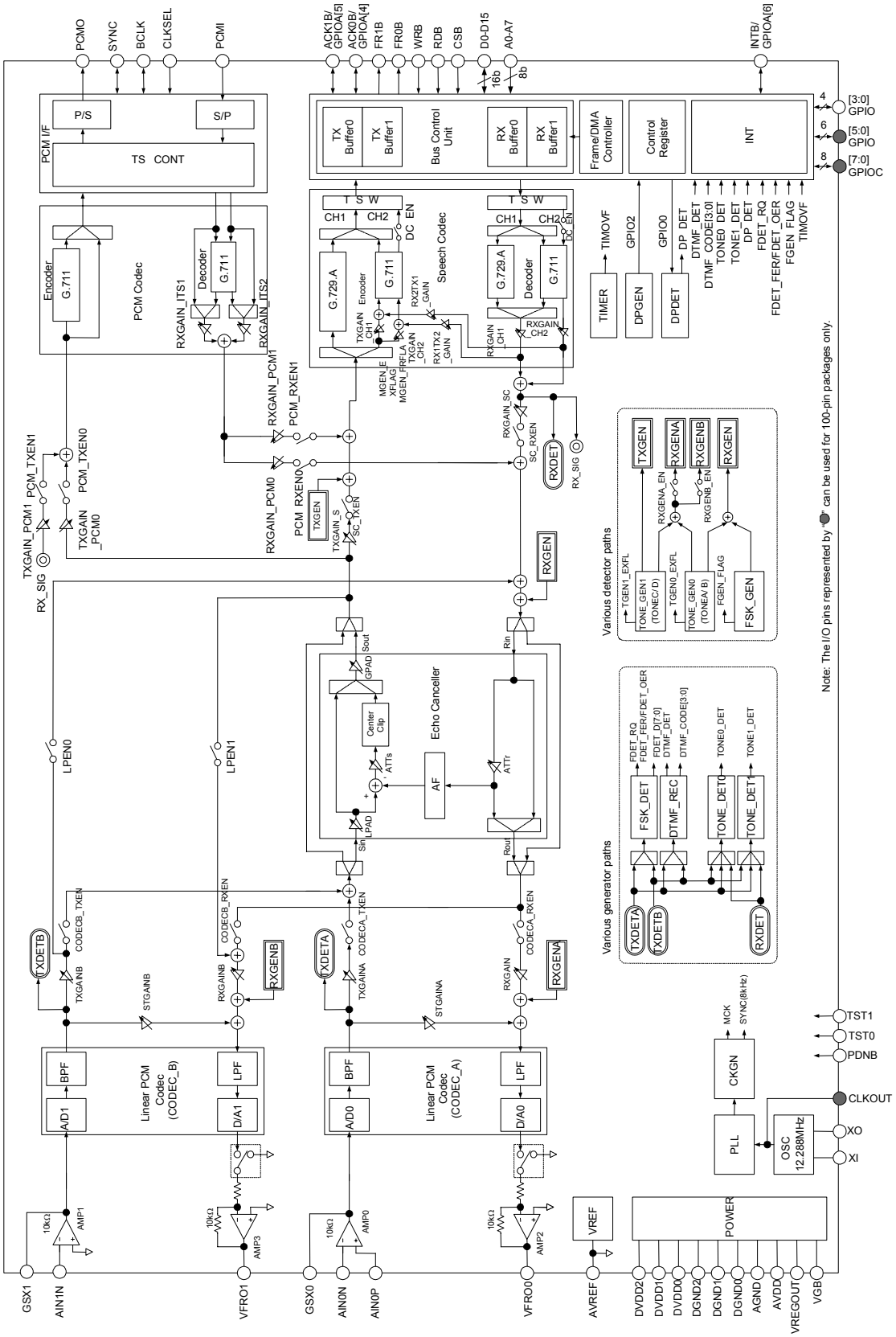
The ML7204-001 is a speech CODEC for VoIP. As a speech CODEC, this LSI allows selection of G.729.A/G711 and supports the PLC (Packet Loss Concealment) function.
With an echo canceler that handles 32 ms-delay and FSK detection/generation, DTMF detection/generation, and tone detection/generation functions, the ML7204-001 is the most suitable LSI for adding the VoIP function to TAs and routers.

FEATURES

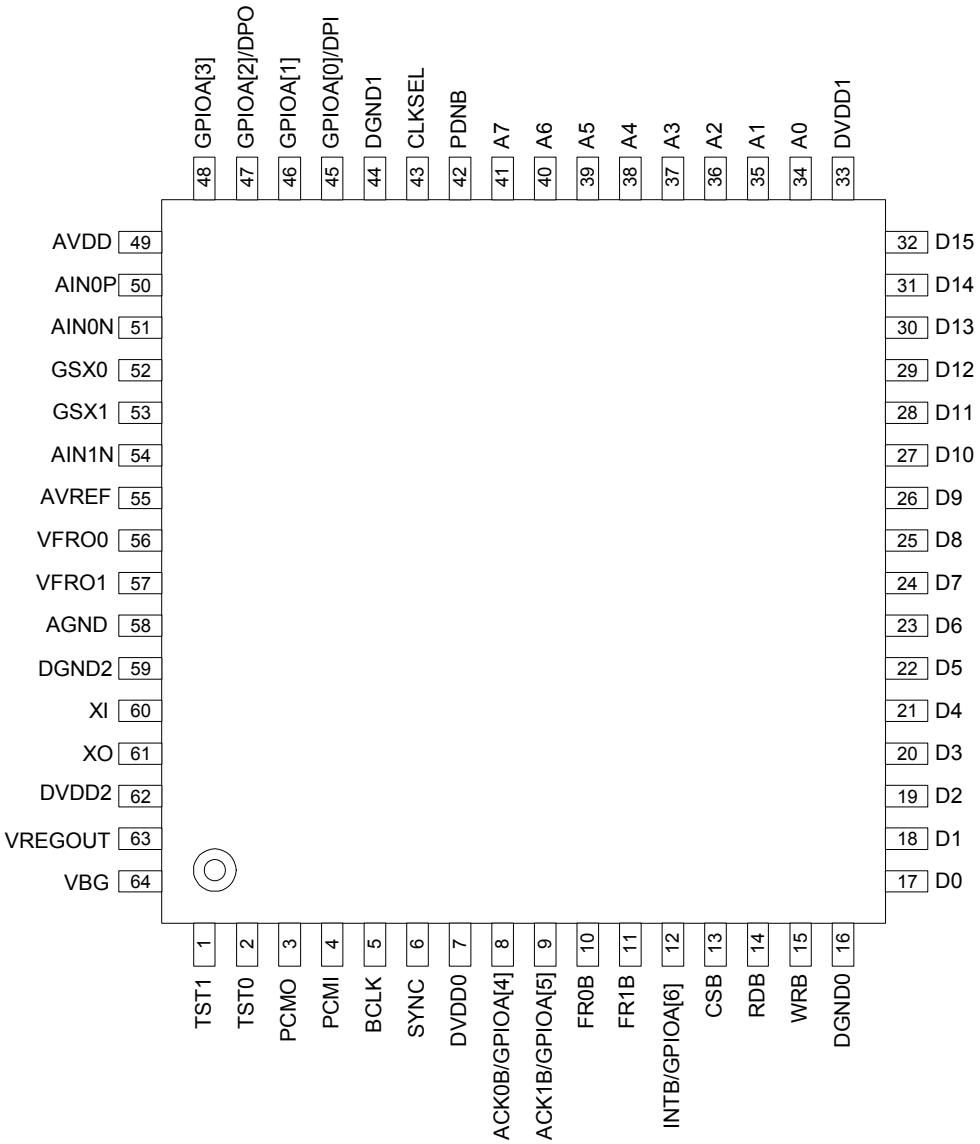
- Power supply voltage
  Digital power supply voltage (DVDD0, 1, 2): 3.0 to 3.6 V
  Analog power supply voltage (AVDD): 3.0 to 3.6 V
- Speech CODEC:
  G.729.A (8 kbps)/G.711 (64 kbps) μ-law and A-law (supports individual setting for transmission and reception)
  Supports ITU-T G.711 Appendix 1 compliant PLC (Packet Loss Concealment) function
  Supports the 2-channel processing function (for 3-way communication)
- Built-in FIFO buffer (640 bytes) for transmission/reception data transfer
  Allows selection of Frame/DMA (slave) interface
- Echo canceler for handling 32 ms delay
- DTMF detection
- DTMF generation (the tone generation function enables generation of DTMF signals)
- Tone detection: 2 types (1650 Hz and 2100 Hz: Detection frequency can be changed)
- Tone generation: 2 types
- FSK detection
- FSK generation
- Built-in 16-bit timer: 1 channel
- Dial pulse detection function (secondary function of general-purpose I/O ports)
- Dial pulse transmission function (secondary function of general-purpose I/O ports)
- General-purpose I/O ports
  64-pin package: Equipped with 7 ports (with some of them having secondary function allocation)
  100-pin package: Equipped with 21 ports (with some of them having secondary function allocation)
- Two types of built-in linear PCM CODEC (CODEC_A and CODEC_B)
- Analog interface
  CODEC_A side: Incorporates one type each of input amplifier and output amplifier (10 kΩ driving)
  CODEC_B side: Incorporates one type each of input amplifier and output amplifier (10 kΩ driving)
- PCM interface coding format:
  Allows selection of 16-bit linear/G.711 (64 kbps) μ-law or A-law
- PCM serial transmission rate: 64 kHz to 2.048 MHz (fixed to 2.048 MHz for output)
- PCM time slot assignment function (allows up to 2 slots for input and 1 slot for output individually)
  When set to μ-law/A-law: Supports up to 32 slots (BCLK: 2.048 MHz)
  When set to 16-bit linear: Supports up to 16 slots (BCLK: 2.048 MHz)

- Master clock frequency:
  12.288 MHz (crystal; external input)
- Supports hardware and software power down
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK) (ML7204-001GA)
  100-pin plastic TQFP (TQFP100-P-1414-0.50-BK) (ML7204V-001TB)

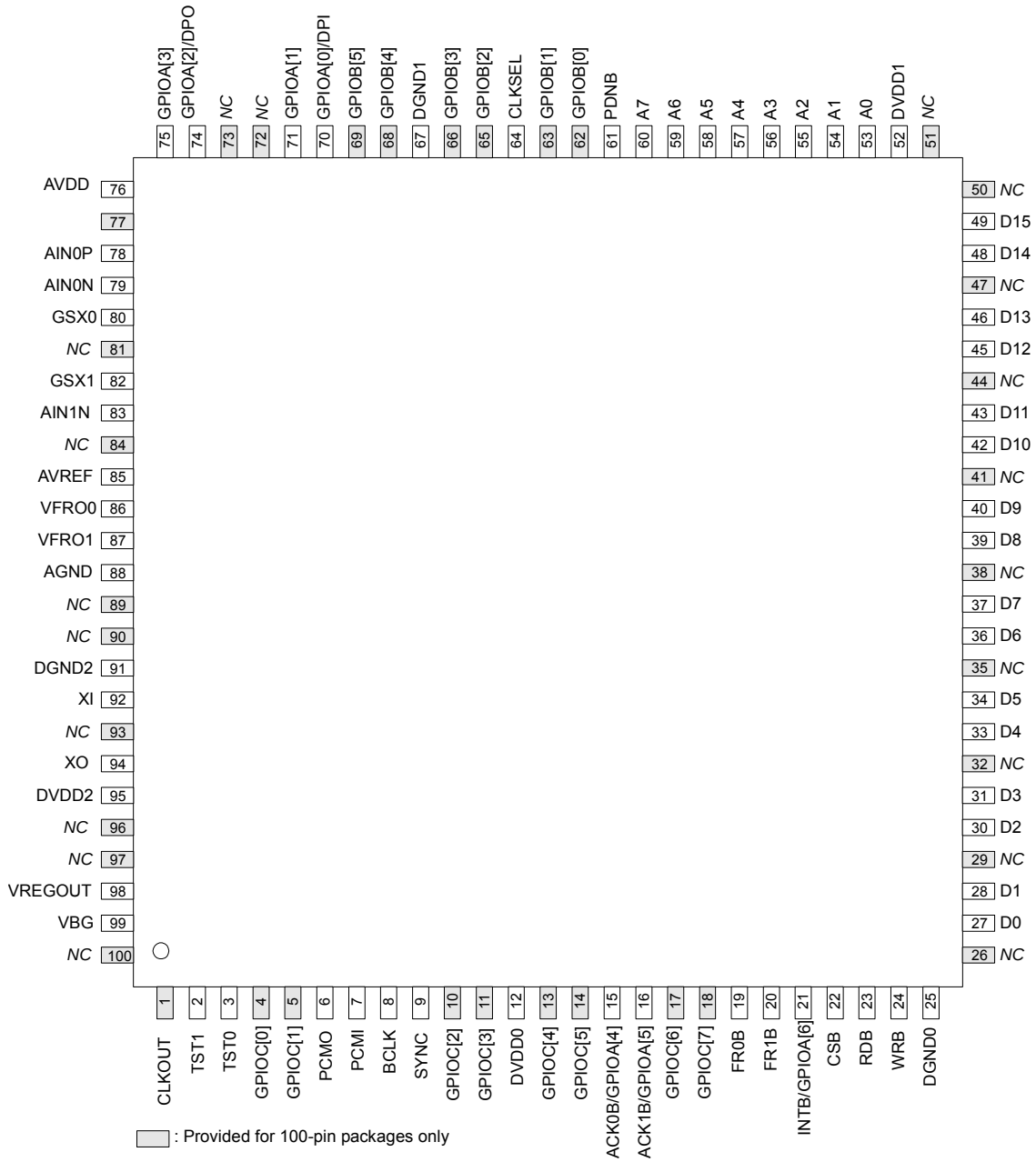
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP



100-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin		Symbol	I/O	When PDNB = "0"	Description
TQFP100	QFP64				
1	—	CLKOUT	O	"L"	12.288 MHz clock output
2	1	TST1	I	"0"	Test control input 1: Normally, input "0".
3	2	TST0	I	"0"	Test control input 0: Normally, input "0".
4	—	GPIOC[0]	I/O	I	General-purpose I/O port C [0]
5	—	GPIOC[1]	I/O	I	General-purpose I/O port C [1]
6	3	PCMO	O	"Hi-z"	PCM data output [Open drain output pin]
7	4	PCMI	I	I	PCM data input
8	5	BCLK	I/O	I	CLKSEL = "0" PCM shift clock input
				"L"	CLKSEL = "1" PCM shift clock output
9	6	SYNC	I/O	I	CLKSEL = "0" PCM synchronous signal 8 kHz input
				"L"	CLKSEL = "1" PCM synchronous signal 8 kHz output
10	—	GPIOC[2]	I/O	I	General-purpose I/O port C[2]
11	—	GPIOC[3]	I/O	I	General-purpose I/O port C[3]
12	7	DVDD0	—	—	Digital power supply
13	—	GPIOC[4]	I/O	I	General-purpose I/O port C[4]
14	—	GPIOC[5]	I/O	I	General-purpose I/O port C[5]
15	8	ACK0B/GPIOA[4]	I/O	I	Transmit buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A[4] (secondary function) [5 V tolerant pin]
16	9	ACK1B/GPIOA[5]	I/O	I	Receive buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A [5] (secondary function) [5 V tolerant pin]
17	—	GPIOC[6]	I/O	I	General-purpose I/O port C [6]
18	—	GPIOC[7]	I/O	I	General-purpose I/O port C [7]
19	10	FR0B (DMARQ0B)	O	"H"	FR0B:(FD_SEL = "0") Transmit buffer frame signal output DMARQ0B: (FD_SEL = "1") Transmit buffer DMA access request signal
20	11	FR1B (DMARQ1B)	O	"H"	FR1B: (FD_SEL = "0") Receive buffer frame signal output DMARQ1B: (FD_SEL = "1") Receive buffer DMA access request signal output
21	12	INTB/GPIOA[6]	I/O	"H"	Interrupt request output (primary function) General-purpose I/O port A [6] (secondary function) [5 V tolerant pin]
22	13	CSB	I	I	Chip select control input
23	14	RDB	I	I	Read control input
24	15	WRB	I	I	Write control input
25	16	DGND0	—	—	Digital ground (0.0 V)

Pin		Symbol	I/O	When PDNB = “0”	Description
TQFP100	QFP64				
26	—	NC	—	—	(Unused)
27	17	D0	I/O	I	Data input-output
28	18	D1	I/O	I	Data input-output
29	—	NC	—	—	(Unused)
30	19	D2	I/O	I	Data input-output
31	20	D3	I/O	I	Data input-output
32	—	NC	—	—	(Unused)
33	21	D4	I/O	I	Data input-output
34	22	D5	I/O	I	Data input-output
35	—	NC	—	—	(Unused)
36	23	D6	I/O	I	Data input-output
37	24	D7	I/O	I	Data input-output
38	—	NC	—	—	(Unused)
39	25	D8	I/O	I	Data input-output. Fix the input to “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
40	26	D9	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
41	—	NC	—	—	(Unused)
42	27	D10	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
43	28	D11	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
44	—	NC	—	—	(Unused)
45	29	D12	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
46	30	D13	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
47	—	NC	—	—	(Unused)
48	31	D14	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
49	32	D15	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
50	—	NC	—	—	(Unused)
51	—	NC	—	—	(Unused)
52	33	DVDD1	—	—	Digital power supply
53	34	A0	I	I	Address input
54	35	A1	I	I	Address input
55	36	A2	I	I	Address input
56	37	A3	I	I	Address input
57	38	A4	I	I	Address input
58	39	A5	I	I	Address input
59	40	A6	I	I	Address input
60	41	A7	I	I	Address input

Pin		Symbol	I/O	When PDNB = “0”	Description
TQFP100	QFP64				
61	42	PDNB	I	“0”	Power-down input “0”: Power-down reset ”1”: Normal operation
62	—	GPIOB[0]	I/O	I	General-purpose I/O port B[0]
63	—	GPIOB[1]	I/O	I	General-purpose I/O port B[1]
64	43	CLKSEL	I	I	SYNC/BCLK input-output control input “0”: SYNC/BCLK are configured to be input “1”: SYNC/BCLK are configured to be output
65	—	GPIOB[2]	I/O	I	General-purpose I/O port B[2]
66	—	GPIOB[3]	I/O	I	General-purpose I/O port B[3]
67	44	DGND1	—	—	Digital ground (0.0 V)
68	—	GPIOB[4]	I/O	I	General-purpose I/O port B[4]
69	—	GPIOB[5]	I/O	I	General-purpose I/O port B[5]
70	45	GPIOA[0]/DPI	I/O	I	General-purpose I/O port A[0] [5 V tolerant pin] Secondary function: Input pin for dial pulse detection
71	46	GPIOA[1]	I/O	I	General-purpose I/O port A[1] [5 V tolerant pin]
72	—	NC	—	—	(Unused)
73	—	NC	—	—	(Unused)
74	47	GPIOA[2]/DPO	I/O	I	General-purpose I/O port A[2] [5 V tolerant pin] Secondary function: Output pin for dial pulse transmission
75	48	GPIOA[3]	I/O	I	General-purpose I/O port A[3] [5 V tolerant pin]
76	49	AVDD	—	—	Analog power supply
77	—	NC	—	—	(Unused)
78	50	AIN0P	I	I	AMP0 non-inverting input
79	51	AIN0N	I	I	AMP0 inverted input
80	52	GSX0	O	“Hi-z”	AMP0 output (10 kΩ driving)
81	—	NC	—	—	(Unused)
82	53	GSX1	O	“Hi-z”	AMP1 output (10 kΩ driving)
83	54	AIN1N	I	I	AMP1 inverted input
84	—	NC	—	—	(Unused)
85	55	AVREF	O	“L”	Analog signal ground (1.4 V)
86	56	VFRO0	O	“Hi-z”	AMP2 output (10 kΩ driving)
87	57	VFRO1	O	“Hi-z”	AMP3 output (10 kΩ driving)
88	58	AGND	—	—	Analog ground (0.0 V)
89	—	NC	—	—	(Unused)
90	—	NC	—	—	(Unused)
91	59	DGND2	—	—	Digital ground (0.0 V)
92	60	XI	I	I	12.288 MHz crystal interface, 12.288 MHz clock input
93	—	NC	—	—	(Unused)
94	61	XO	O	“H”	12.288 MHz crystal interface

Pin		Symbol	I/O	When PDNB = “0”	Description
TQFP100	QFP64				
95	62	DVDD2	—	—	Digital power supply
96	—	NC	—	—	(Unused)
97	—	NC	—	—	(Unused)
98	63	VREGOUT	—	—	Internal regulator voltage output pin (approx. 2.5 V)
99	64	VBG	—	—	Internal regulator reference voltage output pin
100	—	NC	—	—	(Unused)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Analog power supply voltage	AVDD	—		–0.3 to +4.6	V
Digital power supply voltage	DVDD	—		–0.3 to +4.6	V
Analog input voltage	VAIN	Analog pin		–0.3 to AVDD+0.3	V
Digital input voltage	VDIN1	Normal digital pin		–0.3 to DVDD+0.3	V
	VDIN2	5 V tolerant pin	DVDD = 3.0 to 3.6 V	–0.3 to +6.0	V
			DVDD < 3.0 V	–0.3 to DVDD+0.3	V
Output current	IO	—		–20 to +20	mA
Power dissipation	PD	Ta = 60 °C, per package		350	mW
Storage temperature	Tstg	—		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply voltage	AVDD	—	3.0	3.3	3.6	V
Digital power supply voltage	DVDD	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	–20	—	60	°C
Digital high-level input voltage	VIH1	Normal digital pin	0.75 × DVDD	—	DVDD+ 0.3	V
	VIH2	5 V tolerant pin	0.75 × DVDD	—	5.5	V
Digital low-level input voltage	VIL	Digital pin	–0.3	—	0.19 × DVDD	V
Digital input rise time	tIR	Digital pin	—	2	20	ns
Digital input fall time	tIF	Digital pin	—	2	20	ns
Digital output load capacitance	CDL	Digital pin	—	—	50	pF
Digital output load resistance	RDL	Pull-up resistance, PCMO	500	—	—	Ω
AVREF bypass capacitor	Cvref	Between AVREF-AGND	2.2+0.1	—	4.7+0.1	μF
VREGOUT bypass capacitor	Cvout	Between VREGOUT-DGND	—	10+0.1	—	μF
VBG bypass capacitor	CVBG	Between VBG-DGND	—	150	—	pF
Master clock frequency	Fmck	MCK	–0.01%	12.288	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	64	—	2048	kHz
PCM synchronous signal frequency	Fsync	SYNC (at input)	—	8.0	—	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM synchronous timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM synchronous signal width	tWS	SYNC (at input)	1BCLK	—	100	μs

(Note) On power-on/shut-down sequence

For the analog power supply voltage (AVDD) and the digital power supply voltage (DVDD) to be supplied to this LSI, it is recommended that power be applied to them simultaneously. However, if simultaneous power-up is difficult due to the power supply circuit configuration, power them up in the order of DVDD → AVDD.

The power supplies should be shut down in the reverse order of power-on sequence.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	ISS	Standby state (PDNB = ”0”, DVDD = AVDD=3.3 V, Ta = 25°C)	—	200	500	μA
	IDD1	Operating status 1 Speech CODEC activated/PCM I/F not used SC_EN = ”1”, AFEA_EN = ”0”, AFEB_EN = ”1”, XI, XO: 12.288 MHz crystal connected	—	45	55	mA
	IDD2	Operating status 2 Speech CODEC activated/PCM I/F used SC_EN = ”1”,PCMI1_EN = ”1”, PCMO1_EN = ”1”, AFEA_EN=”0”, AFEB_EN=”0” XI, XO: 12.288 MHz crystal connected	—	50	65	mA
Digital input pin Input leakage current	IIH	Vin = DVDD	—	0.01	10	μA
	IIL	Vin = DGND	–10	–0.01	—	μA
Digital I/O pin Output leakage current	IOZH	Vou = DVDD	—	0.01	10	μA
	IOZL	Vout = DGND	–10	—	—	μA
High-level output voltage	VOH	Digital input pins, I/O pin IOH = 4.0 mA IOH = 0.5 mA (XO pin) IOH = 1 2.0 mA (CLKOUT pin)	0.78 × DVDD	—	—	V
Low-level output voltage	VOL1	Digital output pins, I/O pin IOL = –4.0 mA IOL = –0.5 mA (XO pin) IO = –12.0 mA (CLKOUT pin)	—	—	0.4	V
	VOL2	Open drain output pins IOL = –12.0 mA	—	—	0.4	V
Input capacitance (*1)	CIN1	Input pins	—	6	—	pF
	CIN2	I/O pins	—	10	—	pF

*1 Design guaranteed value

Analog Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1 ,2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input resistance (*1)	RIN	AIN0N, AIN0P, AIN1N	10	—	—	MΩ
Output load resistance	RL	GSX0, GSX1, VFRO0, VFRO1	10	—	—	kΩ
Output load capacitance	CL	Analog output pins	—	—	50	pF
Offset voltage	VOF	VFRO0, VFRO1	–40	—	40	mV
Output voltage level (*2)	VO	GSX0, GSX1, VFRO0, VFRO1 RL = 10kΩ, AMP input 1.3 Vpp	1.158	1.3	1.458	Vpp

*1 Design guaranteed value

*2 –7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 Vpp

AC Characteristics in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)				
Transmit frequency characteristics	LT1	0 to 60	0	25	—	—	dB
	LT2	300 to 3000		–0.15	—	0.20	dB
	LT3	1020		Reference			—
	LT4	3300		–0.15	—	0.80	dB
	LT5	3400		0	—	0.80	dB
	LT6	3968.75		13	—	—	dB
Receive frequency characteristics	LR2	0 to 3000	0	–0.15	—	0.20	dB
	LR3	1020		Reference			—
	LR4	3300		–0.15	—	0.80	dB
	LR5	3400		0	—	0.80	dB
	LR6	3968.75		13	—	—	dB
Transmit signal-to-noise ratio (*1)	SDT1	1020	3	35	—	—	dBp
	SDT2		0	35	—	—	dBp
	SDT3		–30	35	—	—	dBp
	SDT4		–40	28	—	—	dBp
	SDT5		–45	23	—	—	dBp
Receive signal-to-noise ratio (*1)	SDR1	1020	3	35	—	—	dBp
	SDR2		0	35	—	—	dBp
	SDR3		–30	35	—	—	dBp
	SDR4		–40	28	—	—	dBp
	SDR5		–45	23	—	—	dBp
Transmit inter-level loss errors	GTT1	1020	3	–0.2	—	0.2	dB
	GTT2		–10	Reference			—
	GTT3		–40	–0.2	—	0.2	dB
	GTT4		–50	–0.6	—	0.6	dB
	GTT5		–55	–1.2	—	1.2	dB
Receive inter-level loss errors	GTR1	1020	3	–0.2	—	0.2	dB
	GTR2		–10	Reference			—
	GTR3		–40	–0.2	—	0.2	dB
	GTR4		–50	–0.6	—	0.6	dB
	GTR5		–55	–1.2	—	1.2	dB
Idle channel noise (*1)	NIDLT	—	Analog input = AVREF	—	—	–70	dBm0p
	NIDLR	—	PCMI = ”1”	—	—	–70	dBm0p
Transmit absolute level (*2)	AVT	1020	0	0.285	0.320	0.359	Vrms
Receive absolute level (*2)	AVR	1020	0	0.285	0.320	0.359	Vrms

*1 P-message weighted filter used

*2 0.320 Vrms = 0 dBm0 = –7.7 dBm (600Ω)

AC Characteristics (Gain Setting) in Speech CODEC = G.711 (μ-law) mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/receive gain setting accuracy	GAC	For all gain set values	–1.0	—	1.0	dB

AC Characteristics (Tone Output) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	For all frequency set values	–1.5	—	1.5	%
Output level	oLEV	For all gain set values	–2.0	—	2.0	dB

AC characteristics (DTMF Detector and Other Detectors) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

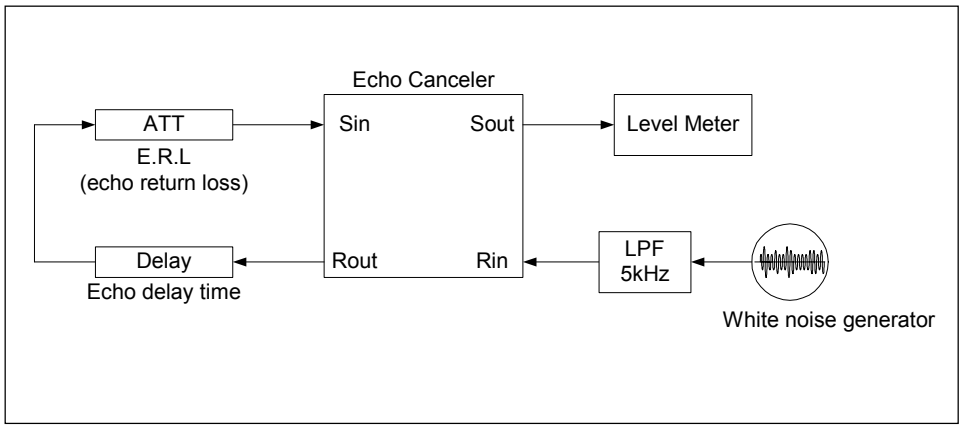
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection level accuracy	dLAC	For all detection level set values	–2.5	—	2.5	dB

AC characteristics (Echo Canceler)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	—	—	35	—	dB
Erasable echo delay time	tECT	—	—	—	32	ms

Measuring method



Timings of PDNB, XO, and AVREF

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down signal pulse width	tPDNB	PDNB pin	250	—	—	μs
AVDD supply delay time	tAVDDON	—	0	—	—	ns
Oscillation activation time	txtal	—	—	—	20	ms
AVREF rise time	tAVREF	AVREF = 1.4 (90%) C5 = 4.7 μF, C6 = 0.1 μF (See Figure 9)	—	—	600	ms
		AVREF = 1.4 (90%) C5 = 2.2 μF, C6 = 0.1 μF (See Figure 9)	—	—	300	ms

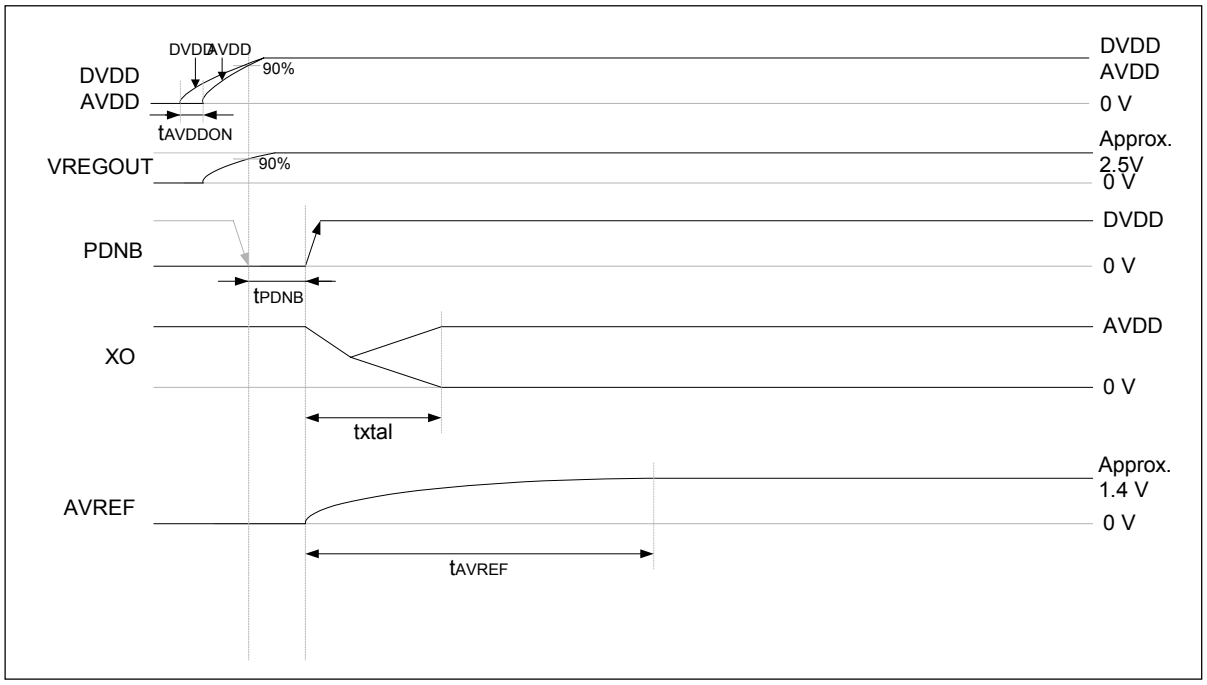


Figure 1 Timings of PDNB, XO, and AVREF

(Note)
The capacitance of the AVREF capacitor (C5) affects the AVREF rise time and analog characteristics. If weight is given to the analog characteristics, specify 4.7 μF, and if it is given to the AVREF rise time, specify 2.2 μF. The electrical characteristics for the analog characteristics that are described above are guaranteed in both capacitances.

PCM interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	fBCLK	CDL = 20 pF (during output)	–0.1%	2.048	+0.1%	MHz
Bit clock duty ratio	dBCLK	CDL = 20 pF (during output)	45	50	55	%
Synchronous signal frequency	fSYNC	CDL = 20 pF (during output)	–0.1%	8	+0.1%	kHz
Synchronous signal duty ratio	dSYNC 1	CDL = 20 pF (during output) BCLK = 2.048 MHz At output	45	50	55	%
Transmit/receive synchronous timing	tBS	BCLK to SYNC (during output)	100	—	—	ns
	tSB	SYNC to BCLK (during output)	100	—	—	ns
Input setup time	tDS	PCMI pin	50	—	—	ns
Input hold time	tDH		50	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up resistance RDL = 500Ω CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
Digital output hold time	tXD2		—	—	100	ns
	tXD3		—	—	100	ns

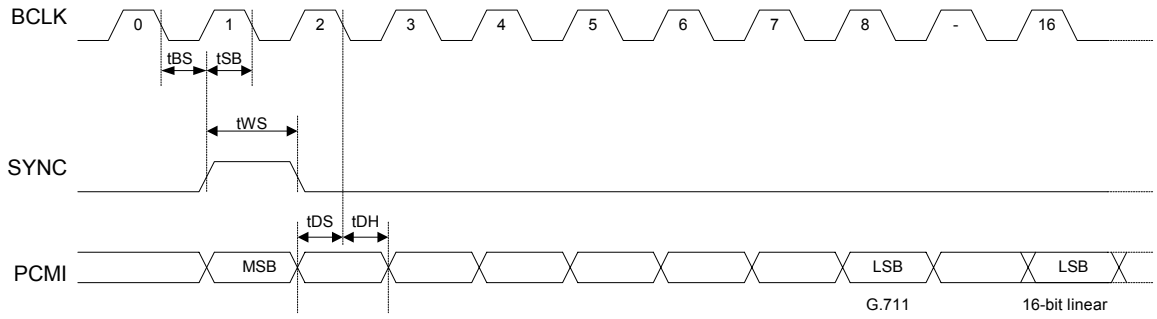


Figure 2 PCM Interface Input Timing (Long Frame)

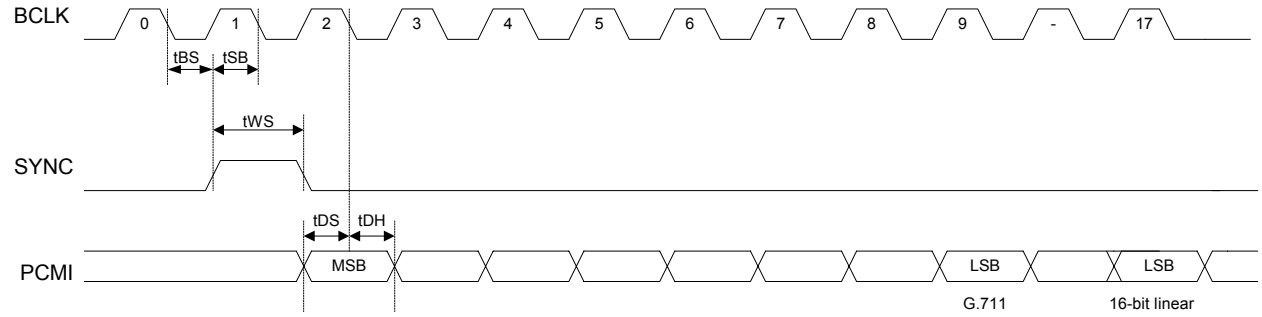


Figure 3 PCM Interface Input Timing (Short Frame)

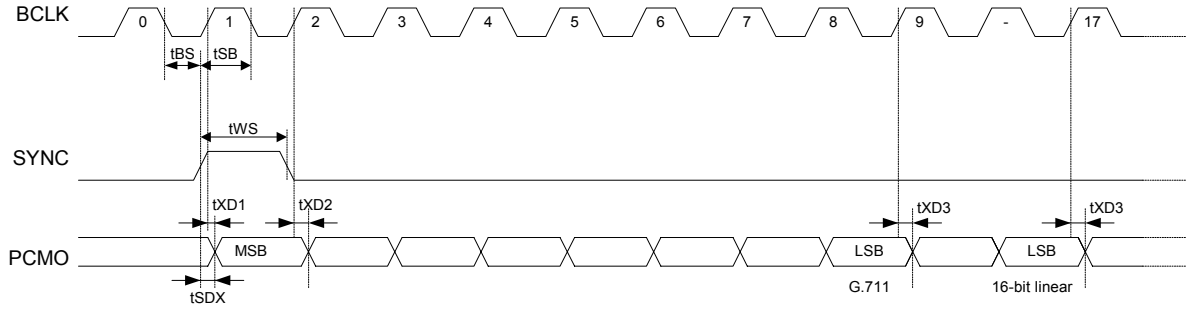


Figure 4 PCM Interface Output Timing (Long Frame)

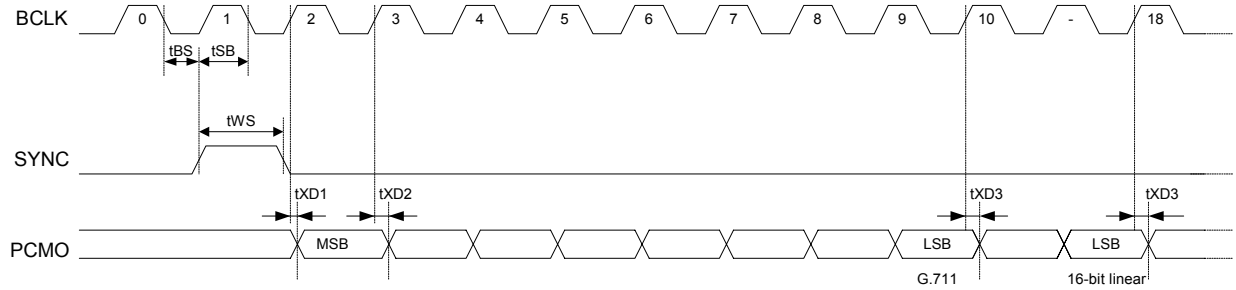


Figure 5 PCM Interface Output Timing (Short Frame)

Control Register Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta= –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address setup time (at Read)	tRAS	CL = 50 pF	10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD		10	—	—	ns

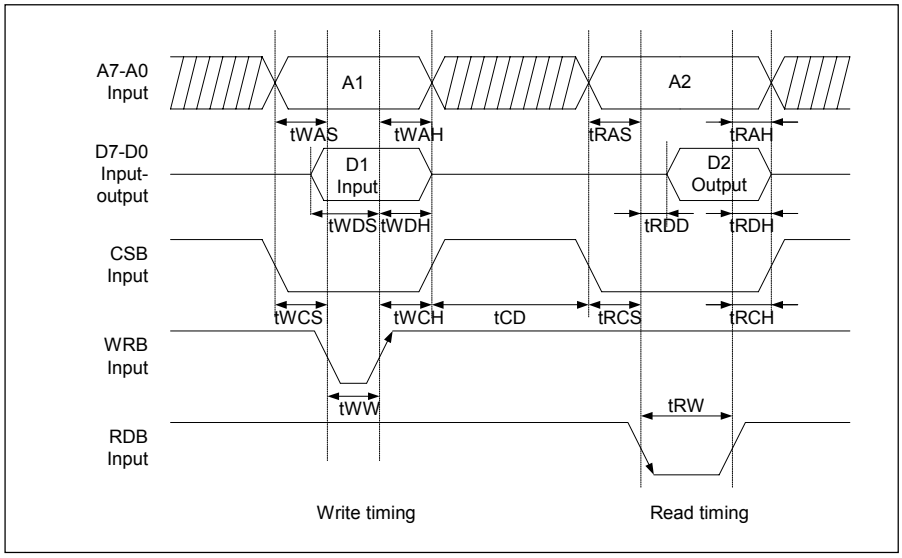


Figure 6 Control Register Interface

Transmit/Receive Buffer Interface (Frame Mode)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

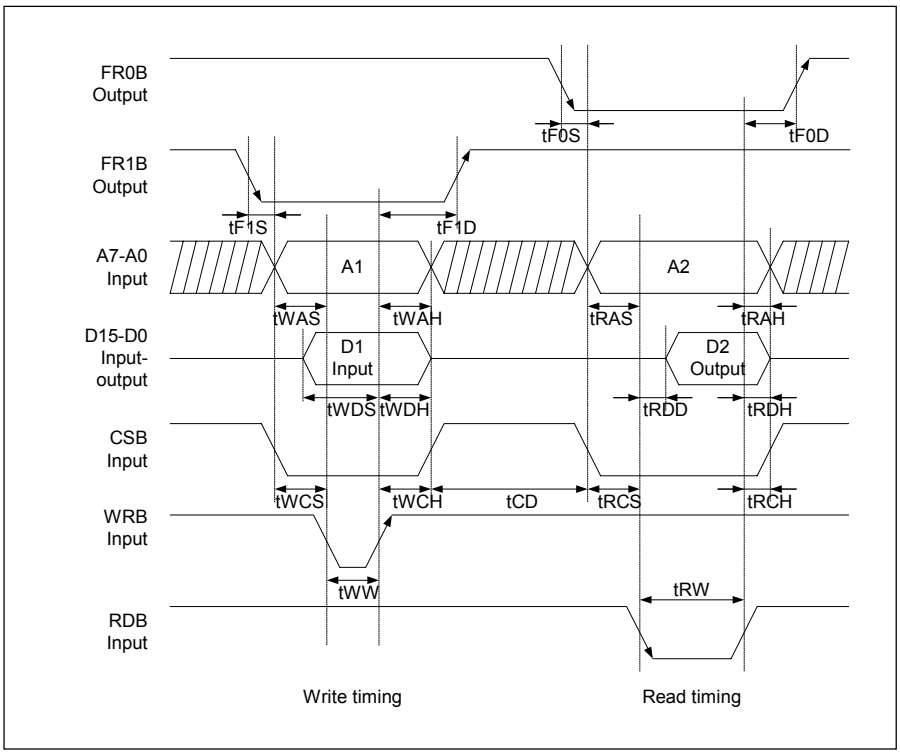


Figure 7 Transmit/Receive Buffer Interface (Frame Mode)

Transmit/Receive Buffer Interface (DMA Mode)

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	30	ns
	tDR1FD		—	—	30	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK0B setup time	tAK0S		10	—	—	ns
ACK0B hold time	tAK0H		0	—	—	ns
ACK1B setup time	tAK1S		10	—	—	ns
ACK1B hold time	tAK1H		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	30	ns
	tDR0FD		—	—	30	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns

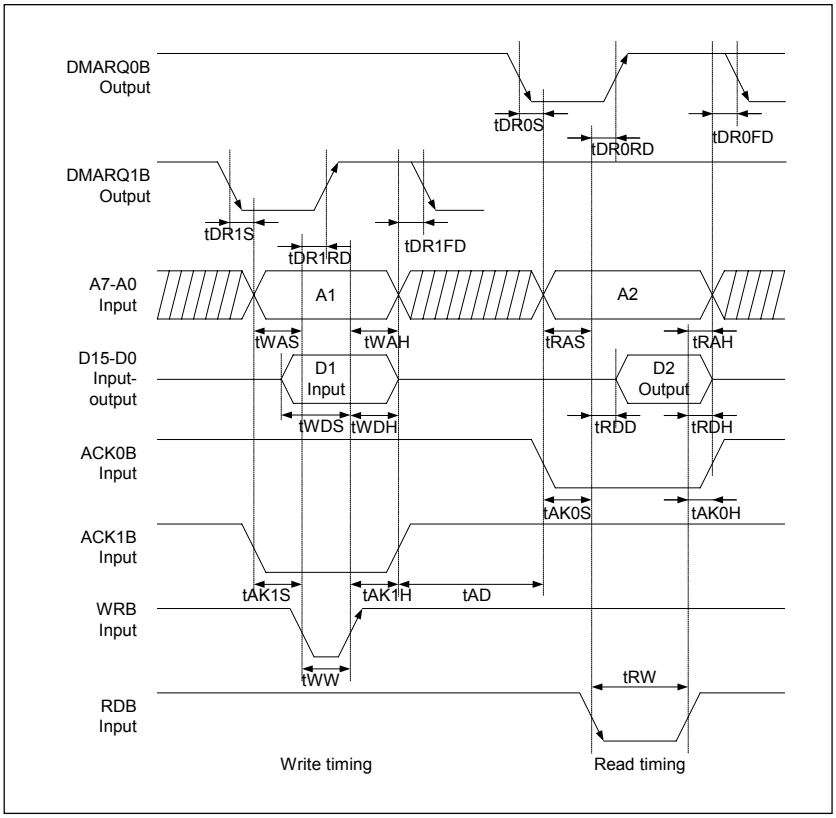


Figure 8 Transmit/Receive Buffer Interface (DMA Mode)

PIN FUNCTIONAL DESCRIPTION

AIN0N, AIN0P, GSX0, AIN1N, and GSX1

These are transmit analog input and transmit gain adjustment pins. AIN0N and AIN1N are connected to inverted input pins of internal transmission amplifiers AMP0 and AMP1, and AIN0P is connected to a noninverting input pin of AMP0. GSX0 and GSX1 are connected to output pins of AMP0 and AMP1. See Figure 9 for the gain adjustment.

At power down (PDNB = "0" or SPDN = "1"), outputs of GSX0 and GSX1 are in a high impedance state. When the application does not use AMP0, short-circuit GSX0 and AIN0N and connect AIN0P with AVREF. When not using AMP1, short-circuit GSX1 and AIN1N.

VFRO0 and VFRO1

These are receive analog output pins. VFRO0 and VFRO1 are connected to output pins of amplifiers AMP2 and AMP3. Output of output signals, VFRO0 and VFRO1, can be selected using the VFRO0 selection register (VFRO0_SEL) and VFRO1 selection register (VFRO1_SEL): When output is selected ("1"), the receive signal is output and when output is not selected ("0"), AVREF (about 1.4 V) is output. In power down mode, these output pins are set to a high impedance state. It is recommended to use output signals through a DC coupling capacitor.

(Note)

If output selection is changed while the conversation is in progress, a micronoise is generated. Therefore, it is recommended to select output before starting a call and then start a call.

Before canceling reset or resetting, it is recommended to select output of VFRO0 and VFRO1 to the AVREF output side.

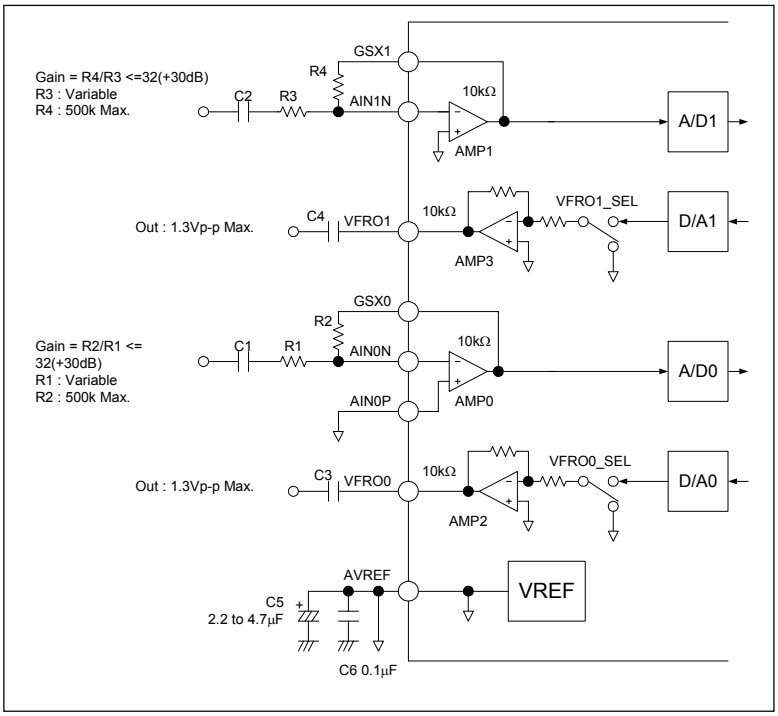
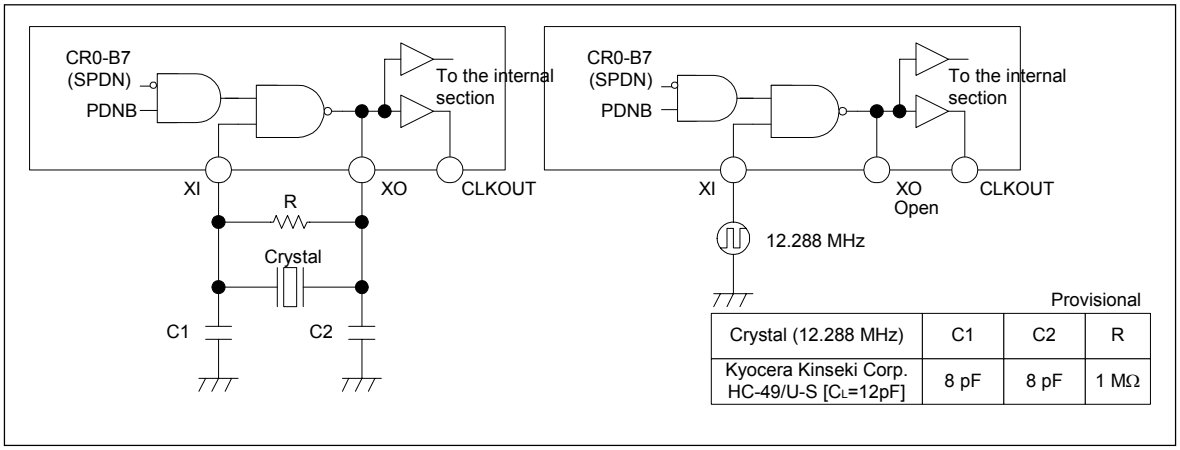


Figure 9 Analog Interface

AVREF
This is an output pin of an analog signal ground potential. With the output potential of about 1.4 V, insert bypass capacitors of 2.2 to 4.7 μF (aluminum electrolysis type) and 0.1 μF (ceramic type) in parallel. AVREF outputs 0.0 V at power down. AVREF starts being powered up after power-down reset, the system restarts from (PDNB = "1" and SPDN = "0").

XI and XO
These are the master clock input pin (XI) and the crystal connection pins for the master clock (XI and XO).
Oscillation stops at power down by PDNB or software power down by SPDN. Oscillation starts after power-down is reset and the clock is supplied to the LSI internal section after oscillation stabilization delay time has elapsed (about 21.3 ms). Figure 10 shows a master clock input example.



Provisional

Crystal (12.288 MHz)	C1	C2	R
Kyocera Kinseki Corp. HC-49/U-S [C_L=12pF]	8 pF	8 pF	1 MΩ

Figure 10 Example of an Oscillation Circuit and Clock Input

CLKOUT
This is a 12.288 MHz master clock output pin. (Provided for 100-pin packages only)
Since output is disabled in the initial state, set the 12.288 MHz clock output enable control register (CLKOUT_EN) to "1" when clock output is required.

PDNB
This is a power-down control input pin. A power-down state can be set by setting this pin to "0". This pin also functions as an LSI reset pin. To prevent an LSI operation error, use PDNB for the initial power-down reset after power is applied. To put the LSI into a power-down state, fix PDNB to "0" for 250 μs or more.
LSI power-down reset can be performed by setting the software power down reset control register SPDN to "0" → "1" → "0".
Power-down is released, the initial mode display register (READY) is set to "1" after 200 ms, and various function setting modes (initial modes) are entered.
See Figure 1 for the timings of PDNB, AVREF, XO, and the initial mode.

(Note)
Turn on the power in a power-down state by PDNB.
When using the LSI by inputting a master clock to the XI pin, first maintain the power-down state (PDNB = 0) until power is applied to the digital power supply (DVD0, 1, and 2) and the analog power supply (AVDD) (90% or more) and the master clock is input to the XI pin, then release the power-down state (PDNB = 0 → 1) . In this case also, fix PDNB to "0" for 250 μs or more.

DVDD0, DVDD1, DVDD2, and AVDD
These are power supply pins. DVDD0, DVDD1, and DVDD2 are connected to the power supply of a digital circuit and AVDD is connected to a power supply of an analog circuit. Connect these pins near the LSI and insert bypass capacitors of 10 μF (electrolysis type) and 0.1 μF (ceramic type) between DGND and AGND in parallel.

DGND0, DGND1, DGND2, and AGND
These are ground pins. DGND0, DGND1, and DGND2 are connected to grounds of digital circuits and AGND is connected to a ground of an analog circuit. Connect these pins near the LSI.

VREGOUT
This is an output pin of an internal regulator voltage (about 2.5 V).
Connect a capacitor of about 0.1 μF (ceramic type) in parallel to about 10 μF (ceramic or tantalum type) between this pin and a ground pin.

VBG
This is a reference output pin for an internal regulator.
Connect a laminated ceramic capacitor of about 150 pF between this pin and a ground pin.

TST0 and TST1
These are input pins for testing. At normal use, input “0”.

INTB/GPIOA[6]

Primary function: INTB

This in an interrupt request output pin.

When the interrupt cause is changed, this pin outputs a "L" level for about 1.0 μs. When the interrupt factor is not changed, "H" is output. The interrupt factor can be checked by reading CR16-CR22. Table 1 lists the interrupt causes.

The interrupt causes can be masked individually in the internal memory (interrupt cause mask control).

Table 1 Interrupt Causes

CR	BIT	Register name	Rising edge	Falling edge	Remarks
CR16	B2	FSK receive overrun error notification register (FDET_OER)	○	×	
	B1	FSK receive framing error notification register (FDET_FER)	○	×	
	B0	FSK receive data read request notification register (FDET_RQ)	○	×	
CR17	B0	FSK output data setting completion flag (FGEN_FLAG)	×	○	
CR18	B0	Timer overflow display register (TMOVF)	○	×	
CR19	B7	DSP status register (DSP_ERR)	○	×	
	B4	TONE1 detector detection status register (TONE1_DET)	○	○	
	B3	TONE0 detector detection status register (TONE0_DET)	○	○	
	B2	TGEN1 execution flag display register (TGEN1_EXFLAG)	○	○	
	B1	TGEN0 execution flag display register (TGEN0_EXFLAG)	○	○	
CR20	B6	Dial pulse detector detection status register (DP_DET)	○	○	
	B4	DTMF detector detection status register (DTMF_DET)	○	○	
	B3-B0	DTMF code display register (DTMF_CODE[3:0])	○	○	
CR21	B3	CH2 transmit error status register (TXERR_CH2)	○	○	
	B2	CH1 transmit error status register (TXERR_CH1)	○	○	
	B1	CH2 transmit request notification register (FR0_CH2)	○	×	
	B0	CH1 transmit request notification register (FR0_CH1)	○	×	
CR22	B3	CH2 receive error status register (RXERR_CH2)	○	○	
	B2	CH1 receive error status register (RXERR_CH1)	○	○	
	B1	Receive invalid write error notification register (RXBW_ERR)	○	○	
	B0	Receive request notification register (FR1)	○	×	

○: With INTB interrupt generation function ×: Without INTB interrupt generation function

Secondary function: GPIOA[6]

When the primary function/secondary function selection register (GPFA[6]) of GPIOA[6] is set to "1", this pin functions as a general-purpose I/O port GPIOA[6].

A0-A7
These are address input pins for accessing a frame/DMA/control register. Each address is as follows.

Transmit buffer (TX Buffer)
A7-A0 = 80h
Receive buffer (RX Buffer)
A7-A0 = 81h
Control register (CR)
See Tables 5 to 8 for the addresses.

D0-D15
These are data I/O pins for accessing a frame/DMA/control register. Since these pins are I/O pins, connect pull-up resistors. When an 8-bit bus access is selected in the MCU interface data width selection register (BW_SEL), pins D0-D7 are enabled. When using the pins with 8-bit bus access (BW_SEL = "1"), fix the input of high-order D8-D15 to either "0" or "1" since they are constantly in an input state.

CSB
This is a chip select input pin for accessing a frame/control register.

RDB
This is a read enable input pin for accessing a frame/DMA/control register.

WRB
This is a write enable input pin for accessing a frame/DMA/control register.

FR0B (DMARQ0B)

- FR0B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This is a transmit frame output pin that outputs data when the transmit buffer for frame access becomes full. When the transmit buffer becomes full, the pin outputs "L" and retains "L" until the specified number of words are read from the MCU.

- DMARQ0B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This is a DMA request output pin that outputs data when the transmit buffer for DMA access becomes full. When the transmit buffer becomes full, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK0B = "0") and the fall of a read enable signal (RDB = "1" → "0") are received from the MCU side. This operation is repeated until the specified number of words are read from the MCU.

FR1B (DMARQ1B)

- FR1B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This receive frame output pin outputs data when the receive buffer for frame access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and retains "L" until the specified number of words are written from the MCU.

- DMARQ1B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This a DMA request output pin that outputs data when the receive buffer for DMA access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK1B = "0") and the fall of a write enable signal (WRB = "1" → "0") are received from the MCU side. This opeation is repeated until the specified number of words are written from the MCU side.

ACK0B/GPIOA[4]

Primary function: ACK0B
This is a DMA acknowledgment input pin for DMARQ0B for transmit buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using the pin in frame mode (FD_SEL = "0"), fix this pin to "1".
Secondary function: GPIOA[4]
When the primary function/secondary function registration register (GPFA[4]) of GPIOA[4] is set to "1", the pin functions as a general-purpose I/O port GPIOA[4].

ACK1B/GPIOA[5]

Primary function: ACK0B
This is a DMA acknowledgment input pin for DMARQ1B for receive buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using this pin in frame mode (FD_SEL = "0"), fix this pin to "1".
Secondary function: GPIOA[5]
When the primary function/secondary function registration register (GPFA[5]) of GPIOA[5] is set to "1", the pin functions as a general-purpose I/O port GPIOA[5].

GPIOA[0], GPIOA[1], GPIOA[2], and GPIOA[3]

These are general-purpose I/O ports A[3:0].
However, the following secondary functions are assigned to GPIOA[0] and GPIOA[2].
Secondary function of GPIOA[0]: Input pin (DPI) of a dial pulse detecter (DPDET)
Secondary function of GPIOA[2]: Output pin (DPO) of a dial pulse transmitter (DPGEN)

GPIOB[5:0]
This is a general-purpose I/O port B[5:0]. (Provided for 100-pin packages only.)

GPIOC[7:0]
This is a general-purpose I/O port C[7:0]. (Provided for 100-pin packages only.)

CLKSEL
This is an input-output control input pin of SYNC and BCLK. The pin controls input when it is set to "0" and output when it is set to "1".

SYNC
This is a 8 kHz synchronous signal I/O pin of PCM signals. When CLKSEL is "0", constantly input an 8 kHz clock synchronized with BCLK. When CLKSEL is "1", this pin outputs an 8 kHz clock synchronized with BCLK. When the SYNC frame control register (SYNC_SEL) is "0", long frame synchronization is specified and when the register is "1", short frame synchronization is specified.

BCLK
This is a shift clock I/O pin of a PCM signal.
When CLKSEL is "0", clock input synchronized with SYNC is necessary. When G.711 is selected, input a clock of 64 kHz to 2.048 MHz and when 16-bit linear is selected, input a clock of 128 kHz to 2.048 MHz. When CLKSEL is "1", this pin outputs a clock of 2.048 MHz synchronized with SYNC.

(Remarks) Table 2 shows the input-output control of SYNC and BCLK and the frequencies.

Table 2 SYNC and BCLK Input-Output Control

CLKSEL	SYNC	BCLK	Remarks
"0"	Input (8 kHz)	Input (64 kHz to 2048 kHz)	Always input a clock after start of power supply. When G.711 is selected, input a clock of 64 kHz to 2.048 MHz. When 16-bit linear is selected, input a clock of 128 kHz to 2.048 MHz.
"1"	Output (8 kHz)	Output (2.048 MHz)	At power down, "L" is output.

PCMO
This is a PCM signal output pin. A PCM signal is output synchronized with the rise of BCLK or SYNC.
For the output from PCMO, data is output to only the applicable time slot section according to the selected coding format and the setting of the time slot position and other sections are set to a high-impedance state. If a PCM interface is not used, PCMO is set to a high impedance state.

(Note)
Be sure to connect a pull-up resistor externally to the PCMO pin, because the pin is an open drain output pin.
Do not use a pull-up voltage greater than the digital power supply voltage (DVDD).

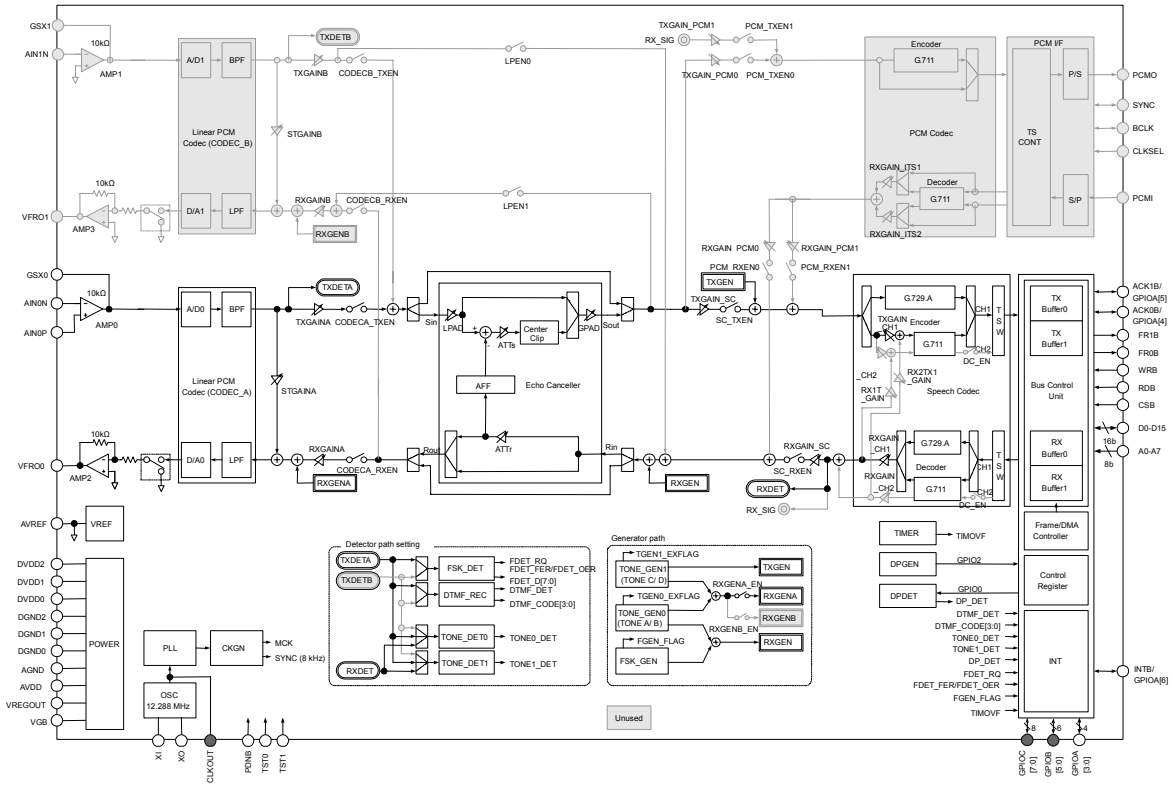
PCMI
This is a PCM signal input pin. The signal is shifted at falling of BCLK and is input from MSB.
If a PCM interface is not used, fix the input to "0" or "1".

FUNCTIONAL DESCRIPTION

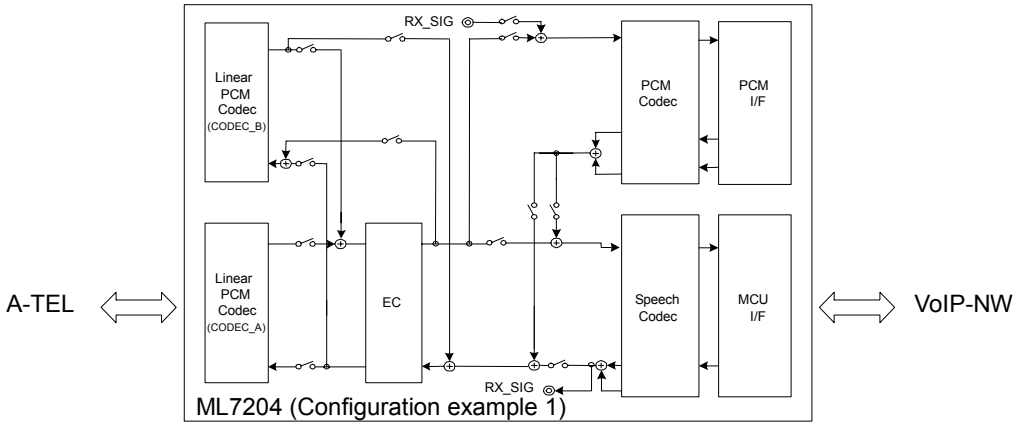
Transmit and receive buffers

CONFIGURATION EXAMPLES

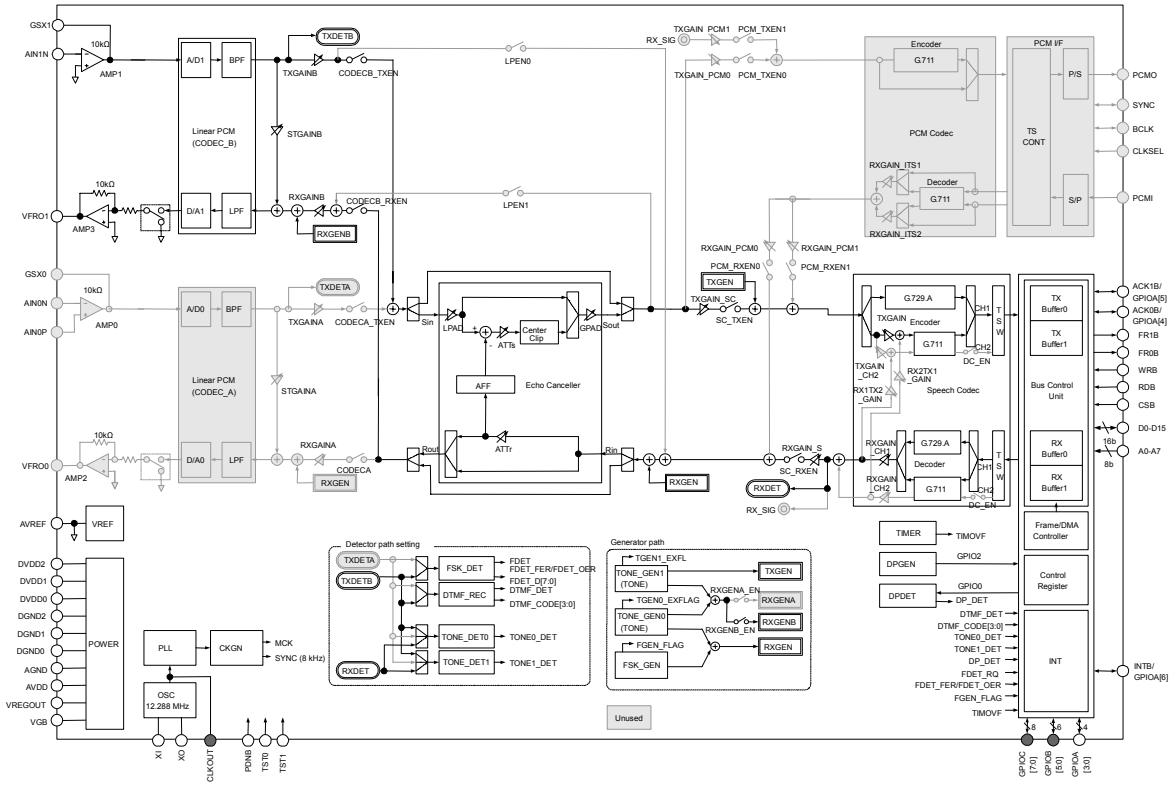
Configuration Example 1 (Basic Call, CODEC_A)



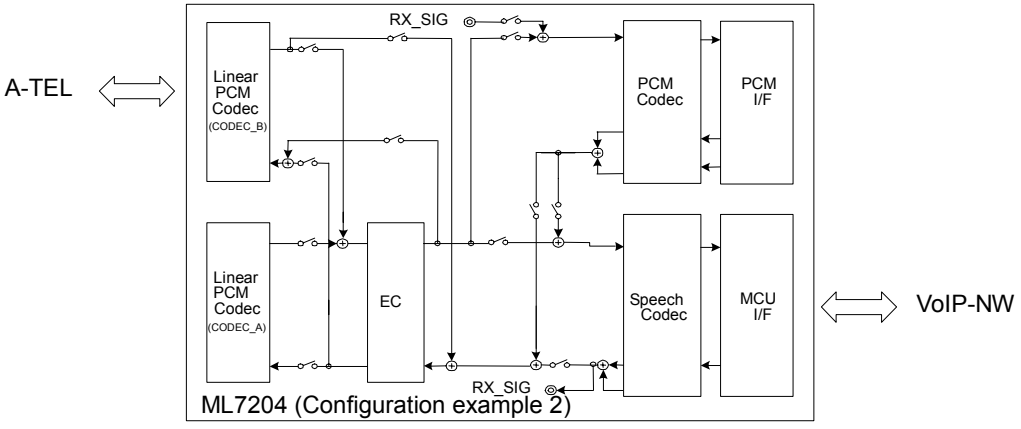
This example shows the configuration for making calls with an analog telephone set (A-TEL) on the NW side by connecting the analog telephone interface on the Linear PCM CODEC_A side.



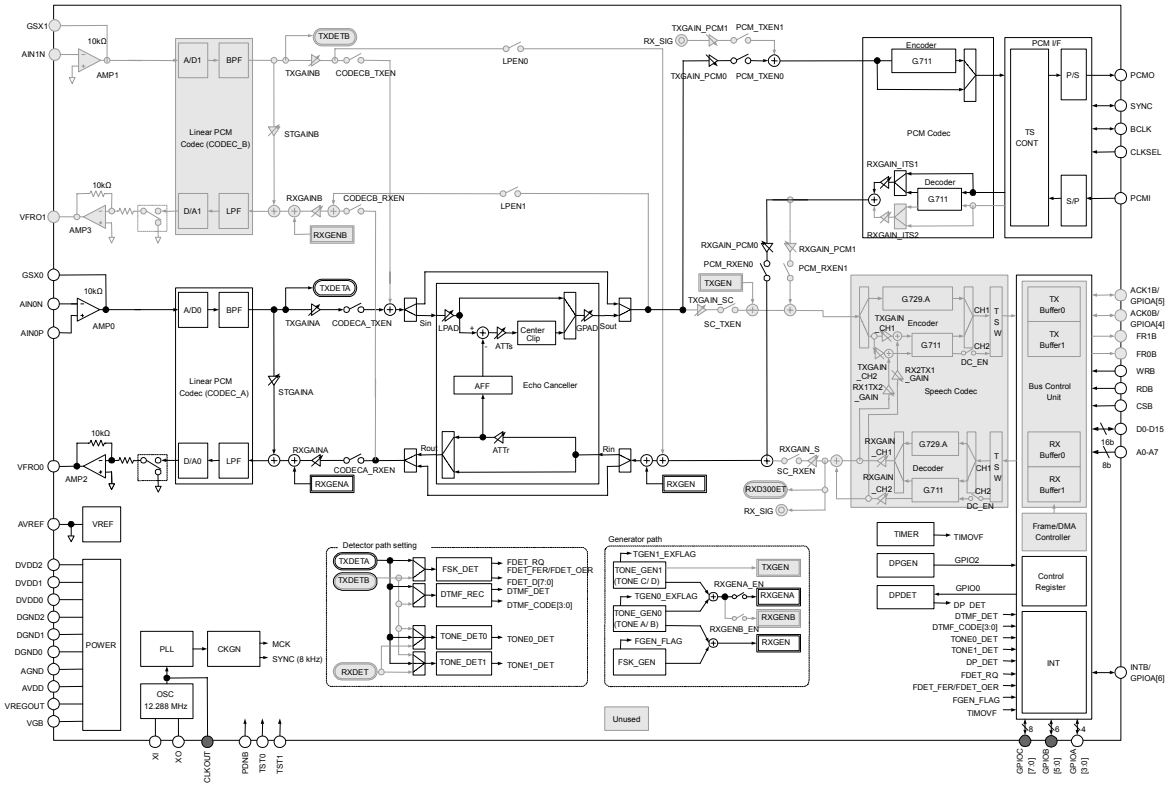
Configuration Example 2 (Basic Call, CODEC_B)



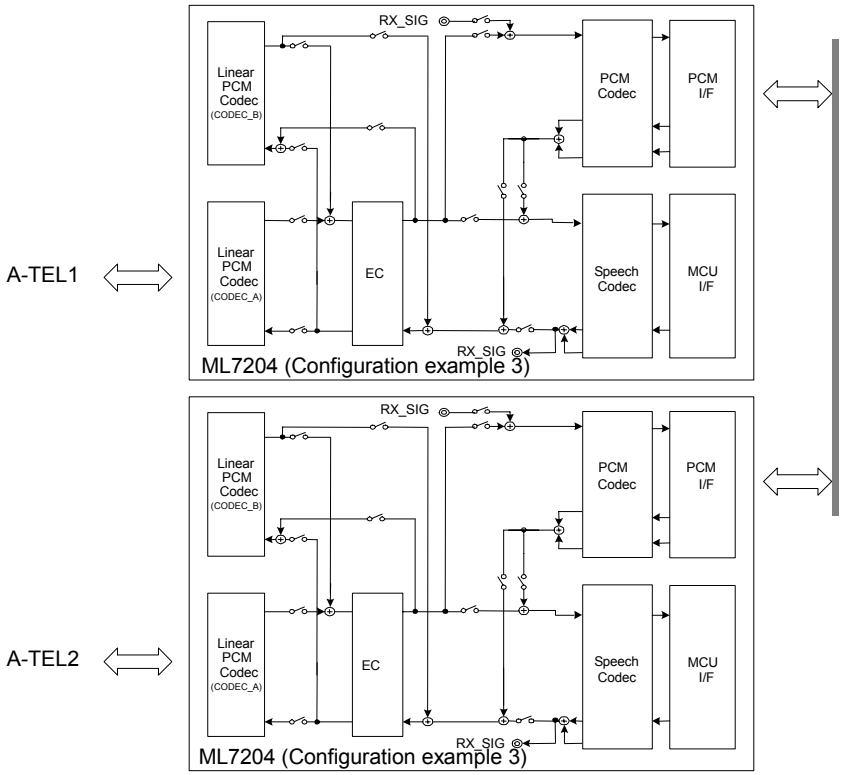
This example shows the configuration for making calls with an analog telephone set (A-TEL) on the NW side by connecting the analog telephone interface on the Linear PCM CODEC_B side.



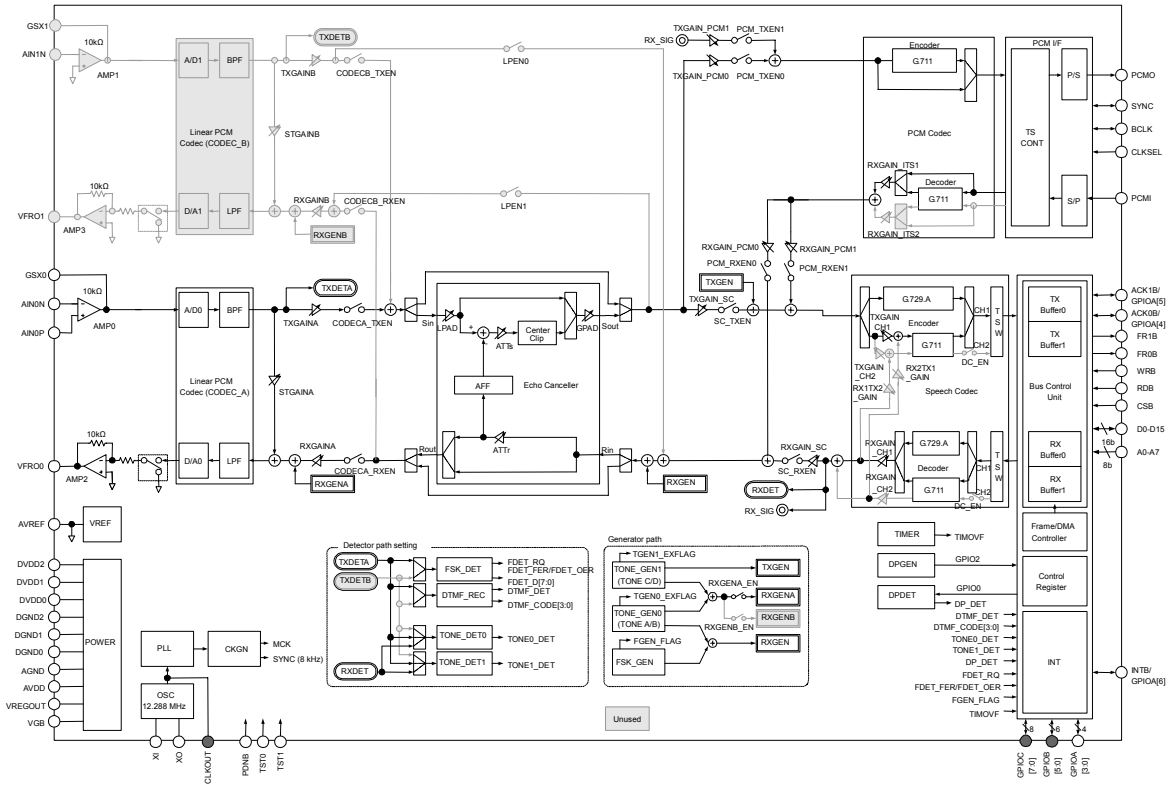
Configuration Example 3 (Calling Using Extension with PCM)



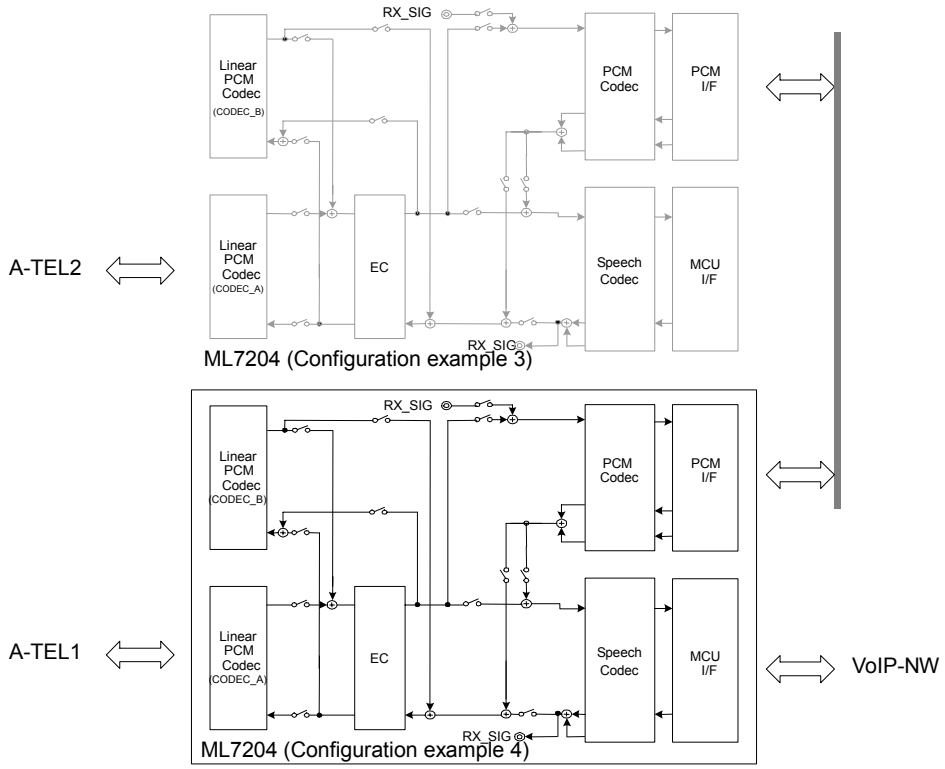
This example shows the configuration for making calls using extension between two analog telephone sets (A-TEL1 and A-TEL2) on the equipment that has two or more analog telephone interface ports.



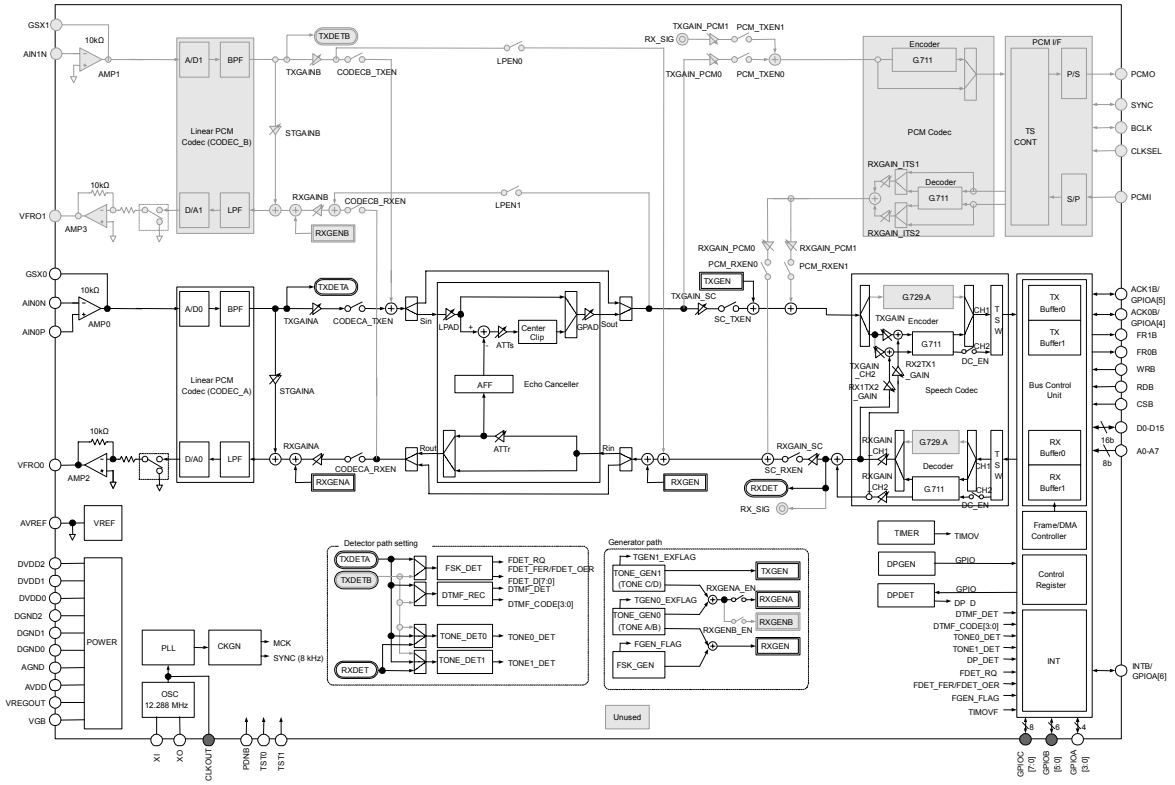
Configuration Example 4 (Three-Way Calling: Terminal Side [Two Parties] – NW Side [One Party])



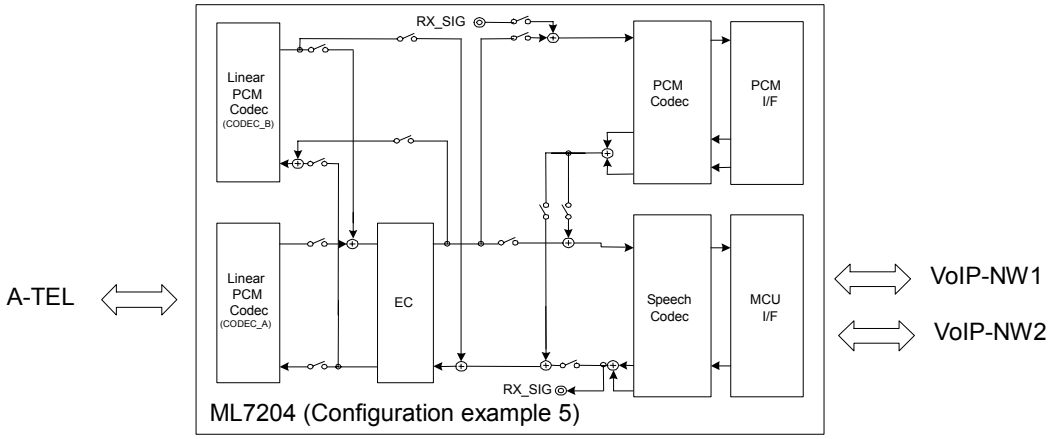
This example shows the configuration for making three-way calling between the terminal side (two parties) and the VoIP NW side (one party).



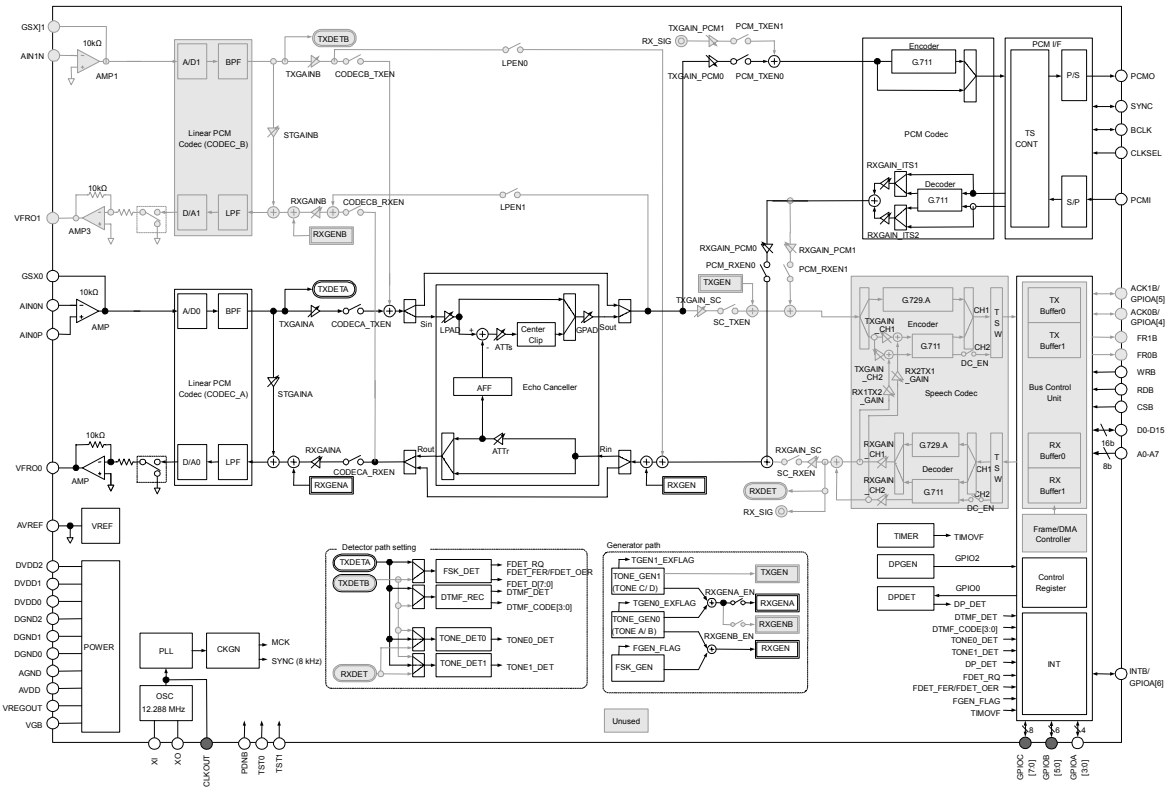
Configuration Example 5 (Three-Way Calling: Terminal Side [One Party] – NW Side [Two Parties])



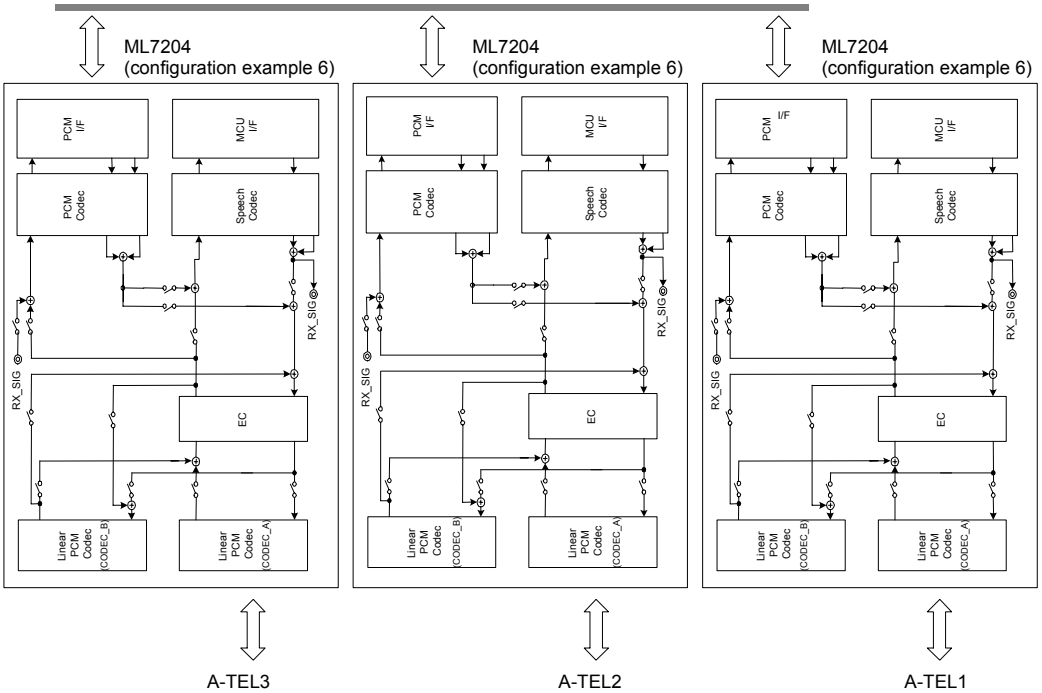
This example shows the configuration for making three-way calling between the terminal side (one party) and VoIP NW side (two parties).



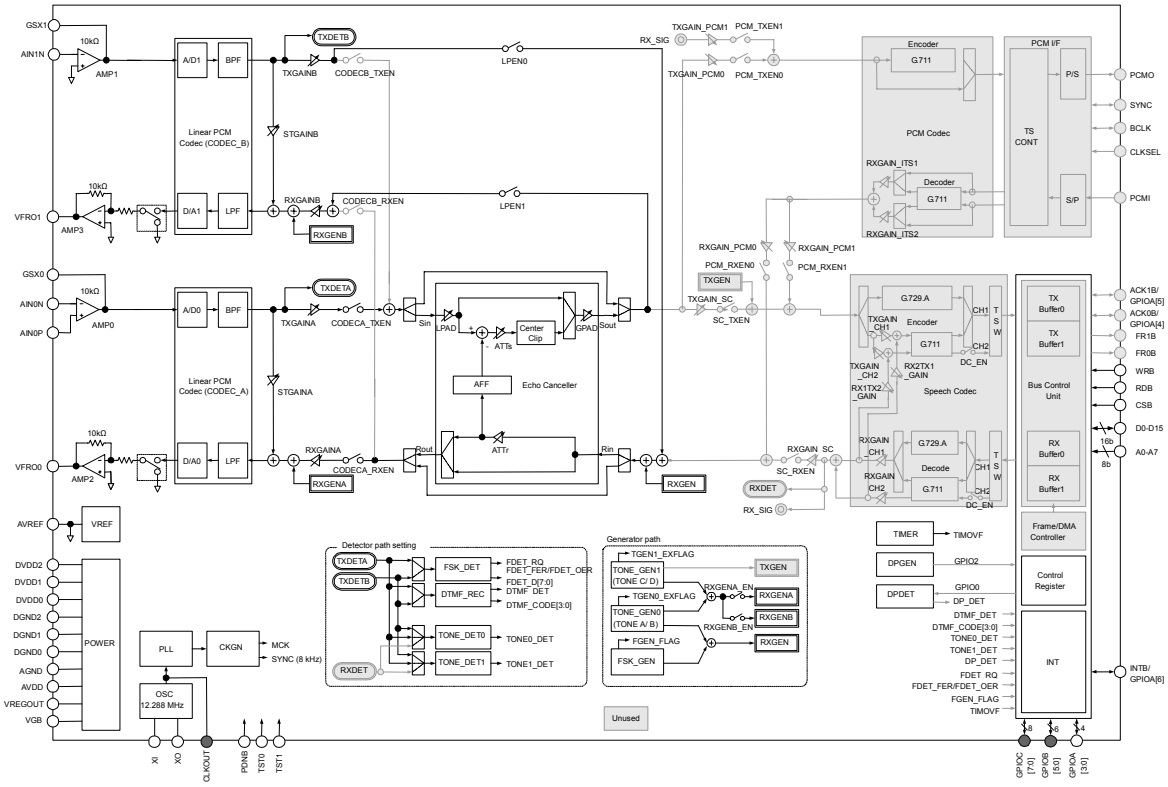
Configuration Example 6 (Three-Way Calling: Terminal Side [Three Parties])



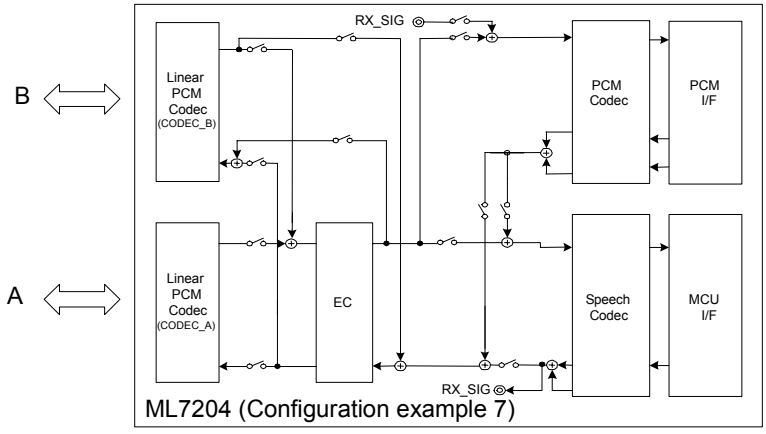
This example shows the configuration for making three-way calling between analog telephones (A-TEL1, A-TEL2, and A-TEL3) on the equipment with multiple analog telephone interface ports.



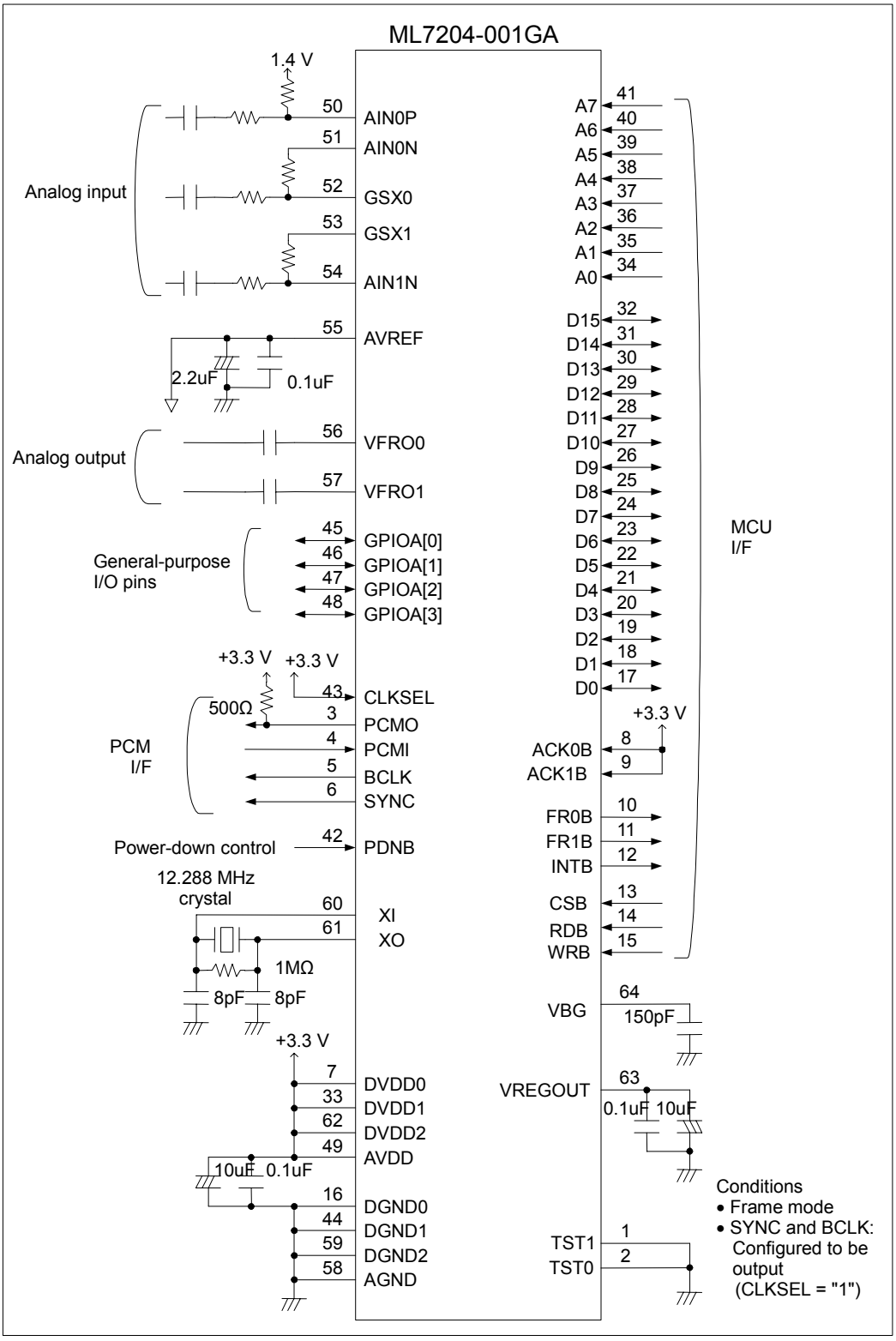
Configuration Example 7 (CODEC-A-CODEC-B Loop Back Mode)

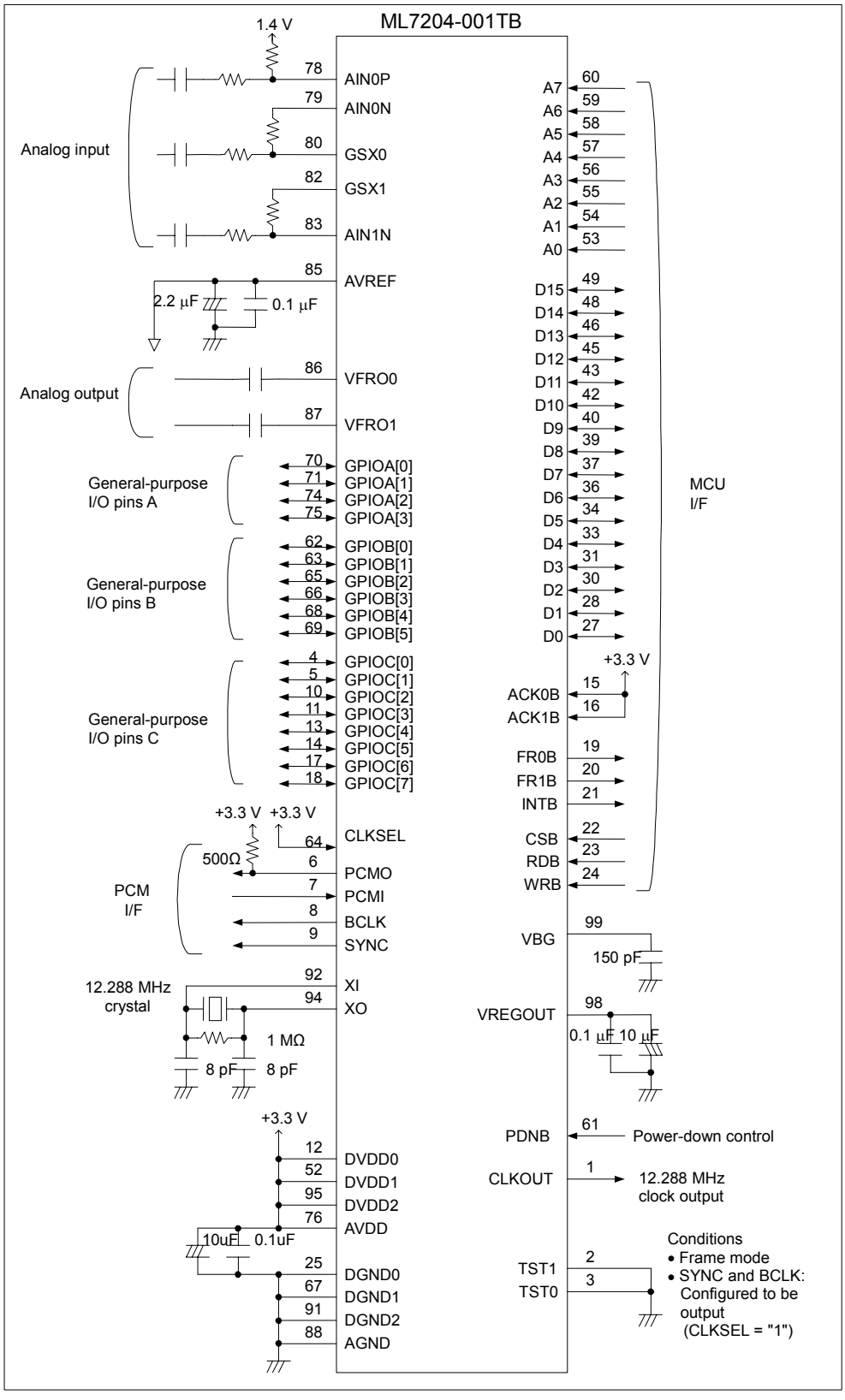


This example shows the configuration where CODEC_A and CODEC_B are connected in loopback mode according to the internal path settings.



APPLICATION CIRCUITS

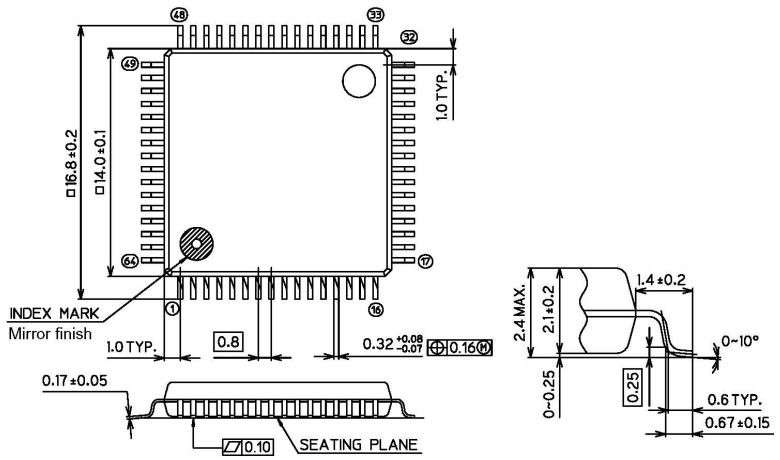



ML7204-001TB
1.4 V
78 AIN0P
79 AIN0N
80 GSX0
82 GSX1
83 AIN1N
Analog input
85 AVREF
2.2 µF
0.1 µF
86 VFRO0
87 VFRO1
Analog output
70 GPIOA[0]
71 GPIOA[1]
74 GPIOA[2]
75 GPIOA[3]
General-purpose I/O pins A
62 GPIOB[0]
63 GPIOB[1]
65 GPIOB[2]
66 GPIOB[3]
68 GPIOB[4]
69 GPIOB[5]
General-purpose I/O pins B
4 GPIOC[0]
5 GPIOC[1]
10 GPIOC[2]
11 GPIOC[3]
13 GPIOC[4]
14 GPIOC[5]
17 GPIOC[6]
18 GPIOC[7]
General-purpose I/O pins C
+3.3 V
+3.3 V
64 CLKSEL
500Ω
6 PCMO
7 PCMI
8 BCLK
9 SYNC
PCM I/F
92 XI
94 XO
12.288 MHz crystal
1 MΩ
8 pF
8 pF
+3.3 V
12 DVDD0
52 DVDD1
95 DVDD2
76 AVDD
10uF
0.1uF
25 DGND0
67 DGND1
91 DGND2
88 AGND
A7 60
A6 59
A5 58
A4 57
A3 56
A2 55
A1 54
A0 53
D15 49
D14 48
D13 46
D12 45
D11 43
D10 42
D9 40
D8 39
D7 37
D6 36
D5 34
D4 33
D3 31
D2 30
D1 28
D0 27
MCU I/F
+3.3 V
ACK0B 15
ACK1B 16
FR0B 19
FR1B 20
INTB 21
CSB 22
RDB 23
WRB 24
VBG 99
150 pF
VREGOUT 98
0.1 µF
10 µF
PDNB 61
Power-down control
CLKOUT 1
12.288 MHz clock output
TST1 2
TST0 3
Conditions
• Frame mode
• SYNC and BCLK: Configured to be output (CLKSEL = "1")

PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

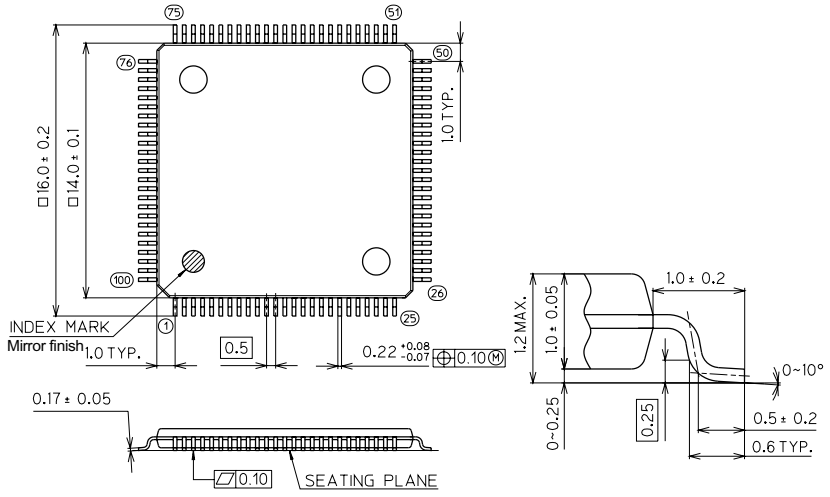
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7204-001DIGEST-01	Aug. 12, 2004	–	–	Final edition 1

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