

## N-Channel Enhancement Mode Power MOSFET

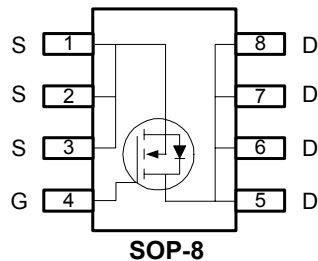
### ■ Features

- Simple Drive Requirement
- Low On-resistance
- Fast Switching Characteristic

### ■ Product Summary

$BV_{DSS}$ (V)	$R_{DS(ON)}$ (m $\Omega$ )	$I_D$ (A)
30	18	9.6

### ■ Pin Assignments



### ■ General Description

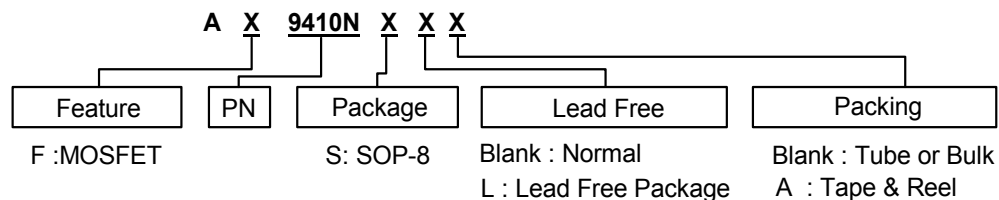
The advanced power MOSFET provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

### ■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

### ■ Ordering information





## N-Channel Enhancement Mode Power MOSFET

### ■ Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 25$	V
$I_D$	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	9.6
		$T_A=70^\circ\text{C}$	7.7
$I_{DM}$	Pulsed Drain Current (Note 2)	40	A
$P_D$	Total Power Dissipation	$T_A=25^\circ\text{C}$	2.5
	Linear Derating Factor		0.02
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### ■ Thermal Data

Symbol	Parameter	Maximum	Units
$R_{thj-amb}$	Thermal Resistance Junction-ambient (Note 1)	Max. 50	$^\circ\text{C}/\text{W}$

### ■ Electrical Characteristics at $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	30	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.04	-	$\text{V}/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance (Note 3)	$V_{GS}=10\text{V}, I_D=9\text{A}$	-	-	18	m $\Omega$
		$V_{GS}=4.5\text{V}, I_D=7\text{A}$	-	-	28	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10\text{V}, I_D=9\text{A}$	-	13	-	S
$I_{DSS}$	Drain-Source Leakage Current ( $T_J=25^\circ\text{C}$ )	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	-	-	1	uA
	Drain-Source Leakage Current ( $T_J=70^\circ\text{C}$ )	$V_{DS}=24\text{V}, V_{GS}=0\text{V}$	-	-	25	
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 25\text{V}$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge (Note 3)	$I_D=9\text{A}$	-	11	18	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=20\text{V}$	-	3	-	
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5\text{V}$	-	7	-	
$t_{d(on)}$	Turn-On Delay Time (Note 3)	$V_{DS}=15\text{V},$ $I_D=1\text{A},$ $R_G=3.3\Omega, V_{GS}=10\text{V}$ $R_D=15\Omega$	-	10	-	ns
$t_r$	Rise Time		-	6	-	
$t_{d(off)}$	Turn-Off Delay Time		-	23	-	
$t_f$	Fall-Time		-	7	-	
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$	-	840	1350	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25\text{V}$	-	190	-	
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	140	-	
$R_G$	Gate Resistance	$f=1.0\text{MHz}$	-	1.4	-	$\Omega$

### ■ Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward On Voltage (Note 3)	$I_S=2.1\text{A}, V_{GS}=0\text{V}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S=9\text{A}, V_{GS}=0\text{V}$	-	18	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100\text{A}/\mu\text{s}$	-	8	-	nC

**Note 1:** Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board,  $t \leq 10$  sec;  $125^\circ\text{C}/\text{W}$  when mounted on Min. copper pad.

**Note 2:** Pulse width limited by Max. junction temperature.

**Note 3:** Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

## N-Channel Enhancement Mode Power MOSFET

### ■ Typical Performance Characteristics

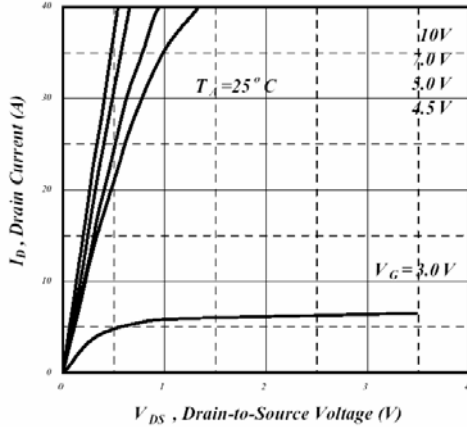


Fig 1. Typical Output Characteristics

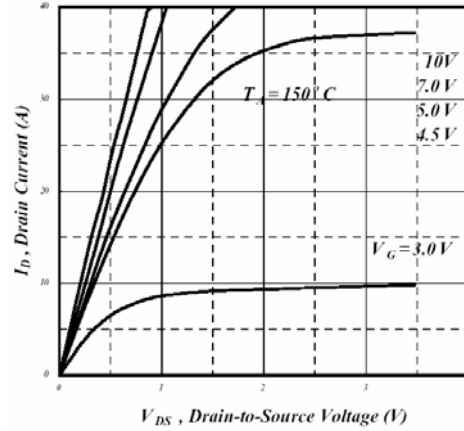


Fig 2. Typical Output Characteristics

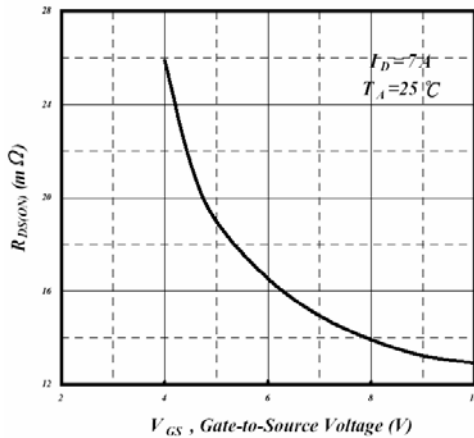


Fig 3. On-Resistance v.s. Gate Voltage

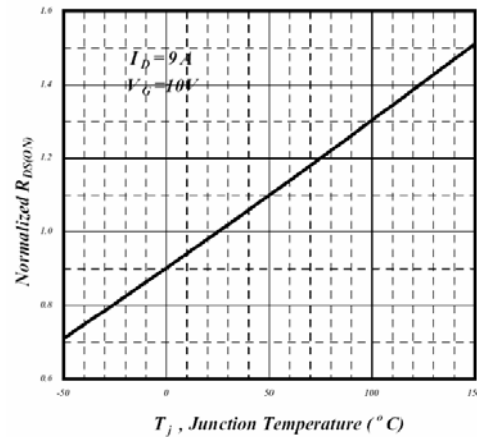


Fig 4. Normalized On-Resistance v.s. Junction Temperature

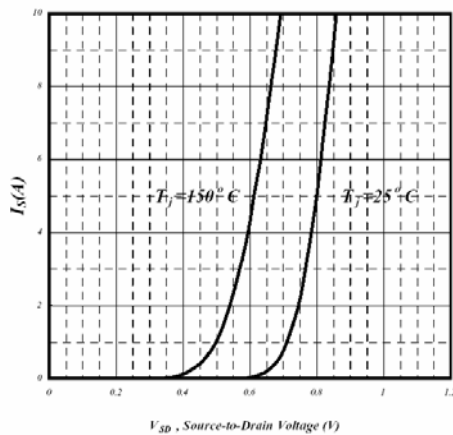


Fig 5. Forward Characteristic of Reverse Diode

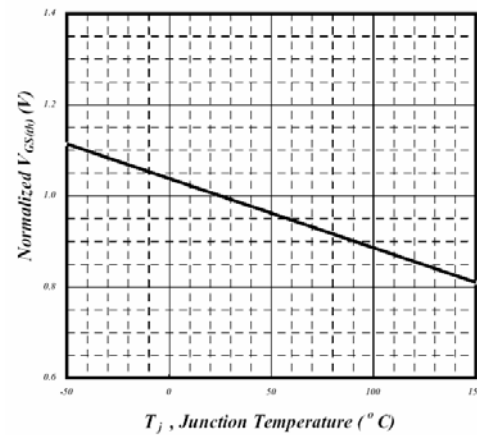


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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### ■ Typical Performance Characteristics

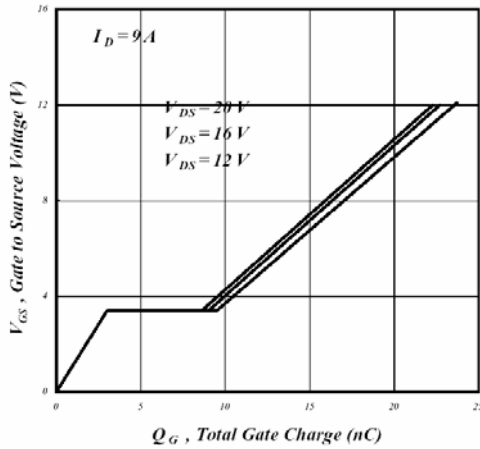


Fig 7. Gate Charge Characteristics

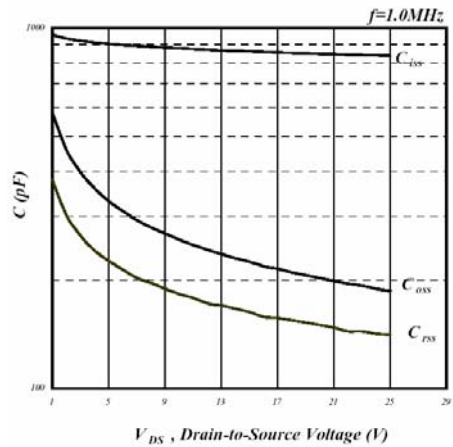


Fig 8. Typical Capacitance Characteristics

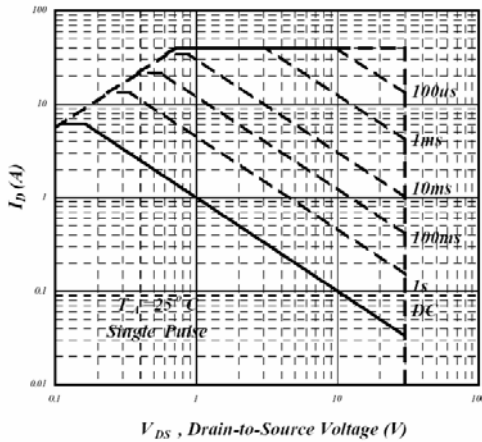


Fig 9. Maximum Safe Operating Area

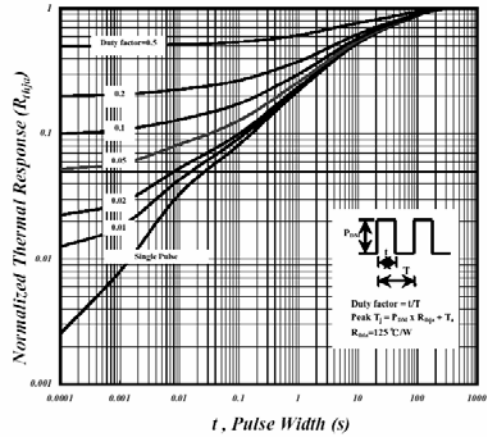


Fig 10. Effective Transient Thermal Impedance

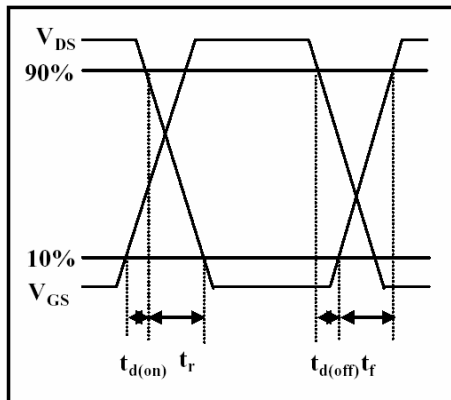


Fig 11. Switching Time Waveform

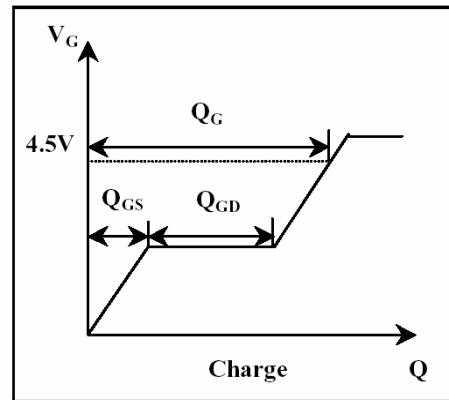
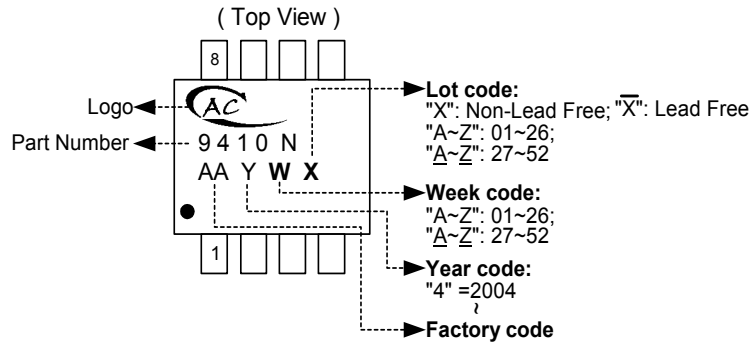


Fig 12. Gate Charge Waveform

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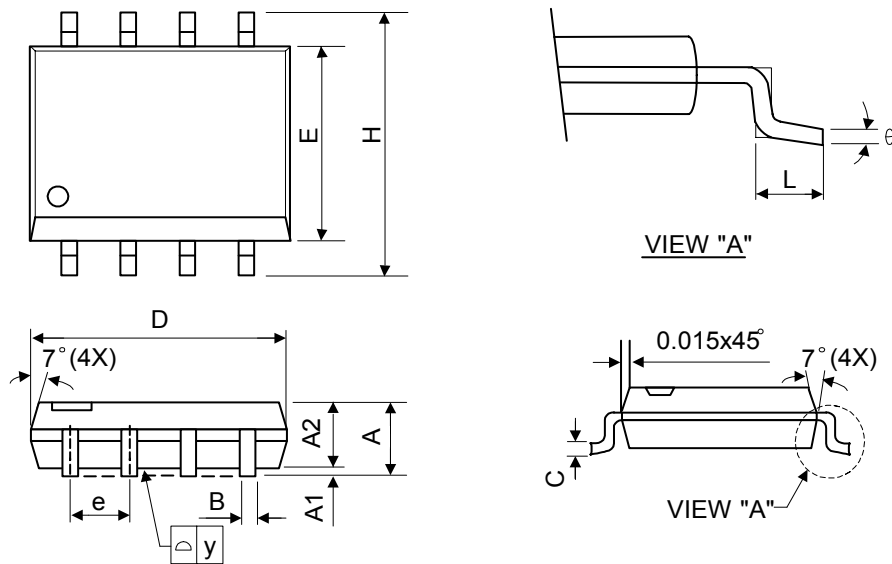
### ■ Marking Information

SOP-8L



### ■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°