Preliminary **16Mb Synchronous DRAM**

Features

- High Performance:

		-70 CL=3	-80 CL=3	-10 CL=3	Units
f_{CK}	Clock Frequency	143	125	100	MHz
t_{CK}	Clock Cycle	7	8	10	ns
t_{AC}	Clock Access Time	5	6	8	ns

- Single Pulsed $\overline{RAS}$ Interface
- Fully Synchronous to Positive Clock Edge
- Dual Banks controlled by A11 (Bank Select)
- Programmable CAS Latency: 1,2,3
- Programmable Burst Length: 1,2,4,8,full-page
- Programmable Wrap Sequence: Sequential or Interleave
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control (x4, x8)
- Dual Data Mask for byte control (x16)
- Auto Refresh (CBR)
- Standard or Low Power Self Refresh (SR)
- Suspend Mode and Power Down Mode
- 4096 refresh cycles/64ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3V ± 0.3V Power Supply
- Supports LVTTL and SSTL_3 I/O interfaces
- Package: 44 pin 400 mil TSOP-Type II (x4,x8)
  50 pin 400 mil TSOP-Type II (x16)
  2-High Stack TSOJ

Description

IBM's 0316409, 0316809, and 0316169 are dual bank Synchronous DRAMs organized as 2Mbit x 4 I/O x 2 Bank, 1Mbit x 8 I/O x 2 Bank, and 512Kbit x 16 I/O x 2 Bank, respectively. These devices support LVTTL or SSTL_3 I/O interface levels. Stacked versions of the x 4 and x 8 components are also offered. These synchronous devices achieve high speed data transfer rates of up to 143 MHz. The chip is fabricated with IBM's advanced 16Mbit CMOS DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address and data input/output circuits are synchronized with the positive edge of an externally supplied clock (CLK).

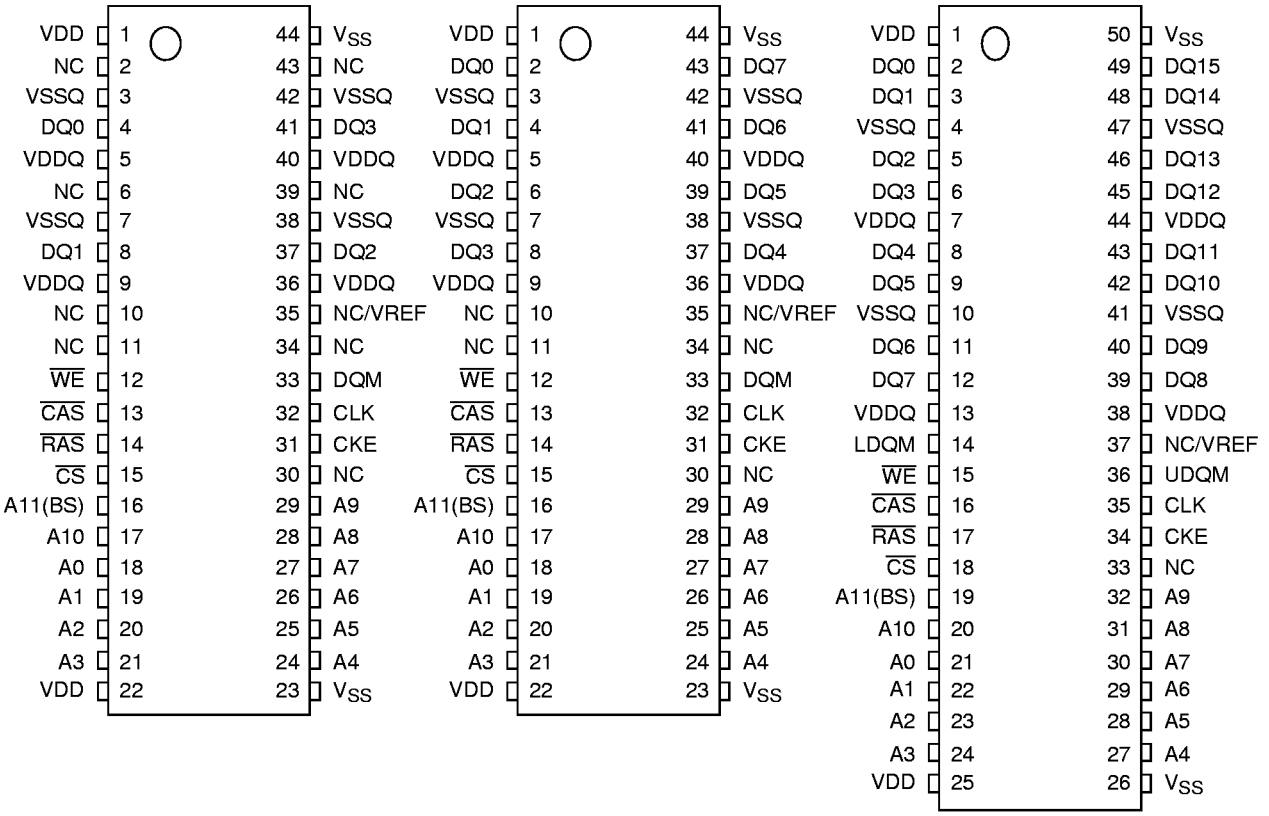
Internal chip operating modes are defined by combinations of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$ and a command decoder initiates the necessary timings for each operation. A twelve bit address bus accepts address data in the conventional $\overline{RAS}$/$\overline{CAS}$ multiplexing style. Eleven row addresses (A0-A10) and a bank select address (A11) are strobed with $\overline{RAS}$. Ten column addresses (A0-A9) plus a bank select address (A11) are strobed with $\overline{CAS}$. Column address A9 is dropped on the x8 device and column addresses A8 and A9 are dropped on the x16 device. Access to the lower or upper DRAM in a stacked device is controlled by $\overline{CS0}$ and $\overline{CS1}$.

Prior to any access operation, the $\overline{CAS}$ latency, burst length, and burst sequence must be programmed into the device by address inputs A0-A9 during a mode register set cycle. In addition, it is possible to program a multiple burst sequence with single write cycle for write through cache operation.

Operating the two memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 143 MHz is possible depending on burst length, $\overline{CAS}$ latency, and speed grade of the device.

Auto Refresh (CBR) and Self Refresh (SR) operation are supported. Refreshing both decks of a stacked device simultaneously is allowed during Self Refresh but all other stacked device operations must be performed on a single deck at a time. Standard Power and Low Power SR are offered.

Pin Assignments for Planar Components (Top View)



44-pin Plastic TSOP(II) 400 mil

2Mbit x 4 I/O x 2 Bank

IBM0316409CT3
IBM0316409PT3
IBM0316409DT3
IBM0316409QT3

44-pin Plastic TSOP(II) 400 mil

1Mbit x 8 I/O x 2 Bank

IBM0316809CT3
IBM0316809PT3
IBM0316809DT3
IBM0316809QT3

50-pin Plastic TSOP(II) 400 mil

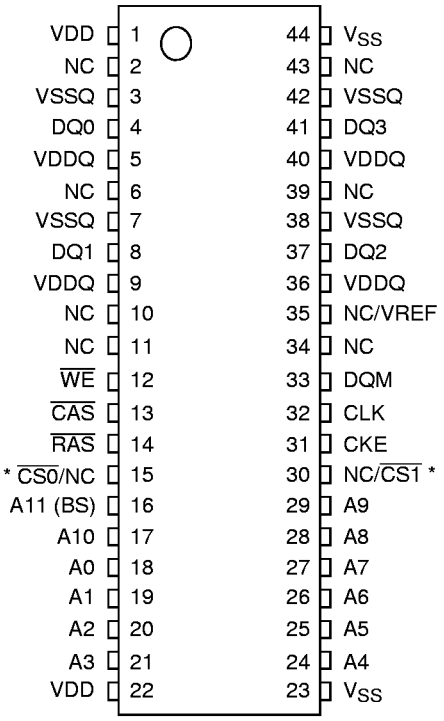
512Kbit x 16 I/O x 2 Bank

IBM0316169CT3
IBM0316169PT3
IBM0316169DT3
IBM0316169QT3

Pin Description

CLK	Clock Input	**DQ0-DQ15**	Data Input/Output
CKE	Clock Enable	**DQM, LDQM, UDQM**	Data Mask
$\overline{CS}$	Chip Select	**VDD**	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	**VSS**	Ground
$\overline{CAS}$	Column Address Strobe	**VDDQ**	Power for DQs (+3.3V)
$\overline{WE}$	Write Enable	**VSSQ**	Ground for DQs
A11 (BS)	Bank Select	**NC**	No Connection
A0 - A10	Address Inputs	**NC / VREF**	No Connection (LVTTL) Reference supply (SSTL_3)

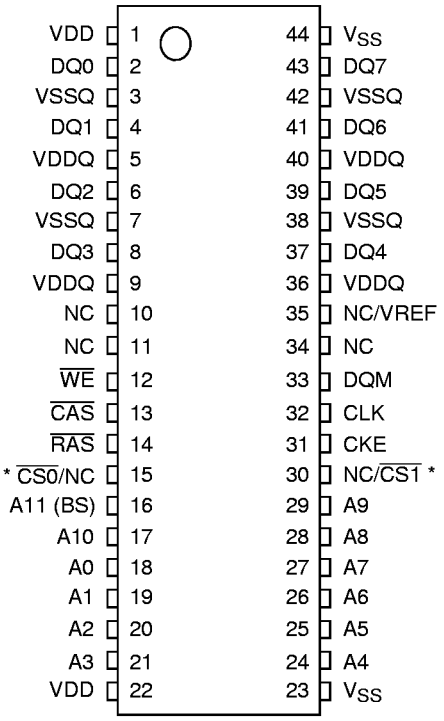
Pin Assignments for 2-High Stack Package (Dual $\overline{CS}$ Pins) (Top View)



44-pin Plastic TSOJ(II) 400 mil

(2Mbit x 4 I/O x 2 Bank) x 2 High

IBM03164B9CT3
IBM03164B9PT3
IBM03164B9DT3
IBM03164B9QT3



44-pin Plastic TSOJ(II) 400 mil

(1Mbit x 8 I/O x 2 Bank) x 2 High

IBM03168B9CT3
IBM03168B9PT3
IBM03168B9DT3
IBM03168B9QT3

* $\overline{CS0}$ selects the lower DRAM in the stack.
* $\overline{CS1}$ selects the upper DRAM in the stack.

Pin Description

CLK	Clock Input	**DQ0-DQ7**	Data Input/Output
CKE	Clock Enable	**DQM**	Data Mask
$\overline{CS0}$, $\overline{CS1}$	Chip Select	**VDD**	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	**VSS**	Ground
$\overline{CAS}$	Column Address Strobe	**VDDQ**	Power for DQs (+3.3V)
$\overline{WE}$	Write Enable	**VSSQ**	Ground for DQs
A11 (BS)	Bank Select	**NC**	No Connection
A0 - A10	Address Inputs	**NC / VREF**	No Connection (LVTTL) Reference supply (SSTL_3)

Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	Pulse	Active Low	$\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$ for stacked devices) enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
A11 (BS)	Input	Level	—	Selects which bank is to be active. A11 low selects bank A and A11 high selects bank B.
A0 - A10	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. A10 is used to invoke Auto-Precharge operation. If A10 is high, Auto-Precharge is selected and A11 defines the bank to be precharged (low=bank A, high=bank B). If A10 is low, Auto-Precharge is disabled. During a Precharge command cycle, A10 is used in conjunction with A11 to control which bank(s) to precharge. If A10 is high, both bank A and bank B will be precharged regardless of the state of A11. If A10 is low, then A11 is used to define which bank to precharge.
DQ0 - DQ15	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Pulse	Active Low	The DQ mask (DQM) places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers consistent with an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VDD, V_{SS}	Supply	—	—	Power and ground for the input buffers and the core logic.
VREF	Supply	—	—	Reference supply for SSTL_3 interface.
VDDQ, VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

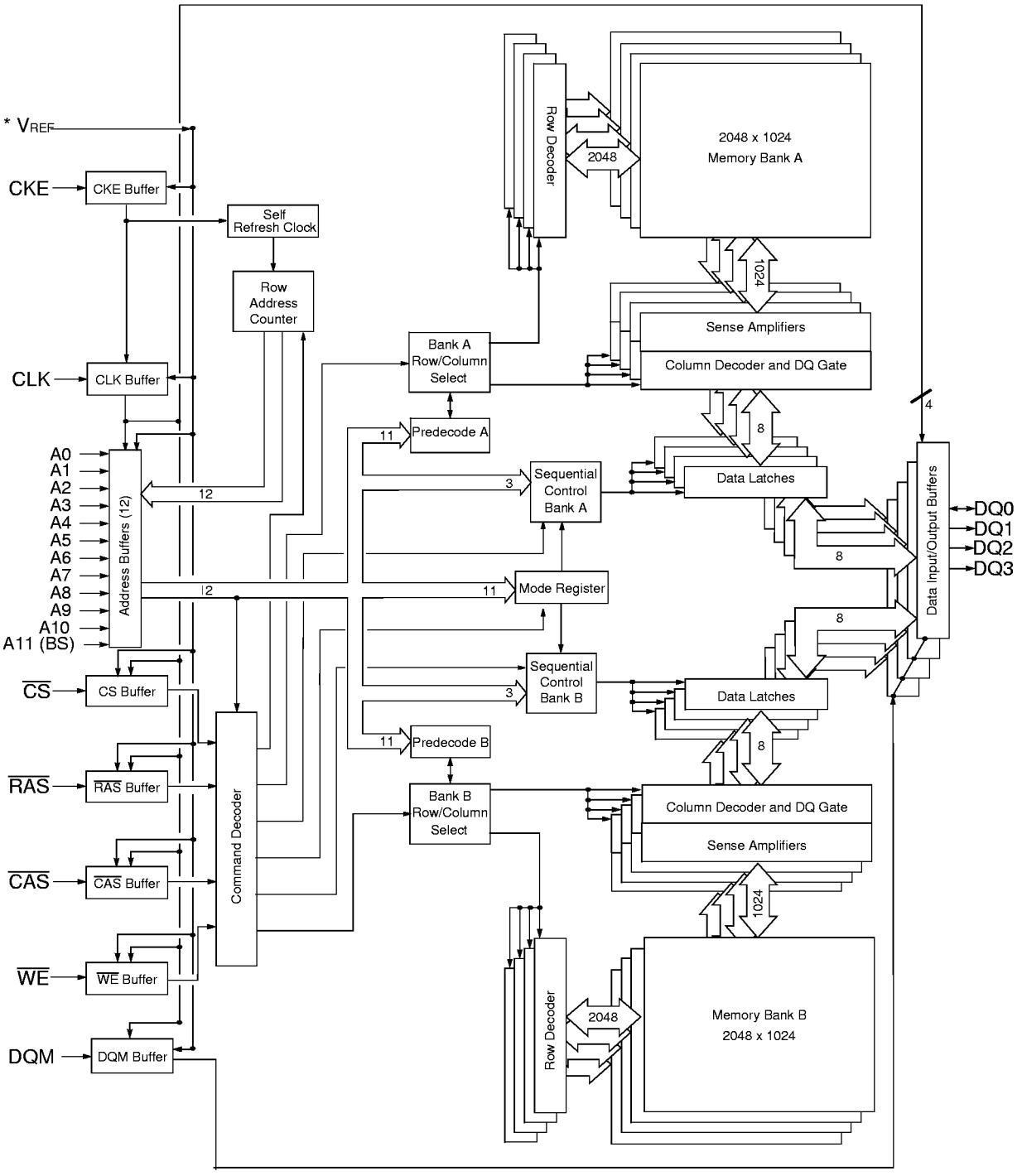
Ordering Information - Planar Devices (Single $\overline{CS}$ Pin)

Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	SP/LP Self Refresh	Clock Cycle
IBM0316409CT3-80	2,3	x4	LVTTL	400mil Type II TSOP-44	3.3V	SP	8ns
IBM0316409PT3-80	2,3	x4	LVTTL	400mil Type II TSOP-44	3.3V	LP	8ns
IBM0316409CT3-10	1,2,3	x4	LVTTL	400mil Type II TSOP-44	3.3V	SP	10ns
IBM0316409PT3-10	1,2,3	x4	LVTTL	400mil Type II TSOP-44	3.3V	LP	10ns
IBM0316809CT3-80	2,3	x8	LVTTL	400mil Type II TSOP-44	3.3V	SP	8ns
IBM0316809PT3-80	2,3	x8	LVTTL	400mil Type II TSOP-44	3.3V	LP	8ns
IBM0316809CT3-10	1,2,3	x8	LVTTL	400mil Type II TSOP-44	3.3V	SP	10ns
IBM0316809PT3-10	1,2,3	x8	LVTTL	400mil Type II TSOP-44	3.3V	LP	10ns
IBM0316169CT3-80	2,3	x16	LVTTL	400mil Type II TSOP-50	3.3V	SP	8ns
IBM0316169PT3-80	2,3	x16	LVTTL	400mil Type II TSOP-50	3.3V	LP	8ns
IBM0316169CT3-10	1,2,3	x16	LVTTL	400mil Type II TSOP-50	3.3V	SP	10ns
IBM0316169PT3-10	1,2,3	x16	LVTTL	400mil Type II TSOP-50	3.3V	LP	10ns
IBM0316409DT3-70	2,3	x4	SSTL_3	400mil Type II TSOP-44	3.3V	SP	7ns
IBM0316409QT3-70	2,3	x4	SSTL_3	400mil Type II TSOP-44	3.3V	LP	7ns
IBM0316409DT3-80	2,3	x4	SSTL_3	400mil Type II TSOP-44	3.3V	SP	8ns
IBM0316409QT3-80	2,3	x4	SSTL_3	400mil Type II TSOP-44	3.3V	LP	8ns
IBM0316809DT3-70	2,3	x8	SSTL_3	400mil Type II TSOP-44	3.3V	SP	7ns
IBM0316809QT3-70	2,3	x8	SSTL_3	400mil Type II TSOP-44	3.3V	LP	7ns
IBM0316809DT3-80	2,3	x8	SSTL_3	400mil Type II TSOP-44	3.3V	SP	8ns
IBM0316809QT3-80	2,3	x8	SSTL_3	400mil Type II TSOP-44	3.3V	LP	8ns
IBM0316169DT3-70	2,3	x16	SSTL_3	400mil Type II TSOP-50	3.3V	SP	7ns
IBM0316169QT3-70	2,3	x16	SSTL_3	400mil Type II TSOP-50	3.3V	LP	7ns
IBM0316169DT3-80	2,3	x16	SSTL_3	400mil Type II TSOP-50	3.3V	SP	8ns
IBM0316169QT3-80	2,3	x16	SSTL_3	400mil Type II TSOP-50	3.3V	LP	8ns

Ordering Information - 2 High Stacked Devices (Dual $\overline{CS}$ Pins)

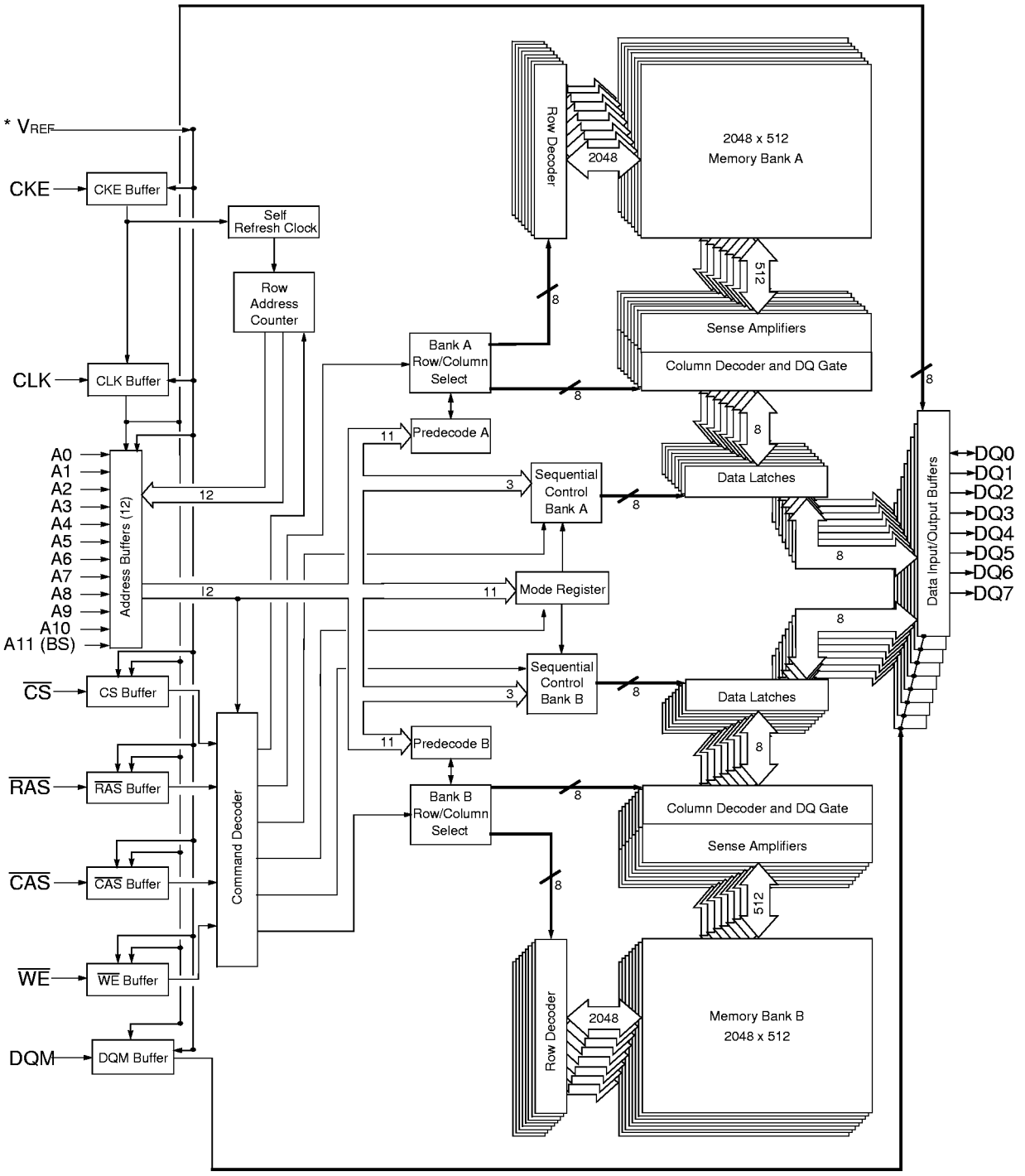
Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	SP/LP Self Refresh	Clock Cycle
IBM03164B9CT3-80	2,3	x4	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	SP	8ns
IBM03164B9PT3-80	2,3	x4	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	LP	8ns
IBM03164B9CT3-10	1,2,3	x4	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	SP	10ns
IBM03164B9PT3-10	1,2,3	x4	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	LP	10ns
IBM03168B9CT3-80	2,3	x8	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	SP	8ns
IBM03168B9PT3-80	2,3	x8	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	LP	8ns
IBM03168B9CT3-10	1,2,3	x8	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	SP	10ns
IBM03168B9PT3-10	1,2,3	x8	LVTTL	400mil Type II TSOJ-44 2-High	3.3V	LP	10ns
IBM03164B9DT3-70	2,3	x4	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	SP	7ns
IBM03164B9QT3-70	2,3	x4	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	LP	7ns
IBM03164B9DT3-80	2,3	x4	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	SP	8ns
IBM03164B9QT3-80	2,3	x4	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	LP	8ns
IBM03168B9DT3-70	2,3	x8	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	SP	7ns
IBM03168B9QT3-70	2,3	x8	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	LP	7ns
IBM03168B9DT3-80	2,3	x8	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	SP	8ns
IBM03168B9QT3-80	2,3	x8	SSTL_3	400mil Type II TSOJ-44 2-High	3.3V	LP	8ns

Block Diagram (2Mbit x 4 I/O x 2 Bank)



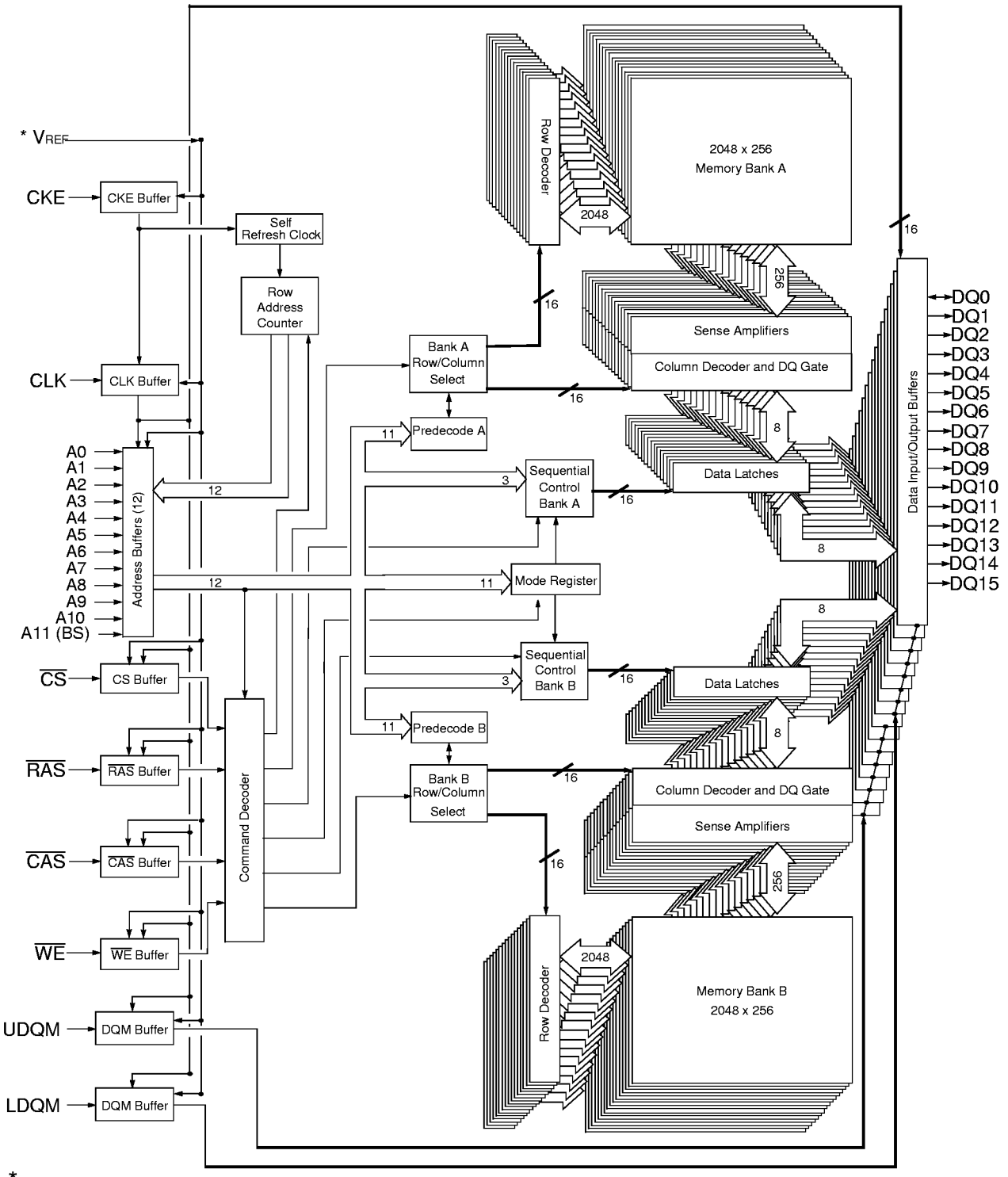
*V_{REF} not applicable for LVTTL devices.

Block Diagram (1Mbit x 8 I/O x 2 Bank)



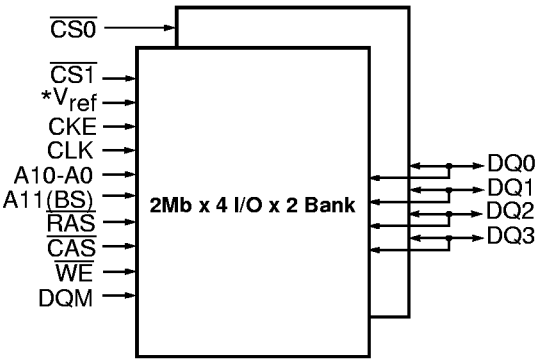
*V_{REF} not applicable for LVTTL devices.

Block Diagram (512Kbit x 16 I/O x 2 Bank)



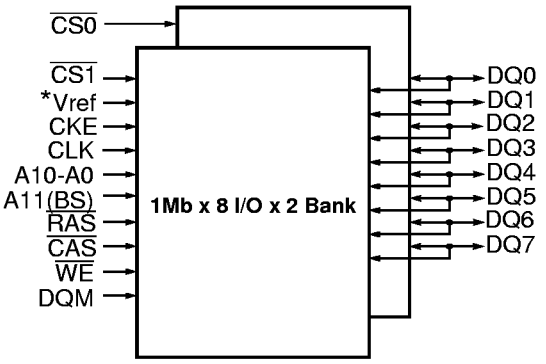
*V_{REF} not applicable for LVTTL devices.

Block Diagram (2Mbit x 4 I/O x 2 Bank) x 2-High



*V_{REF} not applicable for LVTTL devices.

Block Diagram (1Mbit x 8 I/O x 2 Bank) x 2-High



*V_{REF} not applicable for LVTTL devices.

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs.

Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD, VDDQ, and VREF pins must be built up simultaneously to the specified voltage no later than any of the input signal voltages. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. After power on, an initial pause of 100µs is required followed by a precharge of both banks using the precharge command. To reduce the possibility of data contention on the DQ bus during power on, it is recommended that the DQM pin(s) be held high during the initial pause period. Once both banks have been precharged, a minimum of two Auto Refresh cycles (CBR) must occur before the Mode Register can be programmed. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

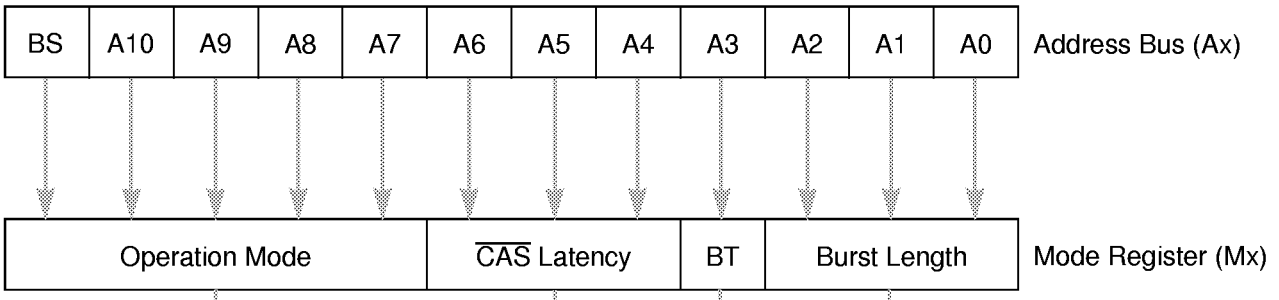
For application flexibility, $\overline{\text{CAS}}$ latency, burst length, burst sequence, and operation type are user defined variables and must be programmed into the SDRAM Mode Register with a single Mode Register Set Command. Contents of the Mode Register can be altered by re-executing the Mode Register Set Command. If the user chooses to modify only a subset of the Mode Register variables, all variables must be redefined when the Mode Register Set Command is issued.

After initial power up, the Mode Register Set Command must be issued before read or write cycles may begin. Both banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued on the second clock following the mode register set command.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is a parameter that is used to define the delay from when a Read Command is registered on a rising clock edge to when the data from that Read Command becomes available at the outputs. $\overline{\text{CAS}}$ latency is expressed in terms of clock cycles and can be programmed to a value of 1, 2, or 3 cycles. The value of $\overline{\text{CAS}}$ latency is determined by the speed grade of the device and the clock frequency that is used in the application. A table showing the relationship between the $\overline{\text{CAS}}$ latency, speed grade, and clock frequency appears in the Electrical Characteristics section of this document. Once the appropriate $\overline{\text{CAS}}$ latency has been selected it must be programmed into the mode register after power up. For an explanation of this procedure, see Programming the Mode Register in the previous section.

Mode Register Operation (Address Input For Mode Set)



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Normal
X	X	1	0	0	Multiple Burst with Single Write

Burst Type

M3	Type
0	Sequential
1	Interleave

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). There are three parameters that define how the burst mode will operate. These parameters include burst sequence, burst length, and operation mode. The burst sequence and burst length are programmable, and are determined by address bits A0 - A3 during the Mode Register Set command. Operation mode is also programmable and is set by address bits A7 - A10 and BS.

The burst type is used to define the order in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequences are supported, sequential and interleaved. See Table.

The burst length controls the number of bits that will be output after a Read Command, or the number of bits to be input after a Write Command. The burst length can be programmed to have values of 1, 2, 4, 8 or full page (actual page length is dependent on organization: x4, x8, or x16). Full page burst operation is only possible using the sequential burst type.

Burst operation mode can be normal operation or multiple burst with single write operation. Normal operation implies that the device will perform burst operations on both read and write cycles until the desired burst length is satisfied. Multiple burst with single write operation was added to support Write Through Cache operation. Here, the programmed burst length only applies to read cycles. All write cycles are single write operations when this mode is selected.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
2	x x 0	0, 1	0, 1
	x x 1	1, 0	1, 0
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
Full Page (Note)	n n n	Cn, Cn+1, Cn+2, ...	Not Supported

Note: Page length is a function of I/O organization and column addressing.

x4 organization (CA0-CA9); Page Length = 1024 bits

x8 organization (CA0-CA8); Page Length = 512 bits

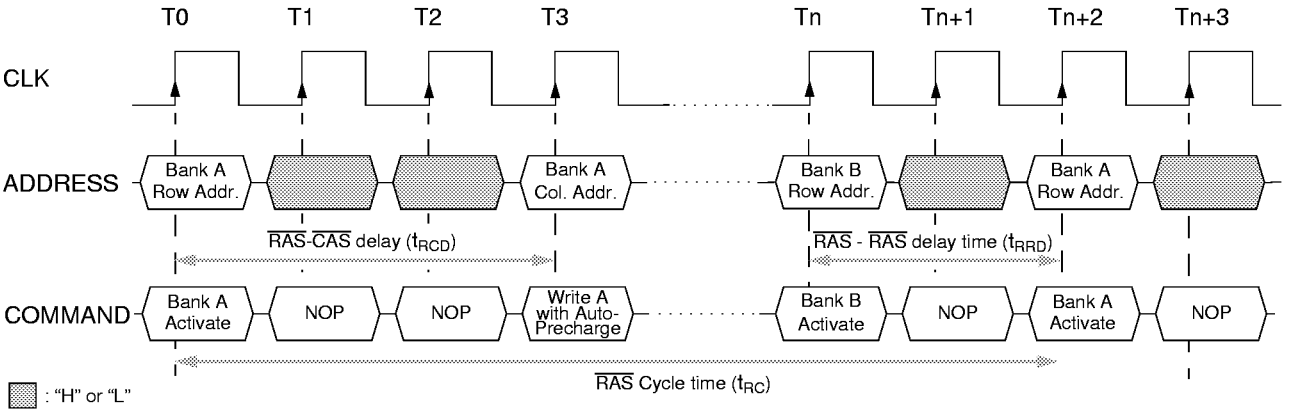
x16 organization (CA0-CA7); Page Length = 256 bits

Bank Activate Command

In relation to the operation of a fast page mode DRAM, the Bank Activate command corresponds to a falling $\overline{RAS}$ signal. The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank select address, A11 (sometimes referred to as BS), is used to select the desired bank. If BS is low then bank A is activated, if BS is high then bank B is activated. The row address A0 - A10 is used to determine which row to activate in the selected bank. Only banks A and B within a single deck of a 2-High stacked device can be accessed. Simultaneous operation of both decks in a stacked device is not allowed, except during Self Refresh.

The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must meet or exceed the $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}). Once a bank has been activated it must be pre-charged before another Bank Activate command can be applied to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}).

Bank Activate Command Cycle ($\overline{CAS}$ Latency = 3)



Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high and $\overline{CAS}$ low at the clock's rising edge after the necessary $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}). $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high), or a write operation ($\overline{WE}$ low).

The SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 143MHz. The number of serial data bits for each access is equal to the burst length, which is programmed into the Mode Register. Although the burst length is user programmable, the boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 2Mbit x 4 I/O x 2 Bank device has a page length of 1024 bits (defined by CA0-CA9). If a burst length of 4 is programmed into the Mode Register, then the page length is divided into 256 uniquely addressable boundary segments (4-bits each). A 4-bit burst operation will occur entirely from one of the 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9). The second, third, and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, the burst sequence, and burst boundary.

The above discussion does not apply when full page burst is programmed into the Mode Register. Full page burst operation is only allowed for the sequential burst sequence and has no address boundaries. The SDRAM device will continue bursting data even after all locations of the page have been accessed. The burst sequence will start at the column address defined during the read or write cycle and will increment sequentially until the highest order column address has been reached. At this point, the burst counter will reset to address 0 and continue to perform burst read or burst write operations sequentially until either a Burst Stop Command is issued, a Precharge Command is issued to the bursting bank, or until a new Read or Write Command is issued.

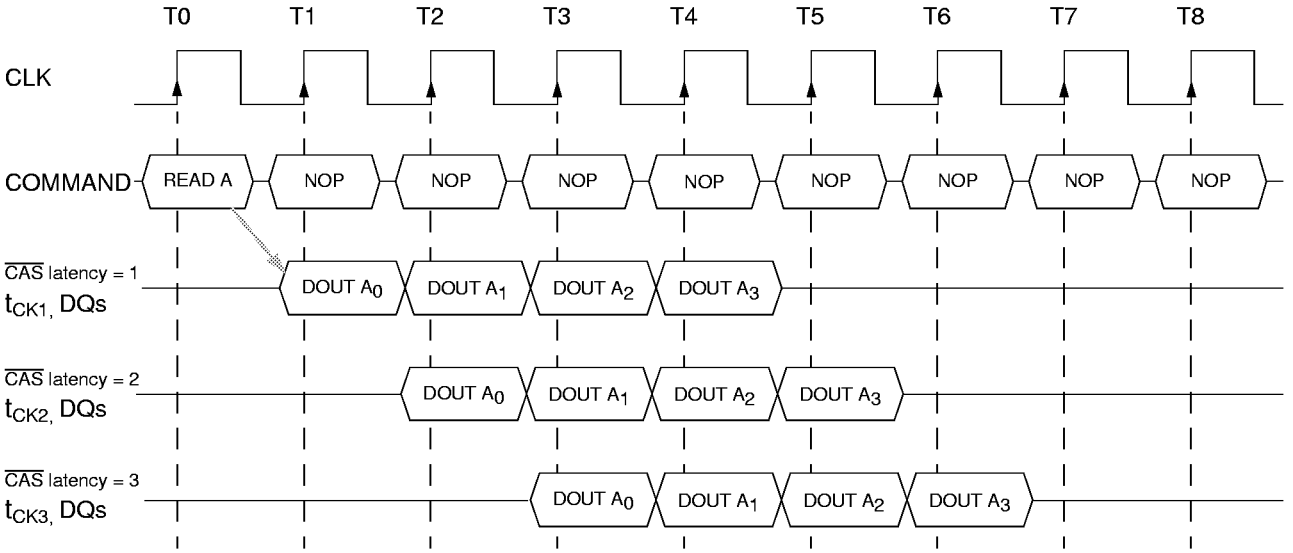
Similar to Page Mode of conventional DRAMs, a read or write cycle can not begin until the sense amplifiers latch the selected row address information. The refresh period (t_{REF}) is what limits the number of random column accesses to an activated bank. A new burst access can be done even before the previous burst ends. The ability to interrupt a burst operation at every clock cycle is supported, this is referred to as the 1-N rule. When the previous burst is interrupted by another Read or Write Command, the remaining addresses are overridden by the new address once the $\overline{CAS}$ Latency has been satisfied.

Precharging an active bank after each read or write operation is not necessary providing the same row is to be accessed again. To perform a read or write cycle to a different row within an activated bank, the bank must be precharged and a new Bank Activate command must be issued. When both Bank A and Bank B are activated, interleaved (ping pong) bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between the two banks, fast and seamless data access operation among many different pages can be realized. When the two banks are activated, column to column interleave operation can be done between two different pages. Finally, Read or Write Commands can be issued to the same bank or between active banks on every clock cycle.

Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst, the Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page). The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the $\overline{CAS}$ latency that is set in the Mode Register.

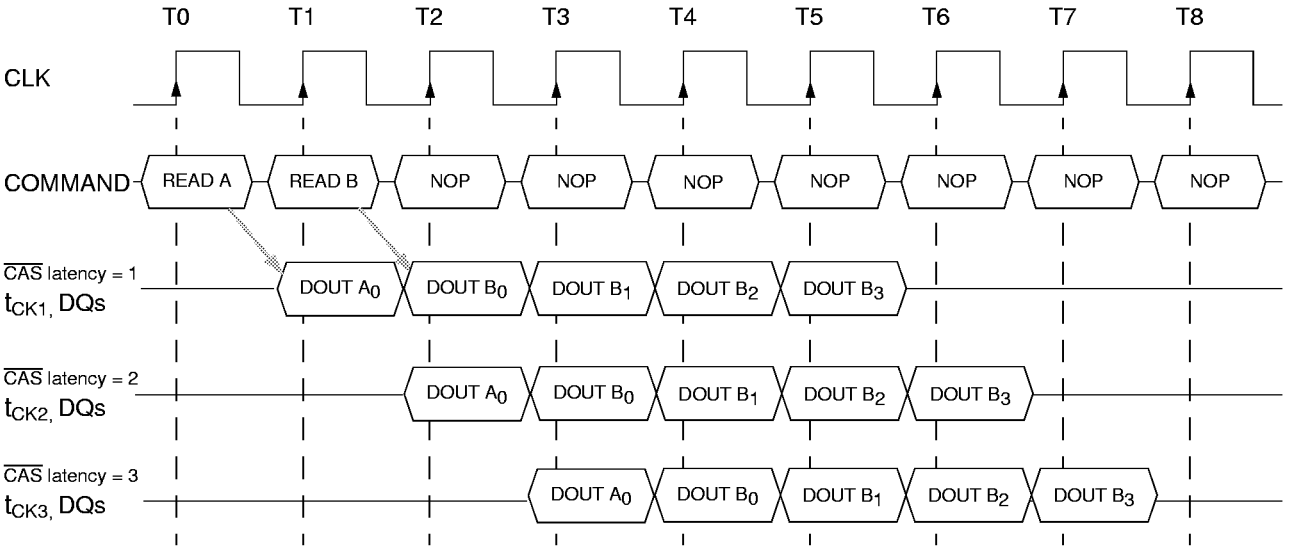
Burst Read Operation (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)



Read Interrupted by a Read

A Burst Read may be interrupted before completion of the burst by another Read Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When a burst read operation is interrupted, the remaining addresses of the current burst cycle are overridden starting with the new column address applied with the interrupting Read Command. The data from the first Read Command continues to appear on the DQs until the $\overline{CAS}$ latency of the interrupting Read Command is satisfied. At this point, the data from the interrupting Read Command will appear on the DQs and continue for the full burst length.

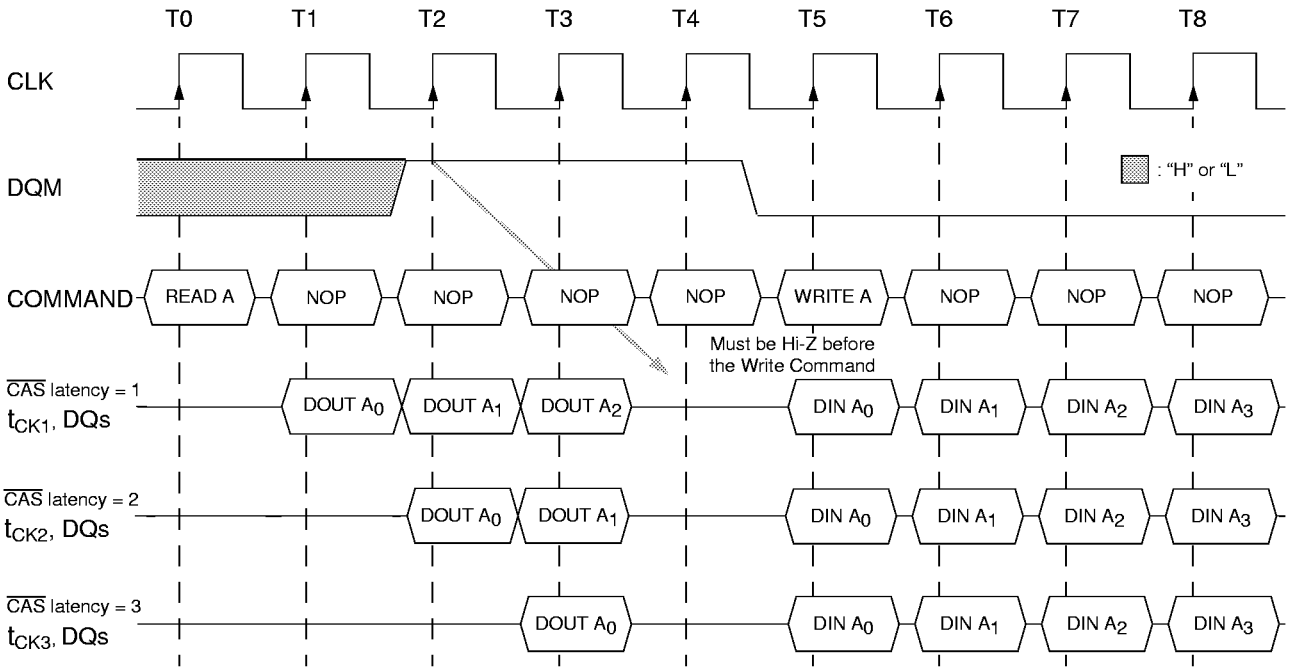
Read Interrupted by a Read (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)



Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM must be used to avoid data contention on the data bus by placing the chip output drivers in a high impedance state at least one clock cycle before the Write Command is initiated. To insure the chip output drivers are tri-stated one cycle before the write operation begins, DQM must be activated at least 3 clock cycles before the Write Command and be deactivated in the same clock cycle as the Write Command.

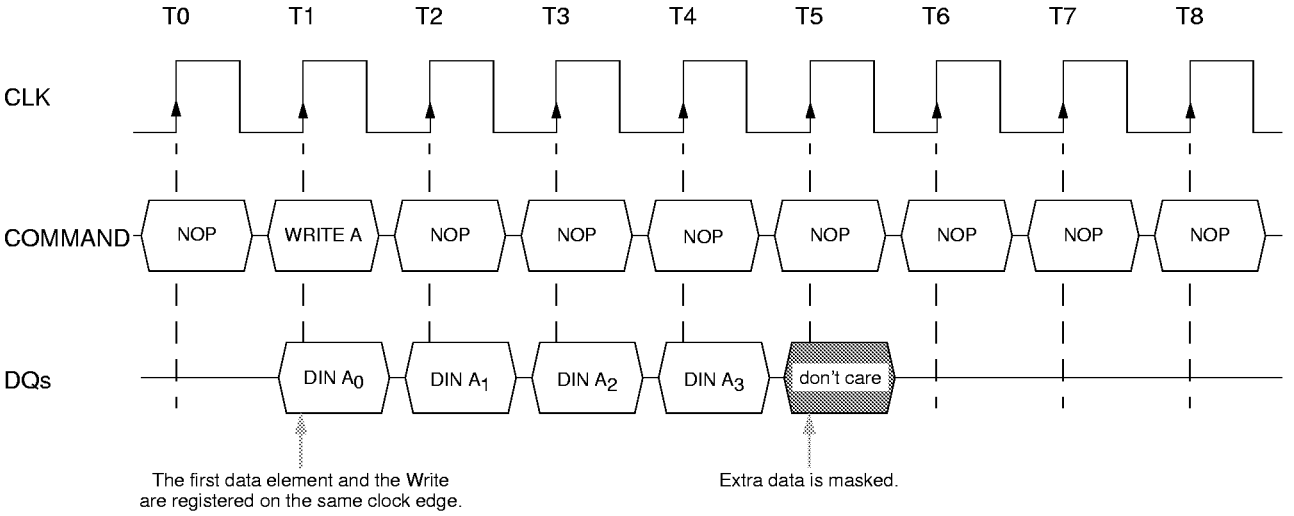
Read Interrupted by a Write (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)



Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. There is no $\overline{CAS}$ latency required for burst write cycles. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

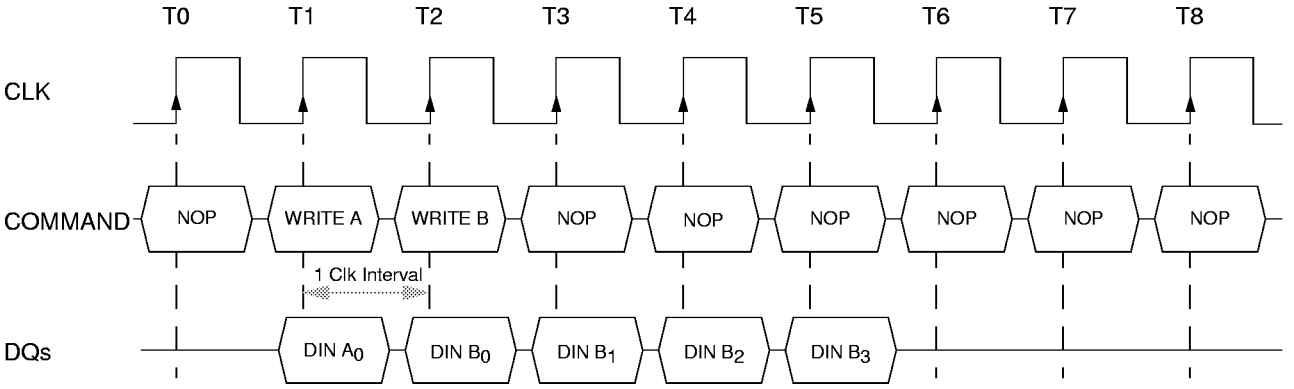
Burst Write Operation(Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)



Write Interrupted by a Write

A burst write operation may be interrupted before completion of the burst. When a burst write cycle is interrupted by a new Write Command, the remaining addresses of the initial write cycle are overridden starting with the new column address applied with the interrupting Write Command. Data will be written into the device until the programmed burst length of the last write command is satisfied.

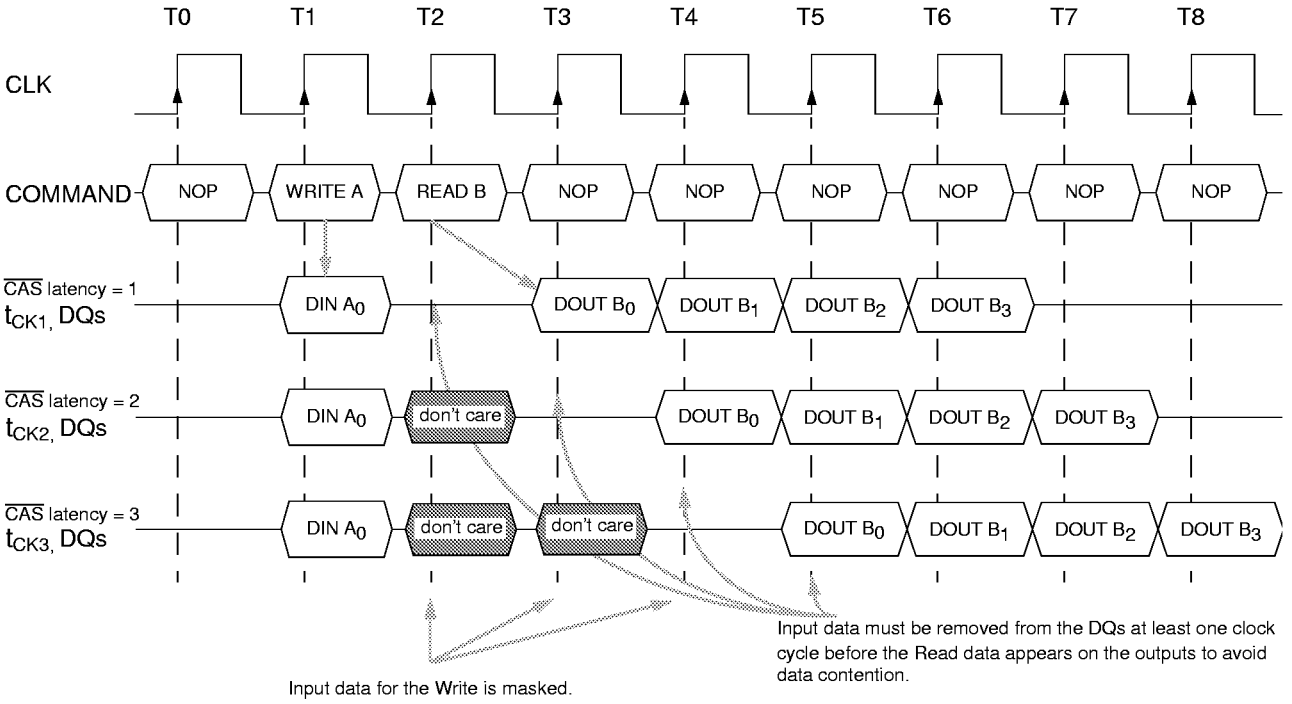
Write Interrupted by a Write (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3



Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is registered. The DQs must be in the high impedance state at least one cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read Command is registered, any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Read Command is initiated will actually be written to the memory.

Write Interrupted by a Read (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)

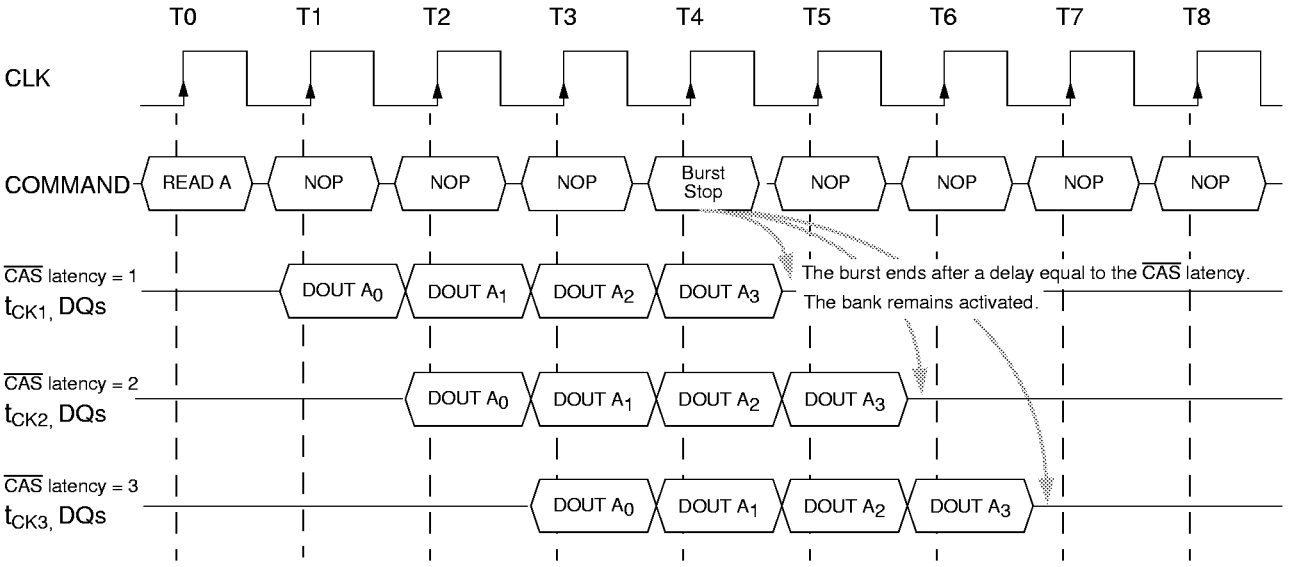


Burst Stop Command

Once a burst read or write operation has been initiated, there exist several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed.

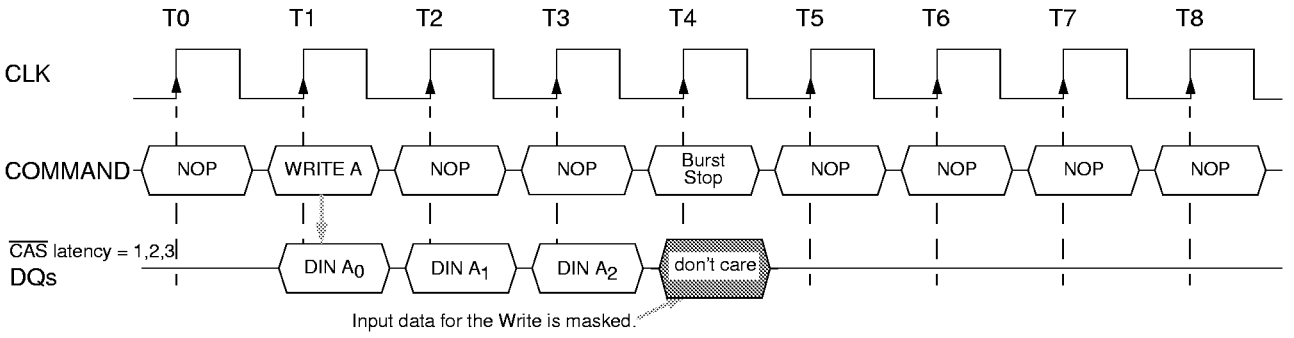
The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. When using the Burst Stop Command during a burst read cycle, the data DQs go to a high impedance state after a delay which is equal to the $\overline{CAS}$ Latency set in the Mode Register.

Termination of a Burst Read Operation (Burst Length > 4, $\overline{CAS}$ Latency = 1, 2, 3)



When a Burst Stop Command is issued during a burst write operation, only data presented prior to the Burst Stop command will be written into the device. Any data presented to the device coincident with the Burst Stop command or later will be ignored.

Termination of a Burst Write Operation (Burst Length =X, $\overline{CAS}$ Latency = 1, 2, 3)



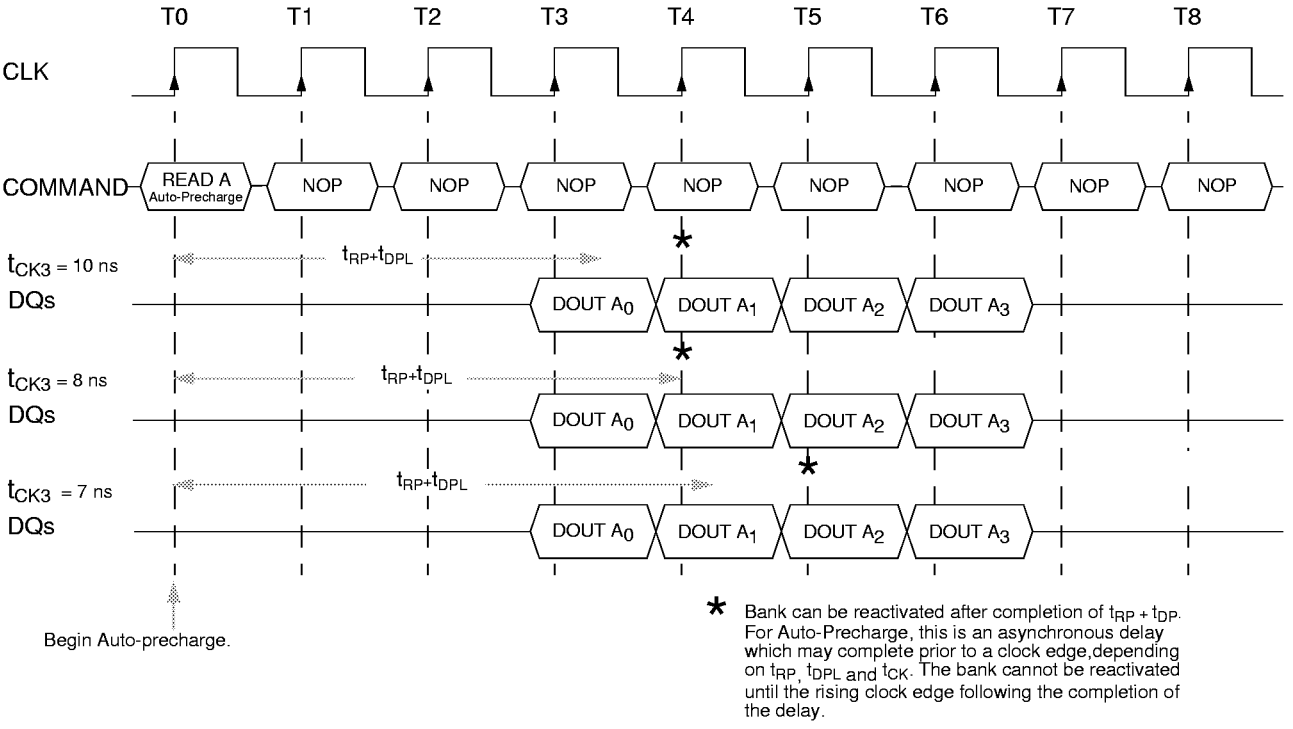
Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the SDRAM, the CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge immediately and may finish before all burst read cycles have been completed. This feature allows the precharge operation to be partially or completely hidden during the burst read cycles (dependent upon burst length) thus improving system performance for random data access. Auto-precharge can also be implemented during Write commands.

A Read or Write Command without auto-precharge can be terminated in the midst of a burst operation. However, a Read or Write Command with auto-precharge can not be interrupted before the entire burst operation is completed. Therefore use of a Read, Write, Precharge, or Burst Stop Command is prohibited during a read or write cycle with auto-precharge.

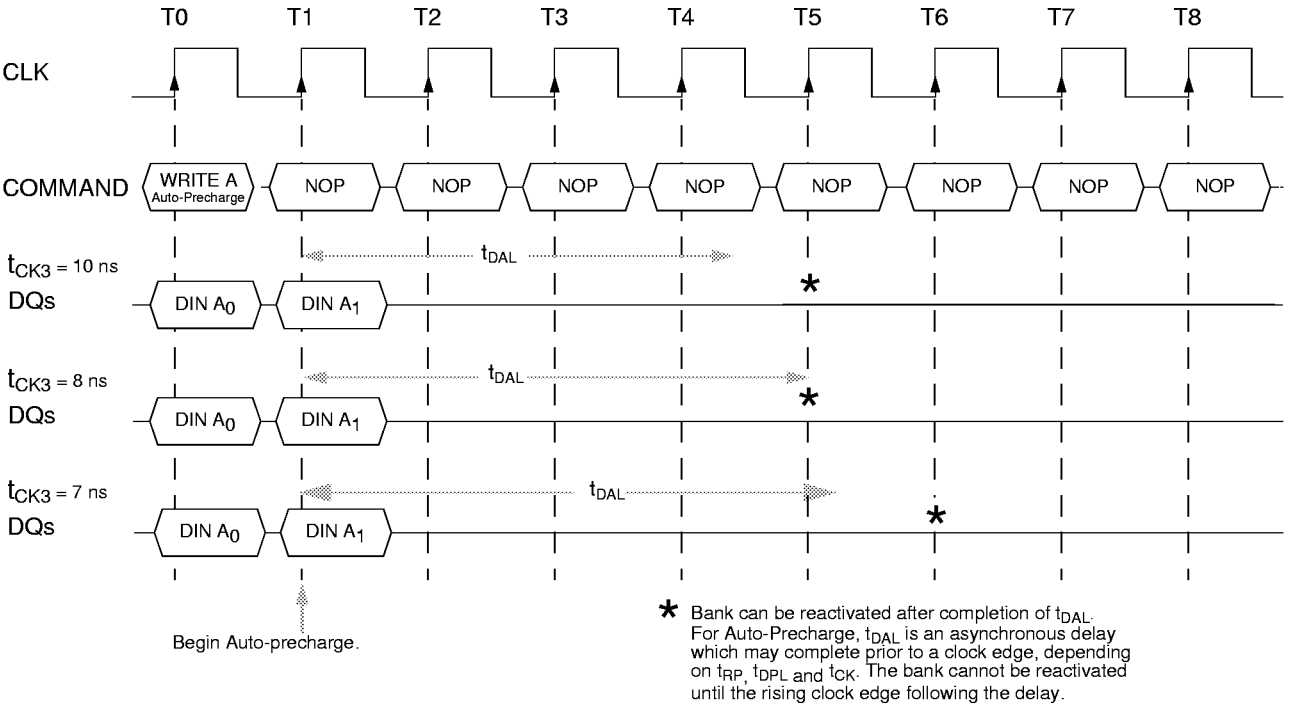
If A10 is high when a Read Command is issued, the Read with auto-precharge function is initiated. Once the precharge operation has started the bank cannot be reactivated until an asynchronous delay time equal to t_{RP} + t_{DPL}, expressed in nanoseconds rather than clocks, has been satisfied. It should be noted that the device will not respond to the Auto-Precharge Command if the device is programmed for full page burst read or write cycles.

Burst Read with Auto-Precharge (Burst Length = 4)



If A10 is high when a Write Command is issued, the Write with auto-precharge function is initiated. The bank undergoing auto-precharge can not be reactivated until t_{DPL} and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay (t_{DAL}= t_{DPL} + t_{RP}), and is an asynchronous delay time during auto-precharge.

Burst Write with Auto-Precharge (Burst Length = 2)



Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or both banks simultaneously. Two address bits A10 and A11 (BS) are used to define which bank(s) is to be precharged when the command is issued.

Bank Selection for Precharge by Address Bits

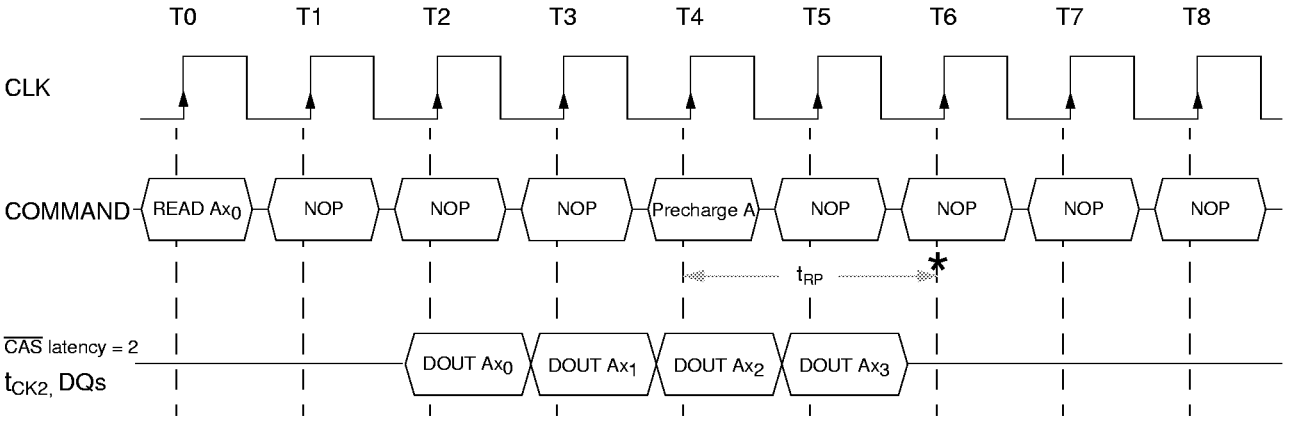
A10	BS(A11)	Precharged Bank(s)
LOW	LOW	Bank A only
LOW	HIGH	Bank B only
HIGH	DON'T CARE	Both Banks A and B

For read cycles, the Precharge Command may be applied consistent with the $\overline{CAS}$ Latency set in the Mode Register. The data DQs go to a high impedance state after a delay which is equal to the latency, similar to a Burst Stop Command. Refer to the following figures.

For write cycles, however, a delay must be satisfied from the start of the last burst write cycle until the Precharge Command can be issued. This delay is known as t_{DPL}, Data-in to Precharge delay.

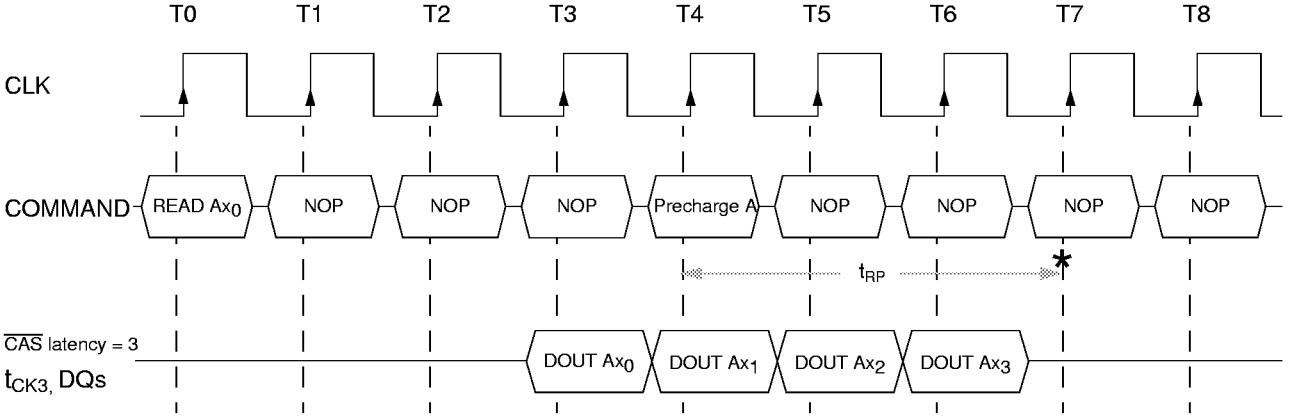
After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

Burst Read followed by Precharge Command (Burst Length = 4, $\overline{CAS}$ Latency = 2)



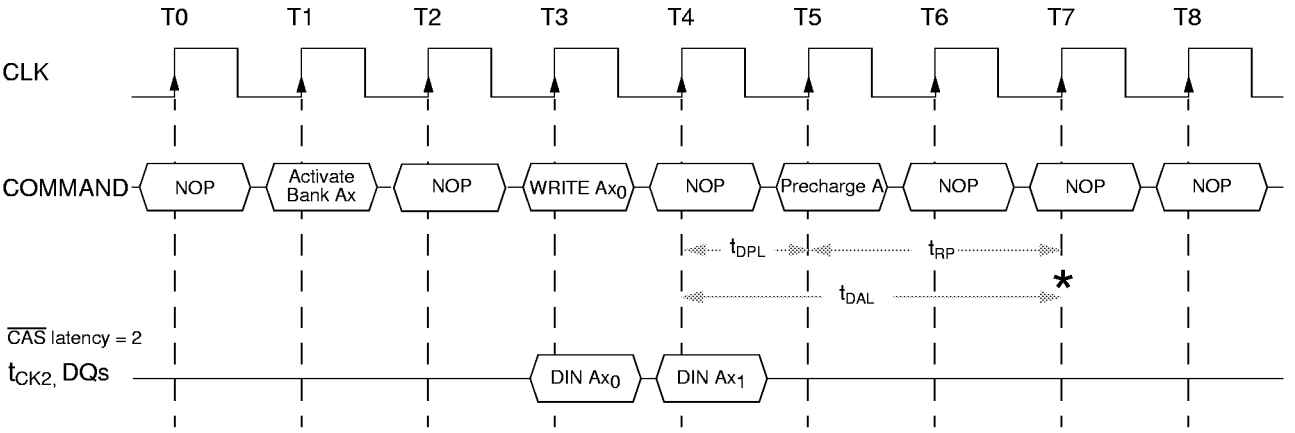
* Bank can be reactivated at completion of t_{RP}.

Burst Read followed by Precharge Command (Burst Length = 4, $\overline{CAS}$ Latency = 3)



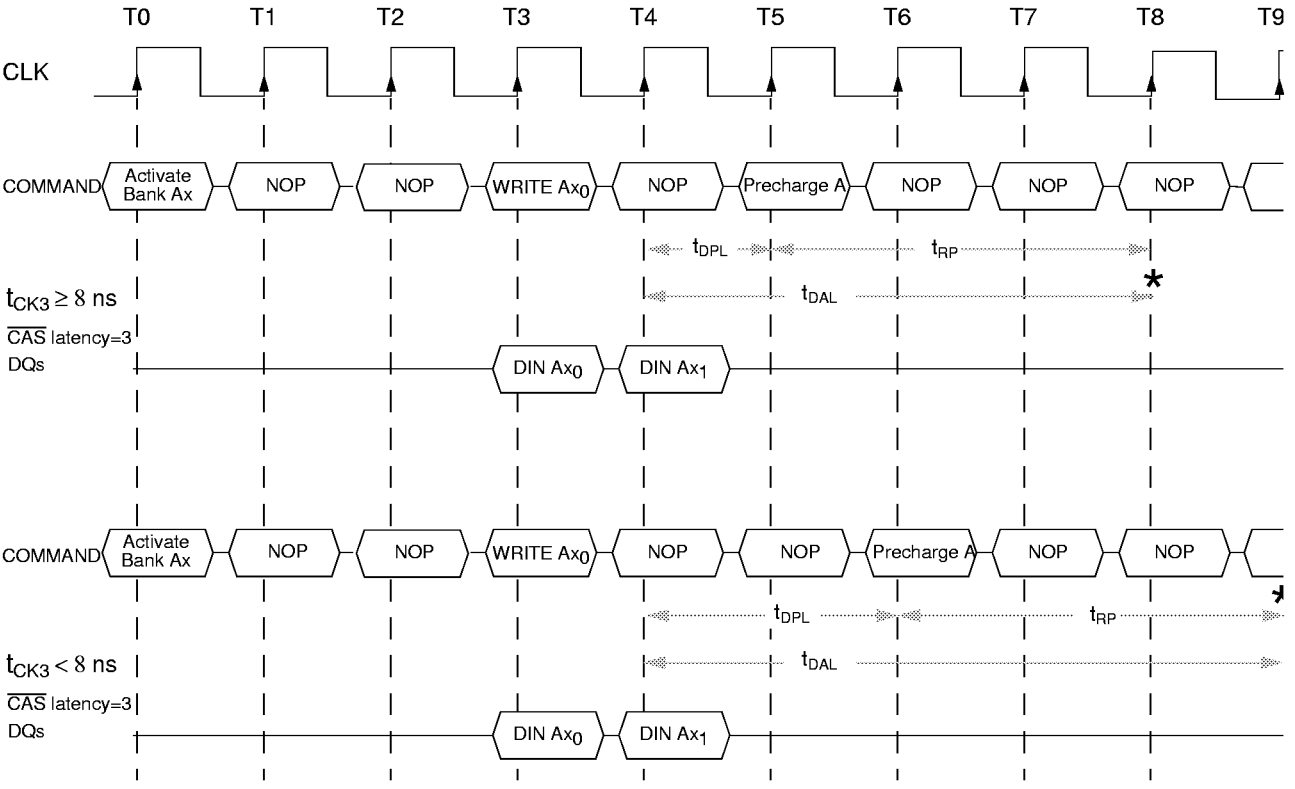
* Bank can be reactivated at completion of t_{RP}.

Burst Write followed by Precharge Command (Burst Length = 2, $\overline{CAS}$ Latency = 2)



* Bank can be reactivated at completion of t_{DAL} (t_{DPL} + t_{RP}).

Burst Write followed by Precharge Command (Burst Length = 2, $\overline{CAS}$ Latency = 3)

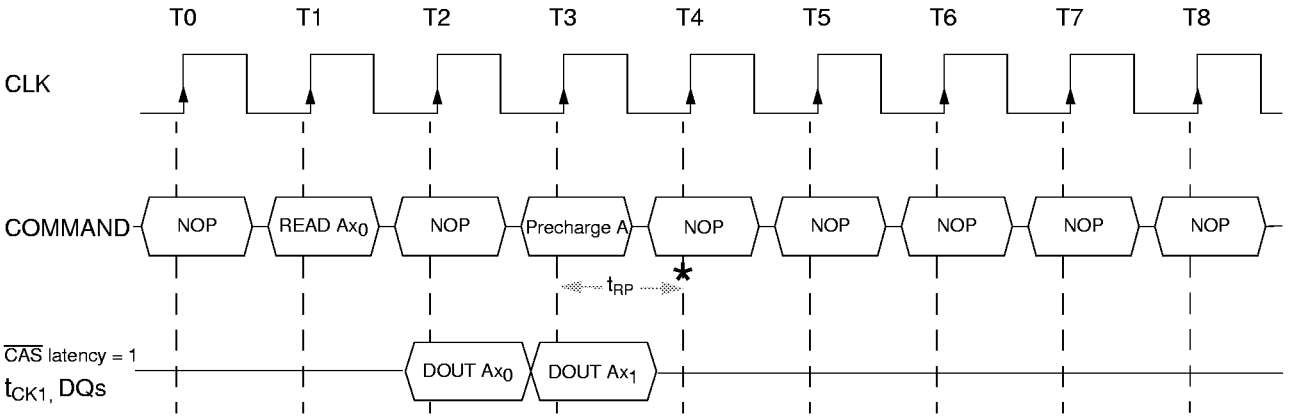


* Bank can be reactivated at completion of t_{DAL} (t_{DPL} + t_{RP}).

Precharge Termination

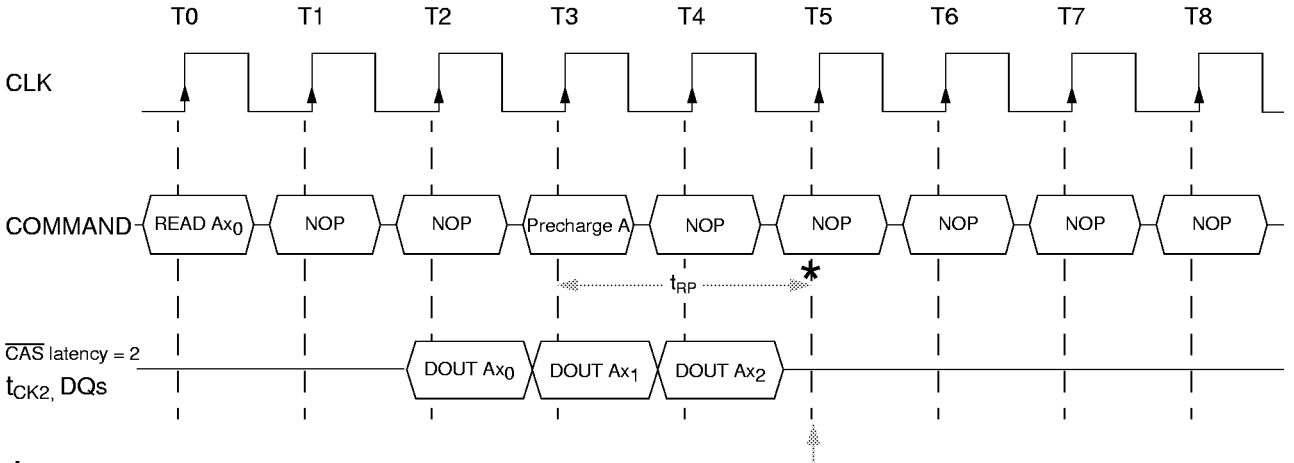
The Precharge Command may be used to terminate either a burst read or burst write operation. When the Precharge command is issued, the burst operation is terminated and bank precharge begins. For burst read operations, valid data will continue to appear on the data bus as a function of $\overline{CAS}$ Latency.

Burst Read Interrupted by Precharge (Burst Length = 8, $\overline{CAS}$ latency = 1)



* Bank can be reactivated at completion of t_{RP}.

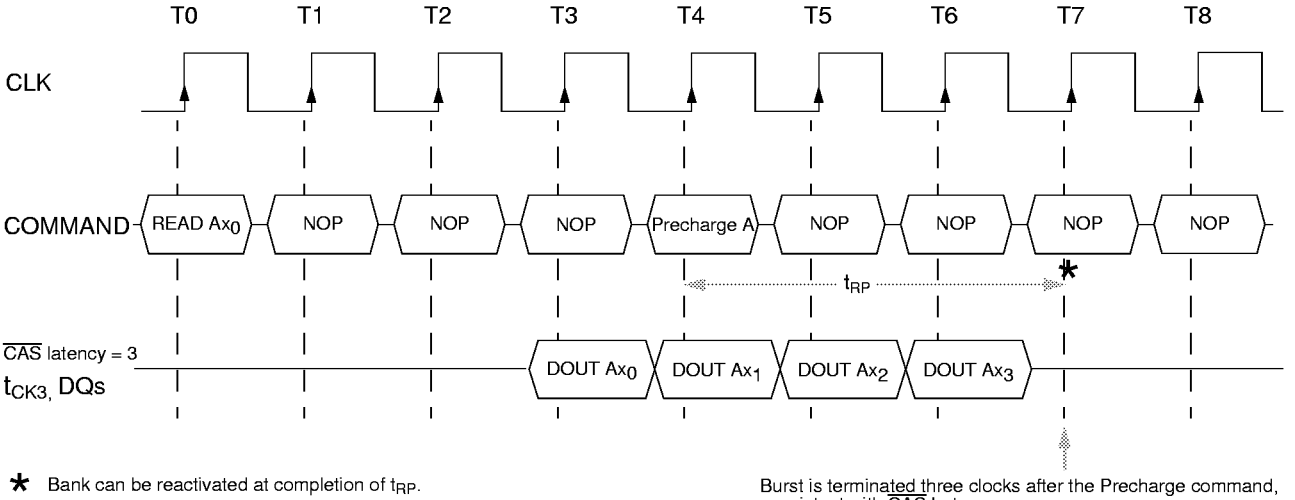
Burst Read Interrupted by Precharge (Burst Length = 8, $\overline{CAS}$ latency = 2)



* Bank can be reactivated at completion of t_{RP}.

Burst is terminated two clocks after the Precharge command, consistent with $\overline{CAS}$ Latency.

Burst Read Interrupted by Precharge (Burst Length = 8, $\overline{CAS}$ Latency = 3)



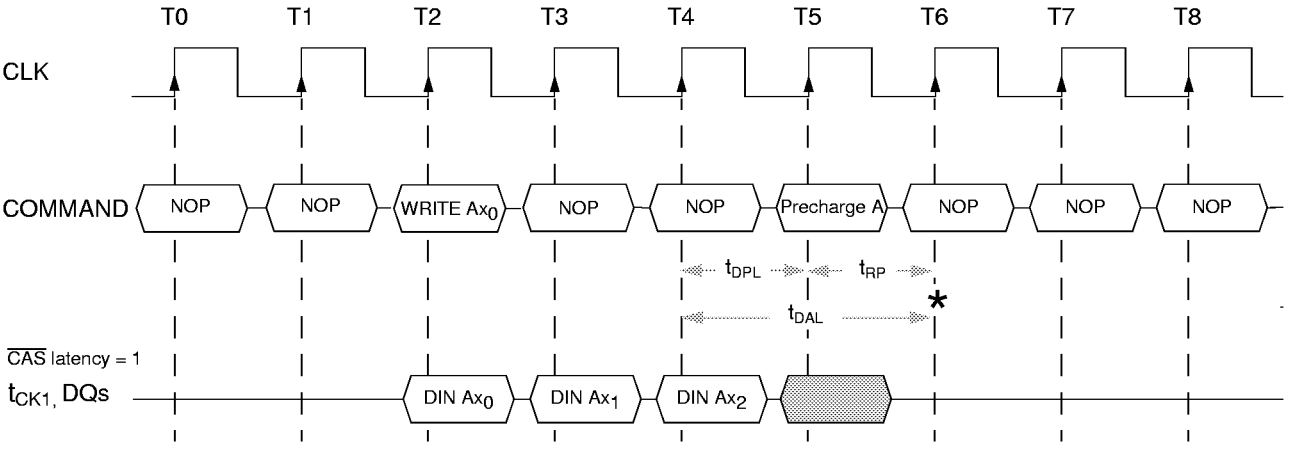
* Bank can be reactivated at completion of t_{RP}.

Burst is terminated three clocks after the Precharge command, consistent with $\overline{CAS}$ Latency.

Burst write operations will be terminated by the Precharge command. However, write data written to the device prior to the Precharge command may be stored incorrectly and is a function of $\overline{CAS}$ latency.

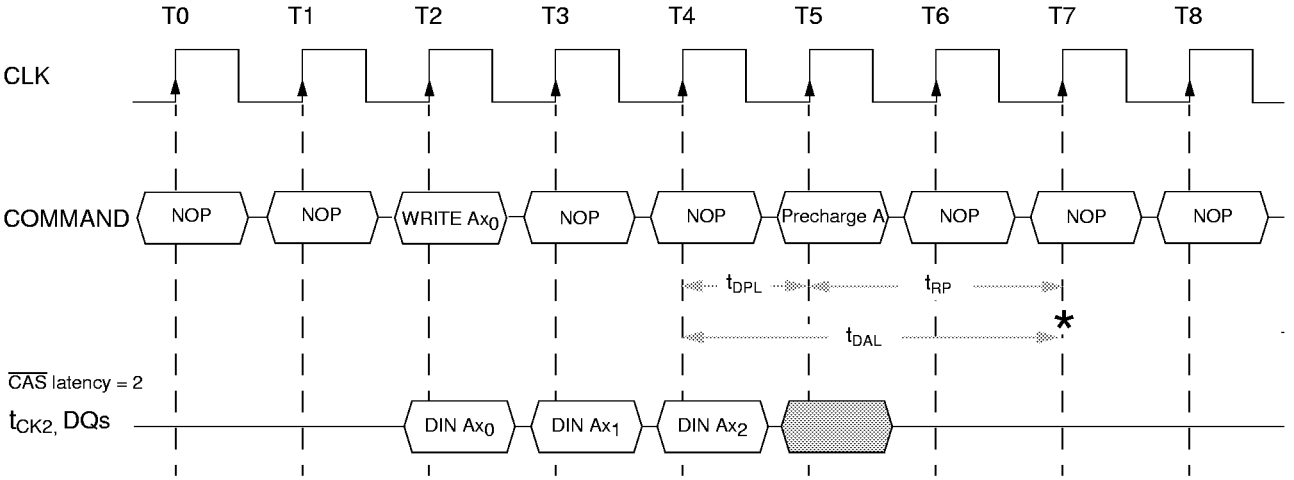
When $\overline{CAS}$ latency is set to equal 1 or 2 or when set to 3 with $t_{CK3} \geq 8$ ns, the last write data that will be properly stored in the device is that write data that is presented to the device on the clock cycle prior to the Precharge command. The write data presented during the Precharge command will not be written.

Precharge Termination of a Burst Write (Burst Length = 8, CAS Latency = 1)



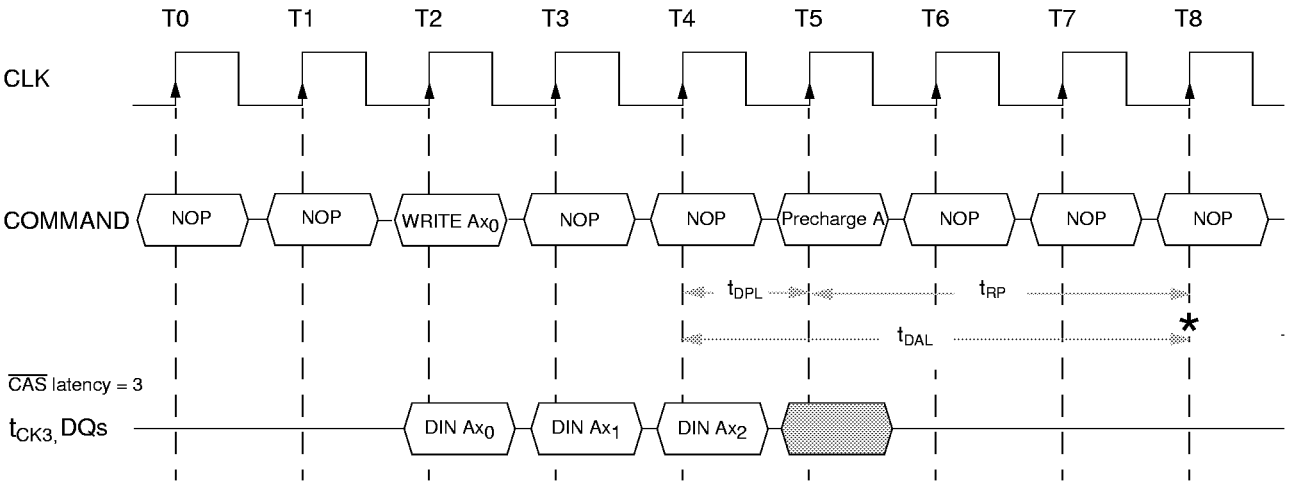
* Bank can be reactivated at completion of t_{DAL}

Precharge Termination of a Burst Write (Burst Length = 8, CAS Latency = 2)



* Bank can be reactivated at completion of t_{DAL}.

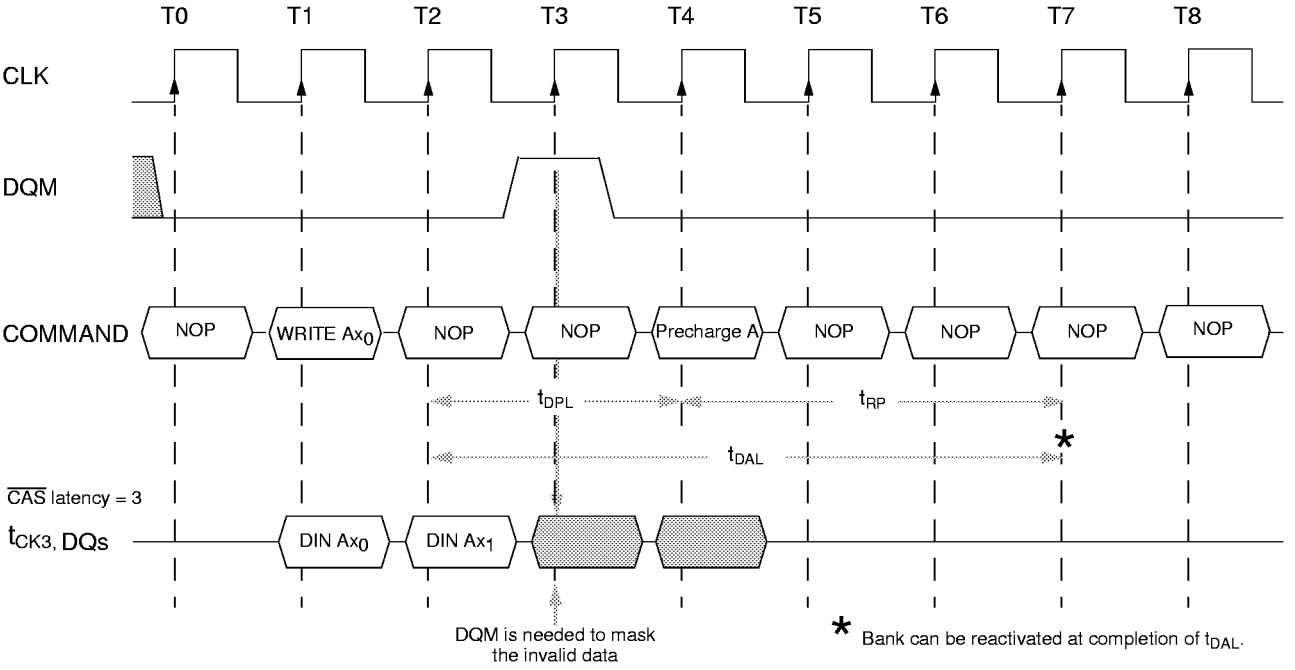
Precharge Termination of a Burst Write (Burst Length = 8, CAS Latency = 3, $t_{CK3} \geq 8$ ns



* Bank can be reactivated at completion of t_{DAL}.

When $\overline{CAS}$ latency is set to equal 3 and $t_{CK3} < 8$ ns, the last write data that will be properly stored in the device is that write data that is presented to the device two clocks prior to the Precharge command. The write data presented during the clock cycle prior to the Precharge command may be stored incorrectly. To prevent the writing of invalid data to the device, DQM must be asserted high one clock cycle prior to the Precharge command to mask the invalid write data.

Precharge Termination of a Burst Write (Burst Length = 8, CAS Latency = 3, $t_{CK3} < 8$ ns)



Automatic Refresh Command ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)

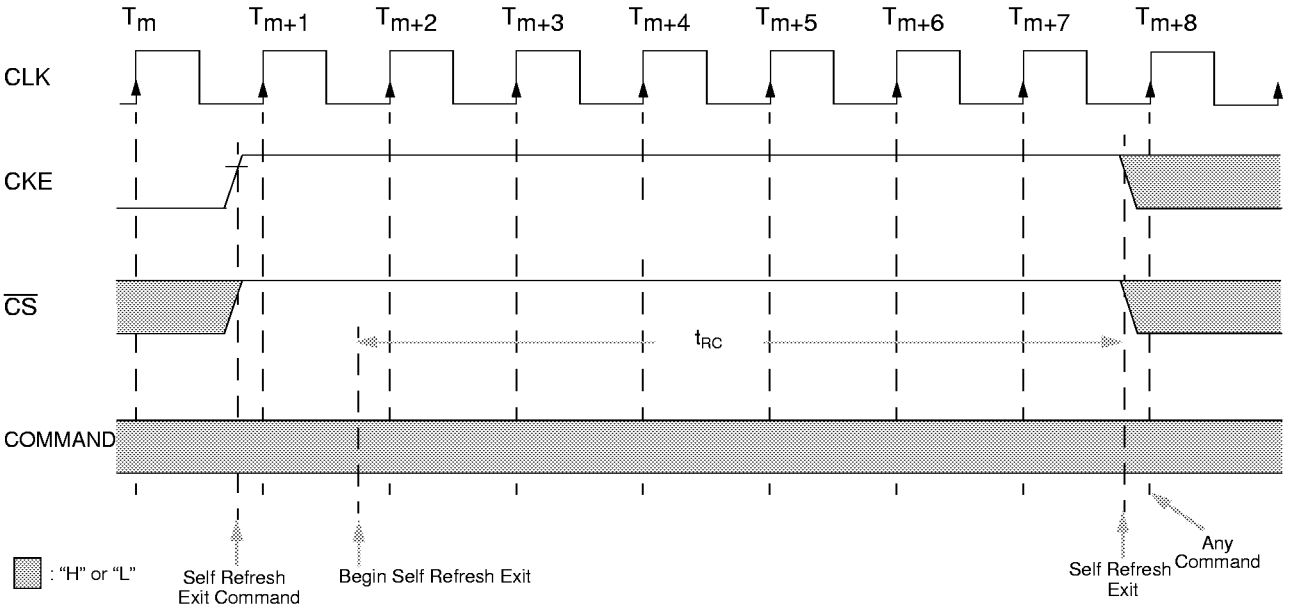
When $\overline{\text{CS}}$, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are held low with CKE and $\overline{\text{WE}}$ high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). Both banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto Refresh Command (CBR) can be applied. For a stacked device, only one deck at a time can be refreshed using Automatic Refresh Mode. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address pins is required once this cycle has started.

When the refresh cycle has completed, both banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the $\overline{\text{RAS}}$ cycle time (t_{RC}).

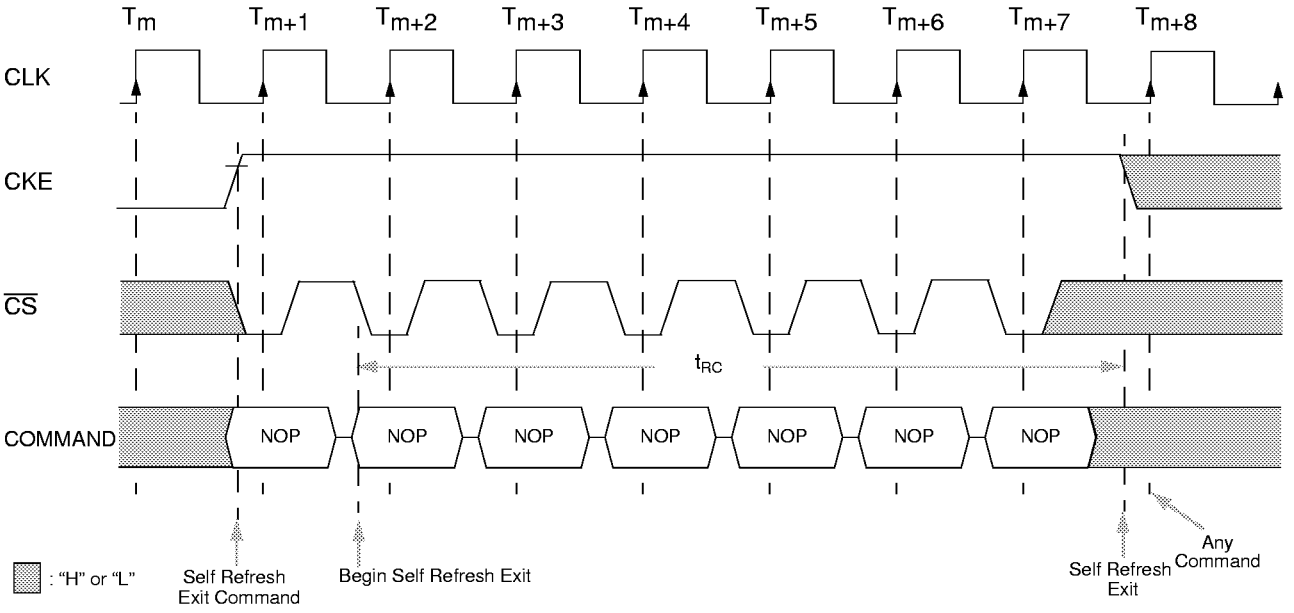
Self Refresh Command

The SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and CKE held low with $\overline{\text{WE}}$ high at the rising edge of the clock. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. Once the clock is cycling, the exit command will be registered asynchronously by bringing CKE high. After CKE is brought high, an internal timer is started to insure CKE is held high for approximately 10ns before registering the Self Refresh exit command. The purpose of this circuit is to filter out noise glitches on the CKE input which may cause the SDRAM to erroneously exit Self Refresh operation. Once the Self Refresh command is registered, a delay equal to the $\overline{\text{RAS}}$ cycle time (t_{RC}) must be satisfied before any new command can be issued to the device. CKE must remain high for the entire Self Refresh exit period (t_{SREX}) and commands must be gated off with $\overline{\text{CS}}$ held high. Alternatively, NOP commands may be registered on each positive clock edge during the Self Refresh exit interval. (See Self Refresh Exit figures.) When using Self Refresh, both decks of a stacked device may be refreshed at the same time.

Self Refresh Exit (Commands Gated Off with $\overline{\text{CS}}$ High)



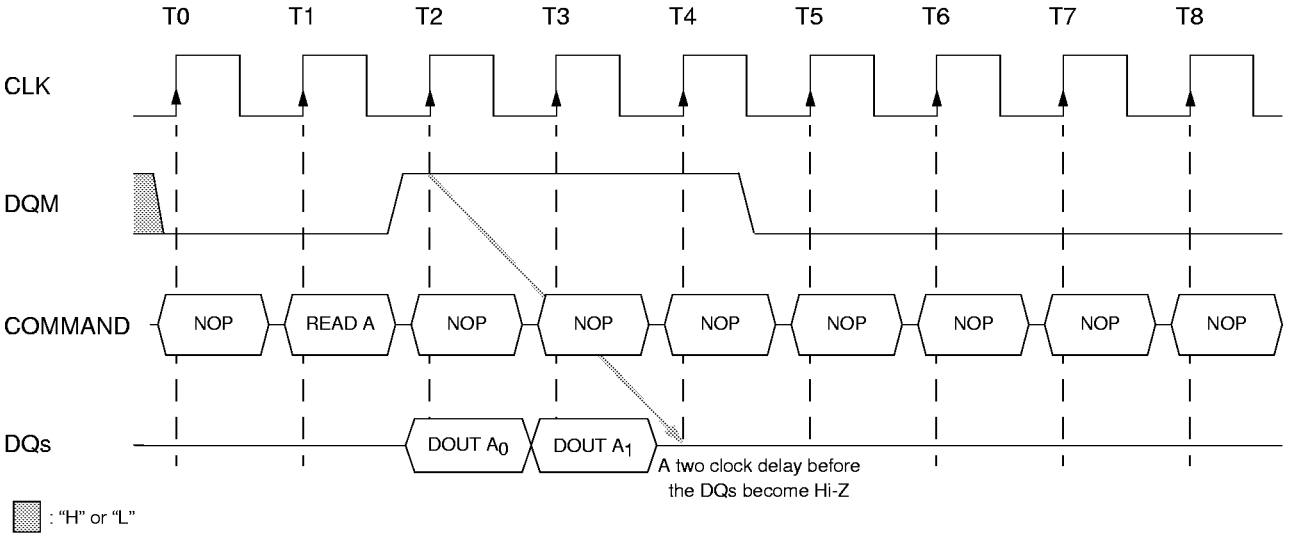
Self Refresh Exit (Commands Gated Off with NOP Commands)



Data Mask

The SDRAM has a Data Mask function that can be used in conjunction with data read and write cycles. When the Data Mask is high during a write cycle, the write operation is prohibited immediately (zero clock latency). If the Data Mask is activated during a read cycle, the data outputs are disabled and become high impedance after a two clock delay, independent of $\overline{CAS}$ latency.

Data Mask Activated During a Read Cycle (Burst Length = 4, $\overline{CAS}$ Latency = 1)



No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

Power Down Mode

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

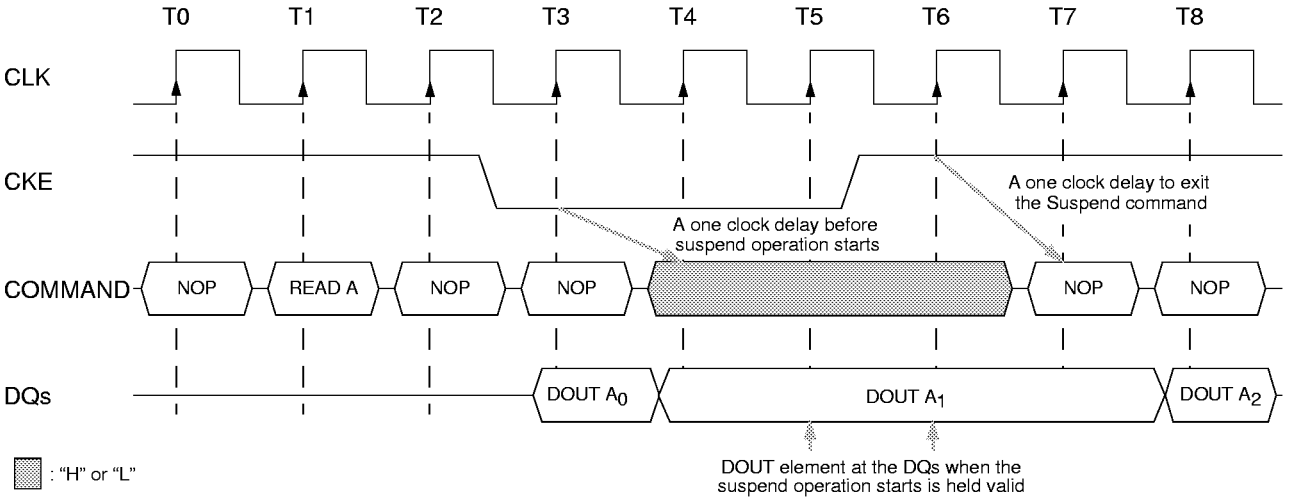
The Power Down mode is exited by bringing CKE high. A one clock delay after the registration of CKE high is required for the SDRAM to exit the Power Down mode.

Clock Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends or "freezes" any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SDRAM's operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

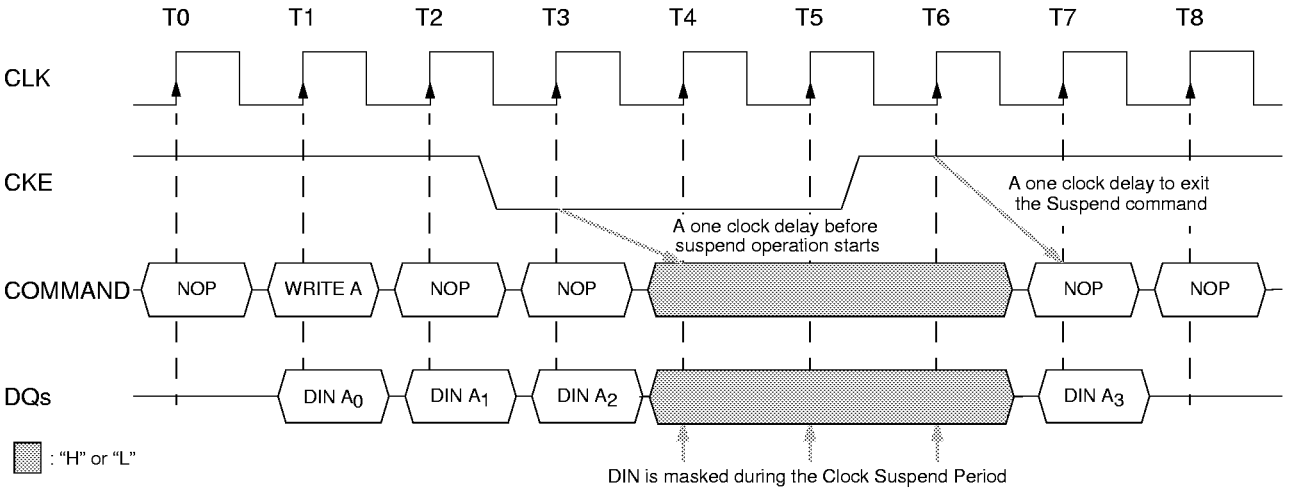
When the operation of the SDRAM is suspended during the execution of a Burst Read operation, the last valid data output onto the DQ pins will be actively held valid until Clock Suspend mode is exited.

Clock Suspend During a Read Cycle (Burst Length = 4, $\overline{CAS}$ latency = 2)



If Clock Suspend mode is initiated during a burst write operation, then the input data is masked and ignored until the Clock Suspend mode is exited.

Clock Suspend During a Write Cycle (Burst Length = 4, $\overline{CAS}$ Latency = 2)



Command Truth Table (Notes: 1)

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Mode Register Set	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	L	H	H	X	X	X	X	X	X	X	
Single Bank Precharge	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	H	X	L	L	H	L	X	X	H	X	
Bank Activate	H	X	L	L	H	H	X	BS	Row Address		2
Write	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	H	X	L	H	L	L	X	BS	H	Column	2
Read	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	H	X	L	H	L	H	X	BS	H	Column	2
Burst Termination	H	X	L	H	H	L	X	X	X	X	3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Clock Suspend/Standby Mode	L	X	X	X	X	X	X	X	X	X	4
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X	5
Power Down Mode Entry	X	L	X	X	X	X	X	X	X	X	6, 7
Power Down Mode Exit	X	H	X	X	X	X	X	X	X	X	6, 7

1. All of the SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.For stacked devices: only one deck can be operated at once, except during Self Refresh.
2. Bank Select (BS), if BS = 0 then bank A is selected, if BS = 1 then bank B is selected.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the $\overline{CAS}$ latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
7. If $\overline{CS}$ is low, then when CKE returns high, no command is registered into the chip for one clock cycle.

Clock Enable (CKE) Truth Table

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

1. For the given Current State, CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CES}) must be satisfied before any command other than Exit is issued.
3. The address inputs (A11 - A0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Power Down Mode, Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

Current State Truth Table (Part 1 of 4) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2, 3
	L	L	H	L	BS	X	Precharge	No Operation	
	L	L	H	H	BS	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BS	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BS	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Precharge	6
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto-Precharge	7, 8
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto-Precharge	7, 8
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start the Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start a new Read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. Both Banks must be idle; otherwise it is an illegal action.
3. If CKE is active (high), the SDRAM will start the Auto (CBR) Refresh operation. If CKE is inactive (low), then the Self Refresh mode is entered.
4. The Current State only refers to one of the banks. If BS selects this bank, then the action is illegal. If BS selects the bank not being referenced by the Current State, then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low), then the Power Down mode is entered. Otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Current State Truth Table (Part 2 of 4) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start a new Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start the Read cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto-Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto-Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. Both Banks must be idle; otherwise it is an illegal action.
3. If CKE is active (high), the SDRAM will start the Auto (CBR) Refresh operation. If CKE is inactive (low), then the Self Refresh mode is entered.
4. The Current State only refers to one of the banks. If BS selects this bank, then the action is illegal. If BS selects the bank not being referenced by the Current State, then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low), then the Power Down mode is entered. Otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Current State Truth Table (Part 3 of 4) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4, 10
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Row Active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{RCD}	
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto-Precharge	9
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto-Precharge	9
	L	H	H	L	X	X	Burst Termination	No Operation; Row Active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{DPL}	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. Both Banks must be idle; otherwise it is an illegal action.
3. If CKE is active (high), the SDRAM will start the Auto (CBR) Refresh operation. If CKE is inactive (low), then the Self Refresh mode is entered.
4. The Current State only refers to one of the banks. If BS selects this bank, then the action is illegal. If BS selects the bank not being referenced by the Current State, then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low), then the Power Down mode is entered. Otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Current State Truth Table (Part 4 of 4) (Notes: 1)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10 - A0	Description		
Write Recovering with Auto-Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4, 9
	L	H	L	H	BS	Column	Read	ILLEGAL	4, 9
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. Both Banks must be idle; otherwise it is an illegal action.
3. If CKE is active (high), the SDRAM will start the Auto (CBR) Refresh operation. If CKE is inactive (low), then the Self Refresh mode is entered.
4. The Current State only refers to one of the banks. If BS selects this bank, then the action is illegal. If BS selects the bank not being referenced by the Current State, then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low), then the Power Down mode is entered. Otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Power Supply Voltage	-1.0 to +4.6	V	1
VDDQ	Power Supply Voltage for Output	-1.0 to +4.6	V	1
V_{IN}	Input Voltage	-1.0 to +4.6	V	1
V_{OUT}	Output Voltage	-1.0 to +4.6	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (LVTTL) (T_A= 0 to 70˚C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	3.0	3.3	3.6	V	1
VDDQ	Supply Voltage for Output	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	VDD + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS} and VSSQ.

Recommended DC Operating Conditions (SSTL_3) (T_A= 0 to 70˚C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	VDDQ	—	3.6	V	1
VDDQ	Supply Voltage for Output	3.0	3.3	3.6	V	1, 2
VREF	Input Reference Voltage	1.3	1.5	1.7		1, 3, 4
VTT	Termination Voltage	VREF-0.05	VREF	VREF+0.05		1, 5
V_{IH} (DC)	Input High Voltage	VREF+0.2	—	VDDQ + 0.3	V	1
V_{IL} (DC)	Input Low Voltage	-0.3	—	VREF-0.2	V	1

1. All voltages referenced to V_{SS} and VSSQ.
2. Under all conditions VDDQ must be less than or equal to VDD.
3. VREF is expected to be 0.45 * VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
4. Peak to peak ac noise on VREF may not exceed 2% VREF (DC).
5. VTT of transmitting device must track VREF of receiving device.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	2.0	2.7	4.0	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM)	2.0	2.7	4.0	pF	1
C_O	Output Capacitance (DQ0 - DQ15)	2.0	4.0	5.0	pF	1

1. Multiply given planar values by 2 for 2-High stacked device.

Output Characteristics (LVTTL) (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Min.	Max.	Units
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	-1	+1	µA
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	-1	+1	µA
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -2.0mA)	2.4	VDDQ	V
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +2.0mA)	0.0	0.4	V

Output Characteristics (SSTL_3) (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.8	V	1
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} – 0.8	V	1
V_{OTR}	Output Timing Measurement Reference Level	0.45*V_{DDQ}	V	2
I_{OH}	Output Minimum Source DC Current	16	mA	3, 4, 6
I_{OL}	Output Minimum Sink DC Current	16	mA	4, 5, 6
RT1, RT2	Termination Resistor	50	Ω	
RS	Series Resistor	25	Ω	

1. Since V_{IN} must be at least 0.4V above or below V_{REF} as a result of V_{OUT}, using a series resistor of 25Ω for a Class II output driver translates into the minimum requirement of a 0.8V swing relative to V_{TT}.
2. The V_{DDQ} of the device under test is referenced.
3. V_{DDQ} = 3.0V; V_{OUT} = V_{DDQ} – 0.9V.
4. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
5. V_{DDQ} = 3.0V; V_{OUT} = 0.5V.
6. The values of $I_{OH\ (DC)}$ and $I_{OL(DC)}$ are based on V_{DDQ} =3.0V and V_{TT} =1.3V. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_3 receiver. Under these conditions V_{OH} is 2.1 V and V_{OL} is 0.5 V.

Standby and Refresh Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V) (Notes: 1)

Parameter	Symbol	Test Condition		Organization x4	Organization x8	Organization x16	Units	Notes
Precharge Standby Current in Power Down Mode	$I_{CC1}P$	CKE ≤ V_{IL}(max), t_{CK} = 15ns		3	3	3	mA	2
	$I_{CC1}PS$	CKE ≤ V_{IL}(max), t_{CK} = Infinity		2	2	2	mA	
Precharge Standby Current in Non-Power Down Mode	$I_{CC1}N$	CKE ≥ V_{IH}(min), t_{CK} = 15ns Input Change every 30ns		25	25	25	mA	$\overline{CS}$=High 2
	$I_{CC1}NS$	CKE ≥ V_{IH}(min), t_{CK} = Infinity No Input Change		10	10	10	mA	2
Active Standby Current in Power Down Mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CK} = 15ns		3	3	3	mA	3, 11
	$I_{CC2}PS$	CKE ≤ V_{IL}(max), t_{CK} = Infinity		2	2	2	mA	4, 11
Active Standby Current in Non-Power Down Mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), t_{CK} = 15ns Input Change every 30ns		25	25	25	mA	$\overline{CS}$=High 5
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), t_{CK} = Infinity No Input Change		15	15	15	mA	6
Auto (CBR) Refresh Current	I_{CC3}	$\overline{CAS}$ Latency = 1 t_{RC} ≥ t_{RC}(min)	-10 (LVTTL)	85	85	85	mA	7, 8, 9, 10
		$\overline{CAS}$ Latency = 2 t_{RC} ≥ t_{RC}(min)	-70 (SSTL)	105	105	105	mA	
			-80 (SSTL)	95	95	95		
			-80 (LVTTL)	110	110	110		
			-10 (LVTTL)	90	90	90		
		$\overline{CAS}$ Latency = 3 t_{RC} ≥ t_{RC}(min)	-70 (SSTL)	135	135	135	mA	
			-80 (SSTL)	120	120	120		
			-80 (LVTTL)	140	140	140		
			-10 (LVTTL)	110	110	110		

1. For stacked devices: only one deck may be active at a time, except during self refresh.
2. For stacked devices: multiply the given planar (individual deck) values by 2.
3. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}P$ + $I_{CC1}P$).
4. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}PS$ + $I_{CC1}PS$).
5. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}N$ + $I_{CC1}N$).
6. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}NS$+ $I_{CC1}NS$).
7. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck (I_{CC3} + $I_{CC1}N$).
8. The specified values are valid when addresses are changed no more than once during t_{CK}(min).
9. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
10. The specified values are valid when data inputs (DQs) are stable during t_{RC}(min).
11. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).

Standby and Refresh Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V) (Notes: 1)

Parameter	Symbol	Test Condition	Organization			Units	Notes
			x4	x8	x16		
Self Refresh Current (Standard Power)	I_{CC4}	CKE ≤ 0.2V	2	2	2	mA	2
Self Refresh Current (Low Power)	I_{CC4}	CKE ≤ 0.2V	500	500	500	µA	2

1. For stacked devices: only one deck may be active at a time, except during self refresh.
2. For stacked devices: multiply the given planar (individual deck) values by 2.
3. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}P + I_{CC1}P$).
4. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}PS + I_{CC1}PS$).
5. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}N + I_{CC1}N$).
6. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC2}NS+ I_{CC1}NS$).
7. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck ($I_{CC3} + I_{CC1}N$).
8. The specified values are valid when addresses are changed no more than once during t_{CK}(min).
9. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
10. The specified values are valid when data inputs (DQs) are stable during t_{RC}(min).
11. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).

Operating Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Speed Sort	Organization			Units	Notes
						X4	X8	X16		
I_{CC5}	Operating Current Burst Length = 1	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	90 ns	-10 (LVTTL)	95	95	95	mA	1, 2, 3
			CL=2	66 ns	-70 (SSTL)	120	120	125	mA	
				72 ns	-80 (SSTL)	110	110	115		
				72 ns	-80 (LVTTL)	130	130	135		
				90 ns	-10 (LVTTL)	105	105	110		
			CL=3	63 ns	-70 (SSTL)	150	150	155	mA	
				72 ns	-80 (SSTL)	130	130	135		
				72 ns	-80 (LVTTL)	155	155	160		
				90 ns	-10 (LVTTL)	125	125	130		
I_{CC6}	Operating Current Burst Length = 2	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	120 ns	-10 (LVTTL)	75	75	80	mA	1, 2, 3, 4
			CL=2	77 ns	-70 (SSTL)	115	115	120	mA	
				84 ns	-80 (SSTL)	105	105	110		
				84 ns	-80 (LVTTL)	125	125	130		
				105 ns	-10 (LVTTL)	100	100	105		
			CL=3	70 ns	-70 (SSTL)	155	155	160	mA	
				80 ns	-80 (SSTL)	135	135	140		
				80 ns	-80 (LVTTL)	155	155	160		
				100 ns	-10 (LVTTL)	125	125	130		

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQs are changed no more than once during t_{CK}(min).
3. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck (Operating Current+ $I_{CC1}N$).
4. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.

Operating Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Speed Sort	Organization			Units	Notes
						X4	X8	X16		
I_{CC7}	Operating Current Burst Length = 4	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	180 ns	-10 (LVTTL)	65	65	70	mA	1, 2, 3, 4
			CL=2	99 ns	-70 (SSTL)	105	110	115	mA	
				108 ns	-80 (SSTL)	95	100	105		
				108 ns	-80 (LVTTL)	110	115	120		
				135 ns	-10 (LVTTL)	90	95	100		
			CL=3	84 ns	-70 (SSTL)	150	155	160	mA	
				96 ns	-80 (SSTL)	130	135	140		
				96 ns	-80 (LVTTL)	150	155	160		
				120 ns	-10 (LVTTL)	120	125	130		
I_{CC8}	Operating Current Burst Length = 8	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	300 ns	-10 (LVTTL)	55	60	65	mA	1, 2, 3, 4
			CL=2	143 ns	-70 (SSTL)	100	105	115	mA	
				156 ns	-80 (SSTL)	90	95	105		
				156 ns	-80 (LVTTL)	105	110	120		
				195 ns	-10 (LVTTL)	85	90	100		
			CL=3	112 ns	-70 (SSTL)	150	155	160	mA	
				128 ns	-80 (SSTL)	130	135	140		
				128 ns	-80 (LVTTL)	150	155	165		
				160 ns	-10 (LVTTL)	120	125	135		

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQs are changed no more than once during t_{CK}(min).
3. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck (Operating Current+ I_{CC1}N).
4. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.

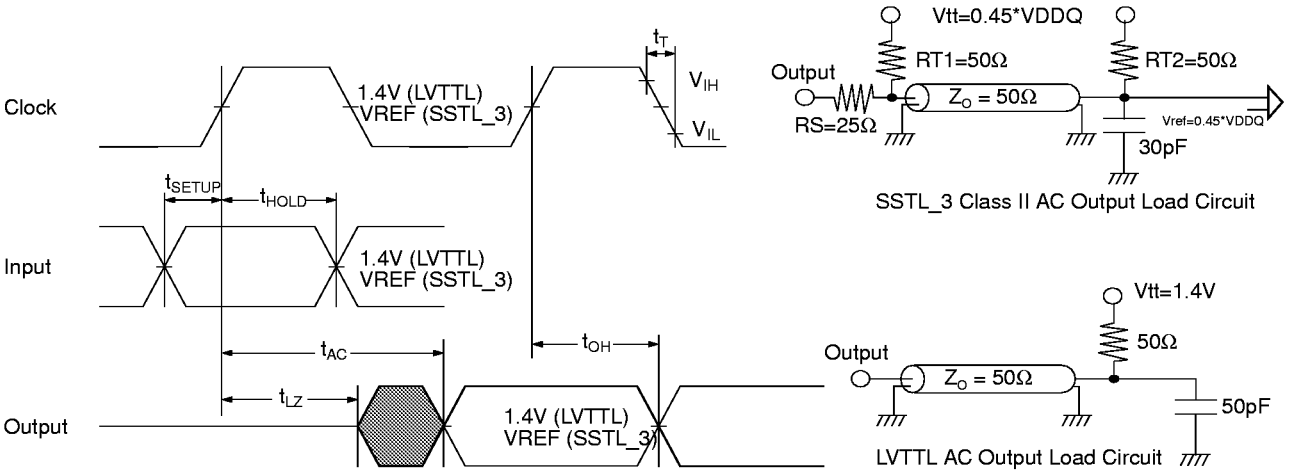
Operating Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Speed Sort	Organization X4	Organization X8	Organization X16	Units	Notes
I_{CC9}	Operating Current Burst Length = Full Page	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	t_{RC} = ∞ t_{CK}=30 ns	-10 (LVTTL)	40	45	55	mA	1, 2, 3, 4
			CL=2	t_{RC} = ∞ t_{CK}=11 ns	-70 (SSTL)	80	85	105	mA	
				t_{RC} = ∞ t_{CK}=12 ns	-80 (SSTL)	75	80	95		
				t_{RC} = ∞ t_{CK}=12 ns	-80 (LVTTL)	90	95	110		
				t_{RC} = ∞ t_{CK}=15 ns	-10 (LVTTL)	70	75	90		
			CL=3	t_{RC} = ∞ t_{CK}=7 ns	-70 (SSTL)	120	125	165	mA	
				t_{RC} = ∞ t_{CK}=8 ns	-80 (SSTL)	105	110	145		
				t_{RC} = ∞ t_{CK}=8 ns	-80 (LVTTL)	125	130	170		
				t_{RC} = ∞ t_{CK}=10 ns	-10 (LVTTL)	100	105	135		
I_{CC10}	Operating Current 1-N Rule (Continuous Read/Write cycles with new column address registered each clock cycle)	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	t_{RC} = ∞ t_{CK}=30 ns	-10 (LVTTL)	85	85	90	mA	1, 2, 3
			CL=2	t_{RC} = ∞ t_{CK}=11 ns	-70 (SSTL)	155	155	160	mA	
				t_{RC} = ∞ t_{CK}=12 ns	-80 (SSTL)	140	140	150		
				t_{RC} = ∞ t_{CK}=12 ns	-80 (LVTTL)	165	165	175		
				t_{RC} = ∞ t_{CK}=15 ns	-10 (LVTTL)	130	130	140		
			CL=3	t_{RC} = ∞ t_{CK}=7 ns	-70 (SSTL)	210	210	230	mA	
				t_{RC} = ∞ t_{CK}=8 ns	-80 (SSTL)	190	190	205		
				t_{RC} = ∞ t_{CK}=8 ns	-80 (LVTTL)	220	220	240		
				t_{RC} = ∞ t_{CK}=10 ns	-10 (LVTTL)	175	175	190		

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQs are changed no more than once during t_{CK}(min).
3. For stacked devices: this is the active portion only.The total stack current includes the Precharge Standby current of the inactive deck (Operating Current+ I_{CC1}N).
4. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.

AC Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point (LVTTL).
3. AC timing tests have V_{IL} = VREF - 0.4 and V_{IH} = VREF + 0.4 with the timing referenced to the VREF crossover point (SSTL_3)
4. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
5. AC measurements assume t_T=1ns.
6. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.



SSTL_3 Input AC Logic Levels

Symbol	Parameter	Min	Max	Units
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.40	—	V
V_{IL} (AC)	AC Input Logic Low	—	V_{REF}-0.40	V

SSTL_3 AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{REF}	Input Reference Voltage	0.45*V_{DDQ}	V	1
V_{SWING} (max)	Input Signal Maximum Peak to Peak Swing	2.0	V	1, 2
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns	3

1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IH} min (AC) range of the input signal swing.

Clock and Clock Enable Parameters

Symbol	Parameter	SSTL_3				LVTTL				Units	Notes
		-70		-80		-80		-10			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK3}	Clock Cycle Time,$\overline{CAS}$ Latency=3	7	**143MHz**	8	**125MHz**	8	**125MHz**	10	**100MHz**	ns	
t_{CK2}	Clock Cycle Time,$\overline{CAS}$ Latency=2	11	**91MHz**	12	**83MHz**	12	**83MHz**	15	**66MHz**	ns	
t_{CK1}	Clock Cycle Time,$\overline{CAS}$ Latency=1	—	—	—	—	—	—	30	**33MHz**	ns	
t_{AC3}	Clock Access Time,$\overline{CAS}$ Latency=3	—	5	—	6	—	6	—	8	ns	1, 2
t_{AC2}	Clock Access Time,$\overline{CAS}$ Latency=2	—	6	—	7.5	—	7.5	—	9	ns	1, 2
t_{AC1}	Clock Access Time,$\overline{CAS}$ Latency=1	—	—	—	—	—	—	—	27	ns	1, 2
t_{CKH}	Clock High Pulse Width	2.5	—	3	—	3	—	3.5	—	ns	3
t_{CKL}	Clock Low Pulse Width	2.5	—	3	—	3	—	3.5	—	ns	3
t_{CES}	Clock Enable Set-up Time	2	—	2.5	—	2.5	—	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	1	—	1	—	1	—	ns	
t_{CESP}	CKE Set-up Time (Power down mode)	2	—	2.5	—	2.5	—	3	—	ns	
t_T	Transition Time (Rise and Fall)	1	30	1	30	1	30	1	30	ns	

1. Access time is measured at 1.4V (LVTTL) or VREF (SSTL_3). See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5)ns should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional [(trise+tfall)/2-1]ns.

Common Parameters

Symbol	Parameter	SSTL_3				LVTTL				Units
		-70		-80		-80		-10		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CS}	Command Setup Time	2	—	2.5	—	2.5	—	3	—	ns
t_{CH}	Command Hold Time	1	—	1	—	1	—	1	—	ns
t_{AS}	Address and Bank Select Set-up Time	2	—	2.5	—	2.5	—	3	—	ns
t_{AH}	Address and Bank Select Hold Time	1	—	1	—	1	—	1	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	21	—	24	—	24	—	30	—	ns
t_{RC}	Bank Cycle Time	63	120K	72	120K	72	120K	90	120K	ns
t_{RAS}	Active Command Period	42	120K	48	120K	48	120K	60	120K	ns
t_{RP}	Precharge Time	21	—	24	—	24	—	30	—	ns
t_{RRD}	Bank to Bank Delay Time	14	—	16	—	16	—	20	—	ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	1	—	1	—	1	—	1	—	CLK

Refresh Cycle

Symbol	Parameter	SSTL_3				LVTTL				Units	Notes
		-70		-80		-80		-10			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	—	**64**	—	**64**	—	**64**	—	**64**	ms	1, 2
t_{SREX}	Self Refresh Exit Time	10ns + t_{RC}	—	10ns + t_{RC}	—	10ns + t_{RC}	—	10ns + t_{RC}	—	ns	3

1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
3. Self Refresh Exit is an asynchronous operation. Self refresh exit is accomplished by starting the clock (CLK) and then asserting CKE high. During the exit time (t_{SREX}), no commands may be issued until tRC is satisfied and CKE must remain high. It is recommended to hold $\overline{CS}$ high during the self refresh exit time, but NOP commands may be issued with each rising clock edge during this period as an alternative. To prevent erroneous exit of self refresh operation, a glitch suppressor circuit is incorporated into the CKE receiver. If CKE is asserted high (system noise) for less than 10ns (approximately), then the device will not exit self refresh operation.

Read Cycle

Symbol	Parameter	SSTL_3				LVTTL				Units	Notes
		-70		-80		-80		-10			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{OH}	Data Out Hold Time	2	—	2.5	—	2.5	—	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	2	—	2.5	—	2.5	—	3	—	ns	
t_{HZ3}	Data Out to High Impedance Time,CL= 3	2	7	2.5	8	2.5	8	3	8	ns	1
t_{HZ2}	Data Out to High Impedance Time,CL= 2	2	8	2.5	8	2.5	8	3	10	ns	1
t_{HZ1}	Data Out to High Impedance Time,CL= 1	—	—	—	—	—	—	3	18	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	2	—	2	—	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	SSTL_3				LVTTL				Units
		-70		-80		-80		-10		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DS}	Data In Set-up Time	2	—	2.5	—	2.5	—	3	—	ns
t_{DH}	Data In Hold Time	1	—	1	—	1	—	1	—	ns
t_{DPL}	Data Input to Precharge	8	—	8	—	8	—	10	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	0	—	0	—	0	—	CLK

Clock Frequency and Latency

Symbol	Parameter	SSTL_3				LVTTL					Units
		-70		-80		-80		-10			
fCK	**Clock Frequency**	**143**	**91**	**125**	**83**	**125**	**83**	**100**	**66**	**33**	**MHz**
t_{CK}	Clock Cycle Time	7	11	8	12	8	12	10	15	30	ns
t_{AA}	$\overline{CAS}$ Latency	3	2	3	2	3	2	3	2	1	CLK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	3	2	3	2	3	2	3	2	1	CLK
t_{RL}	$\overline{RAS}$ Latency	6	4	6	4	6	4	6	4	2	CLK
t_{RC}	Bank Cycle Time	9	6	9	6	9	6	9	6	3	CLK
t_{RAS}	Minimum Bank Active Time	6	4	6	4	6	4	6	4	2	CLK
t_{RP}	Precharge Time	3	2	3	2	3	2	3	2	1	CLK
t_{DPL}	Data In to Precharge	2	1	1	1	1	1	1	1	1	CLK
t_{DAL}	Data In to Active/Refresh	5	3	4	3	4	3	4	3	2	CLK
t_{RRD}	Bank to Bank Delay Time	2	2	2	2	2	2	2	2	1	CLK
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	1	1	1	1	1	1	1	CLK
t_{WL}	Write Latency	0	0	0	0	0	0	0	0	0	CLK
t_{DQW}	DQM Write Mask Latency	0	0	0	0	0	0	0	0	0	CLK
t_{DQZ}	DQM Data Disable Latency	2	2	2	2	2	2	2	2	2	CLK
t_{CSL}	Clock Suspend Latency	1	1	1	1	1	1	1	1	1	CLK

Timing Diagrams

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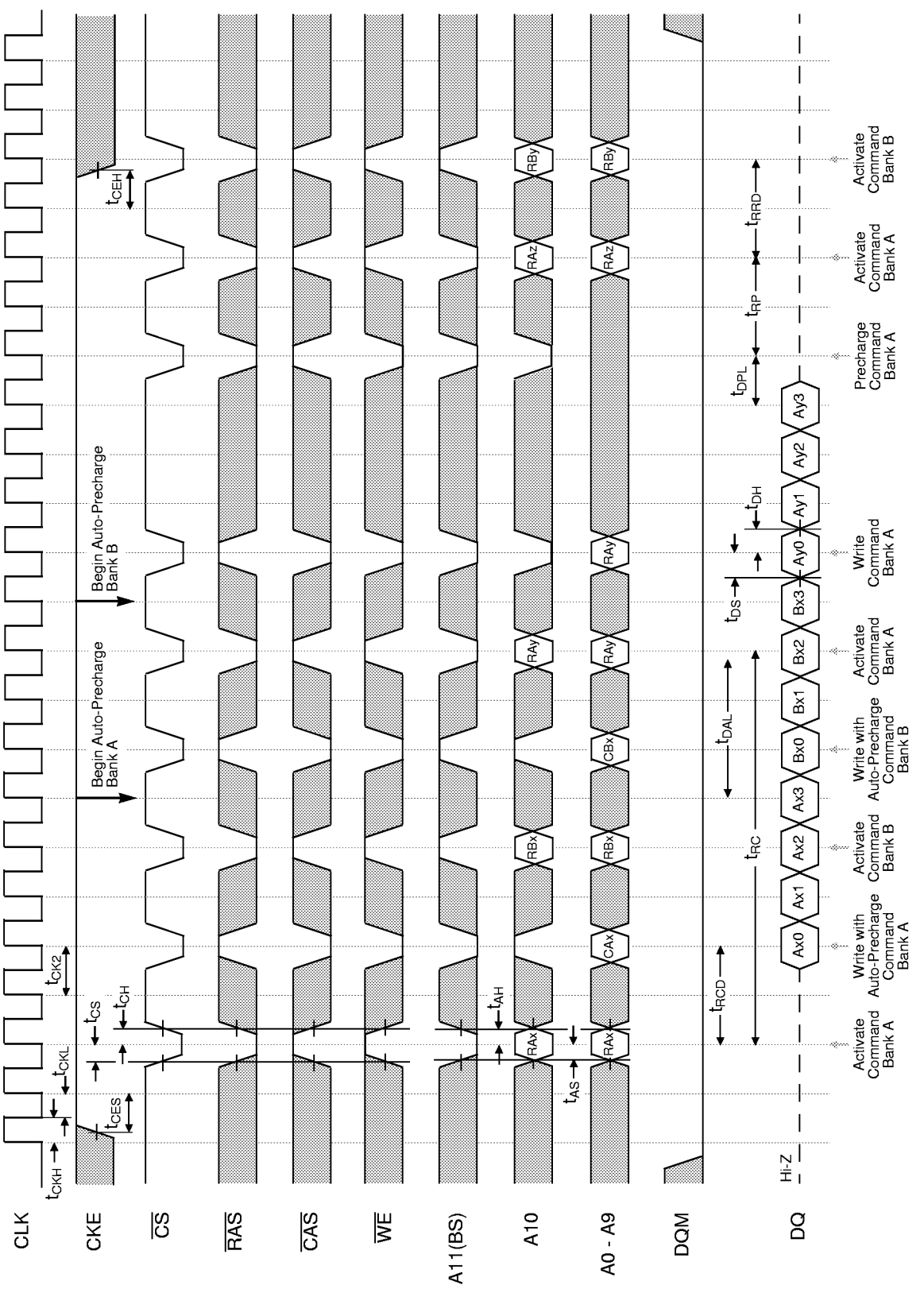
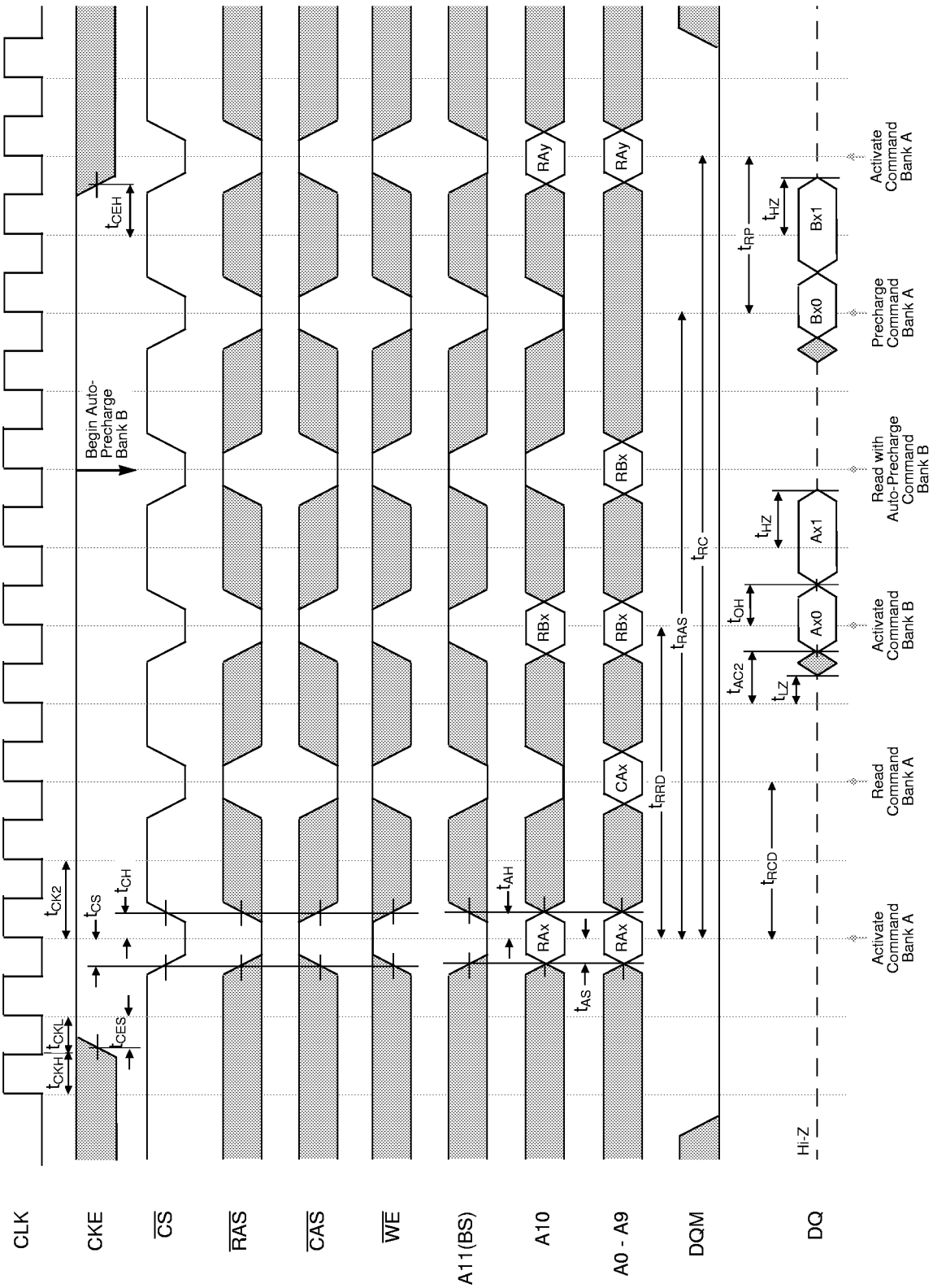
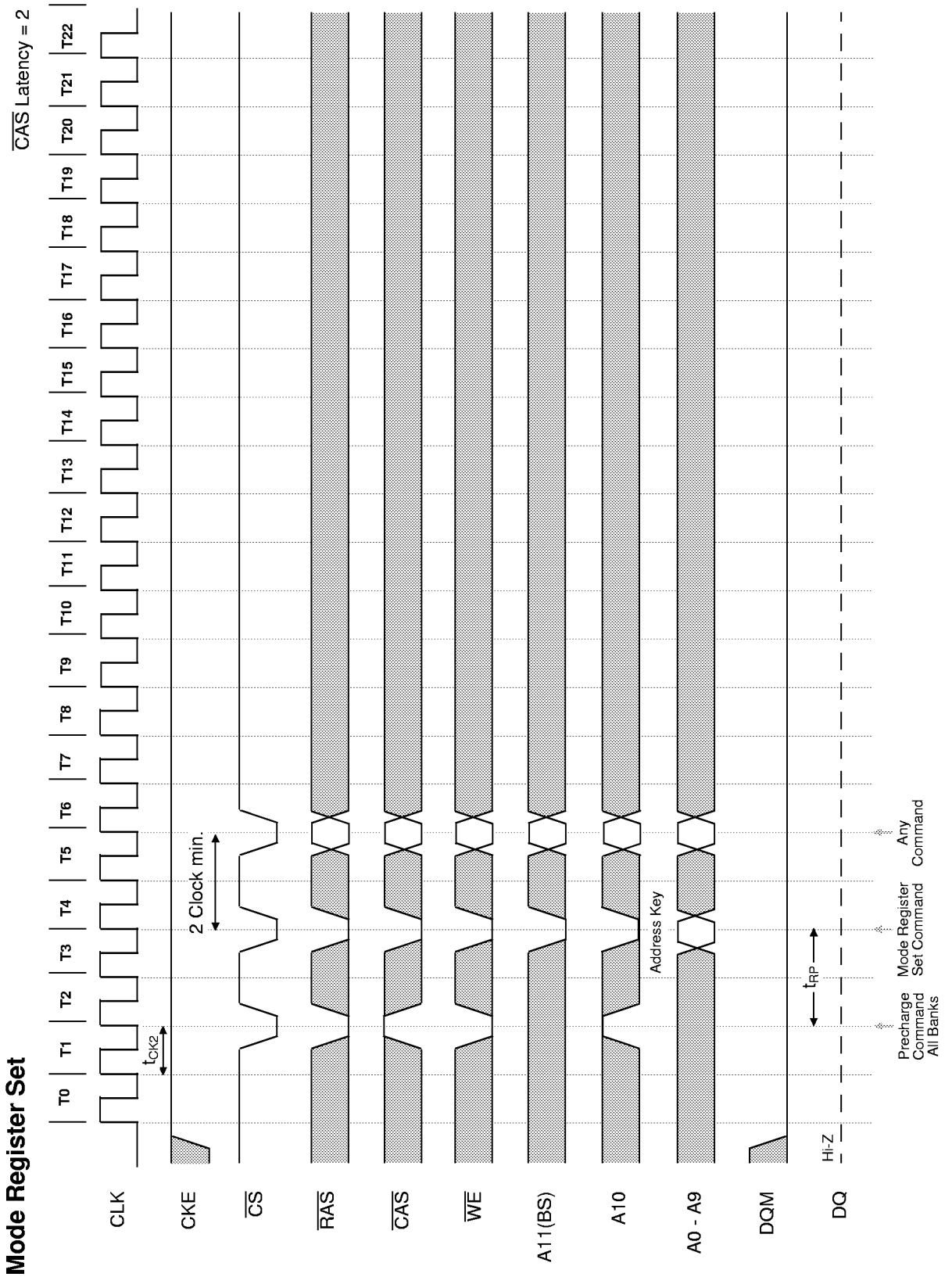
AC Parameters for Write Timing



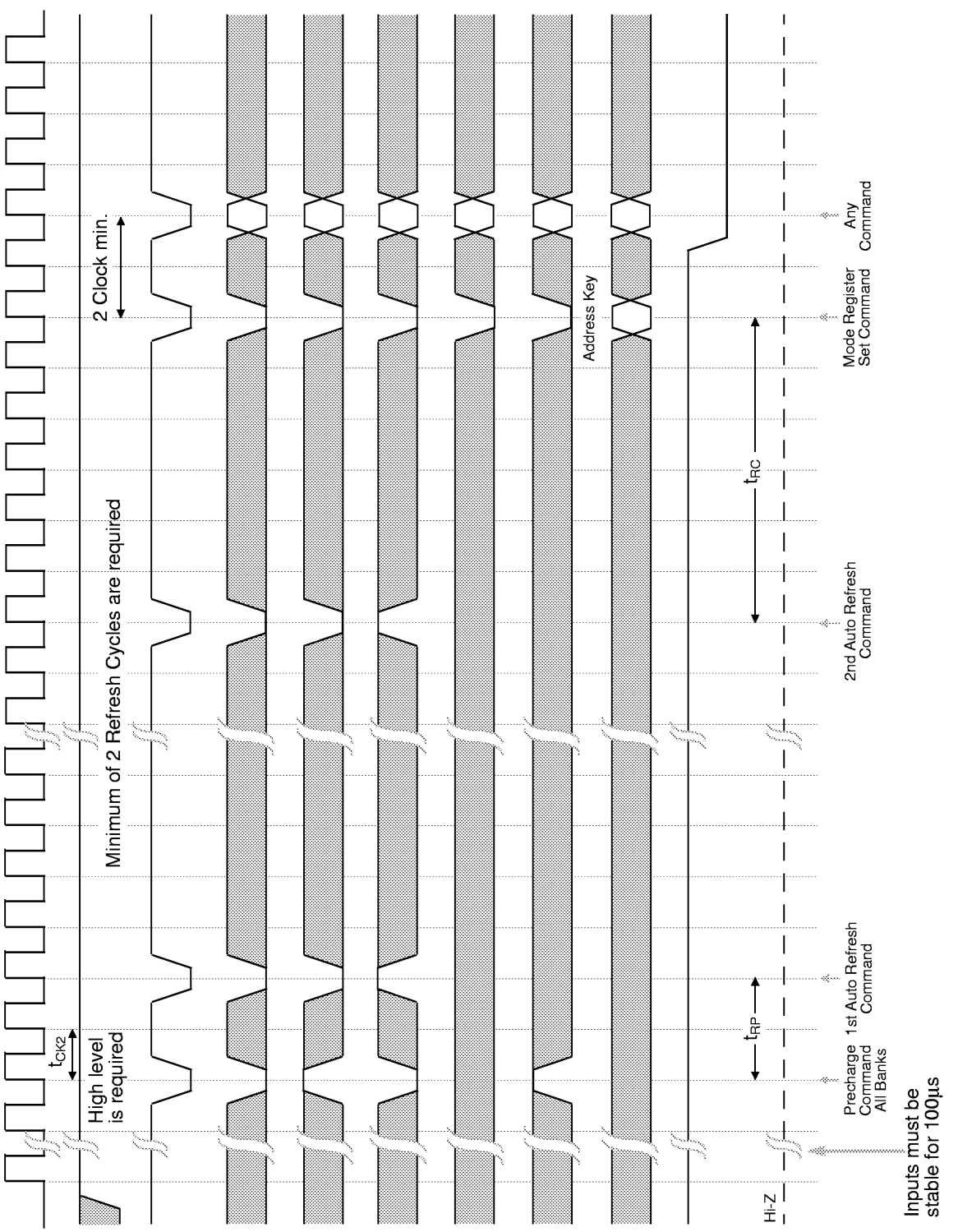
AC Parameters for Read Timing



Mode Register Set

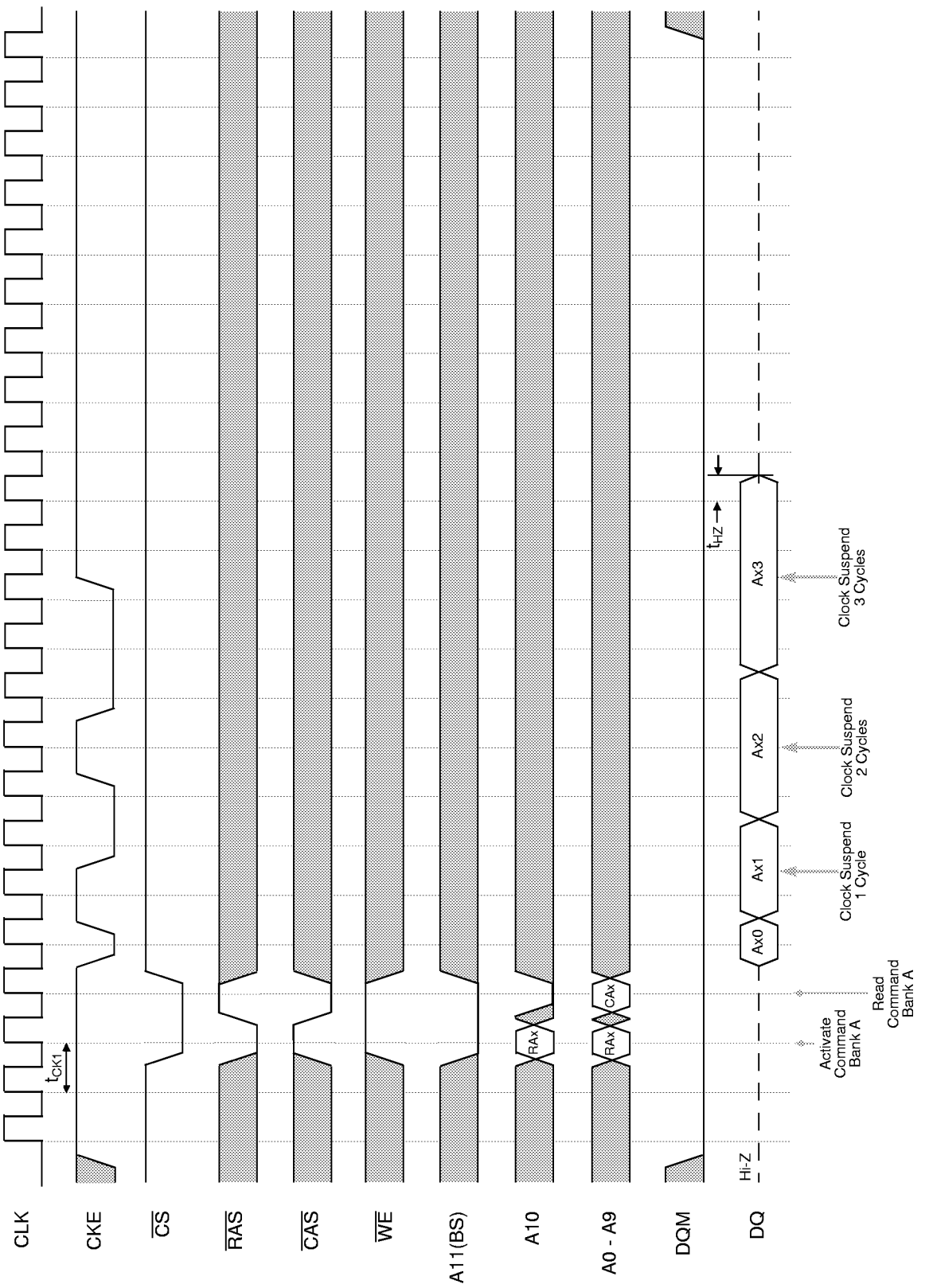


Power on Sequence and Auto Refresh (CBR)



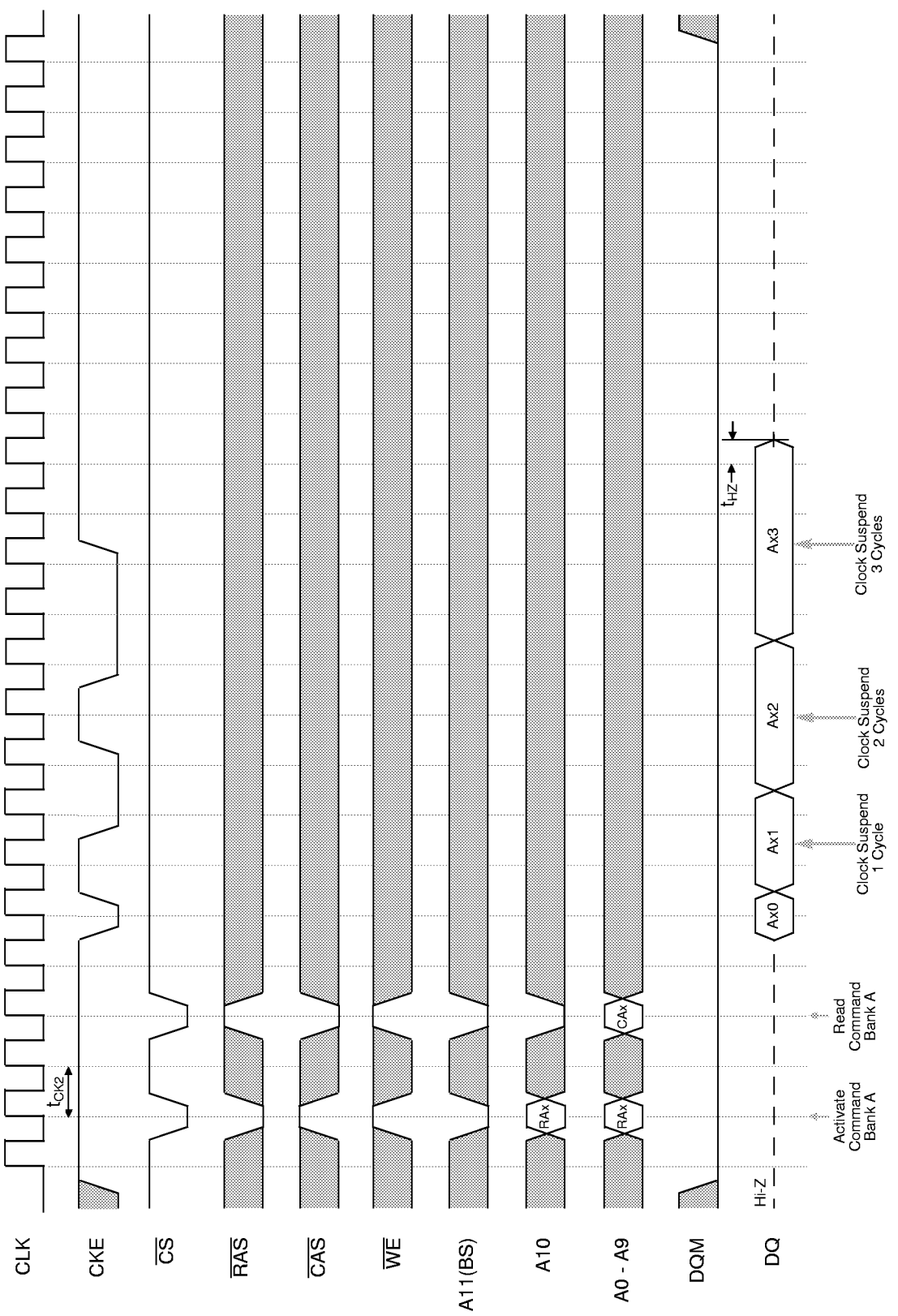
Clock Suspension During Burst Read (Using CKE) (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



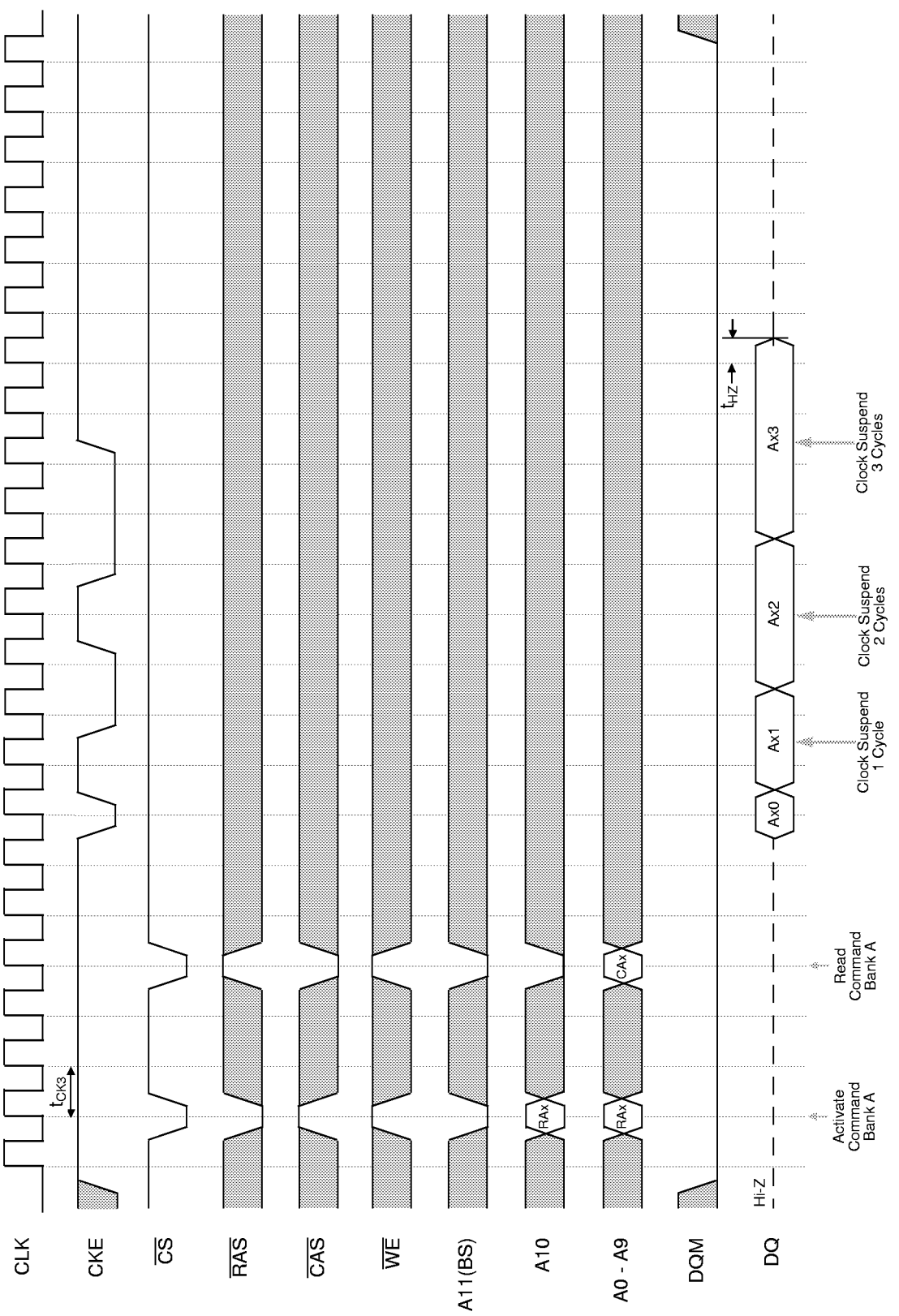
Clock Suspension During Burst Read (Using CKE) (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2



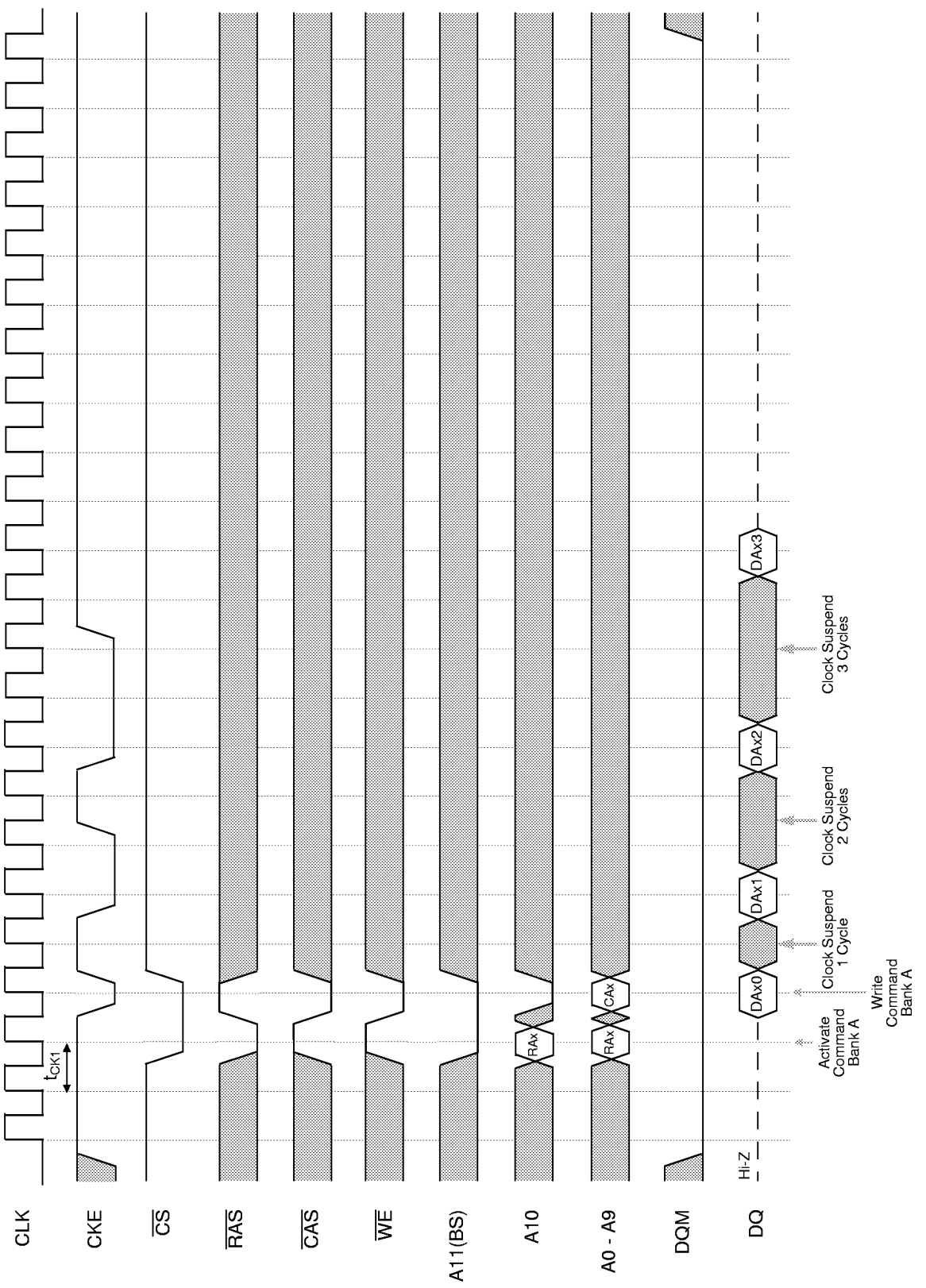
Clock Suspension During Burst Read (Using CKE) (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3



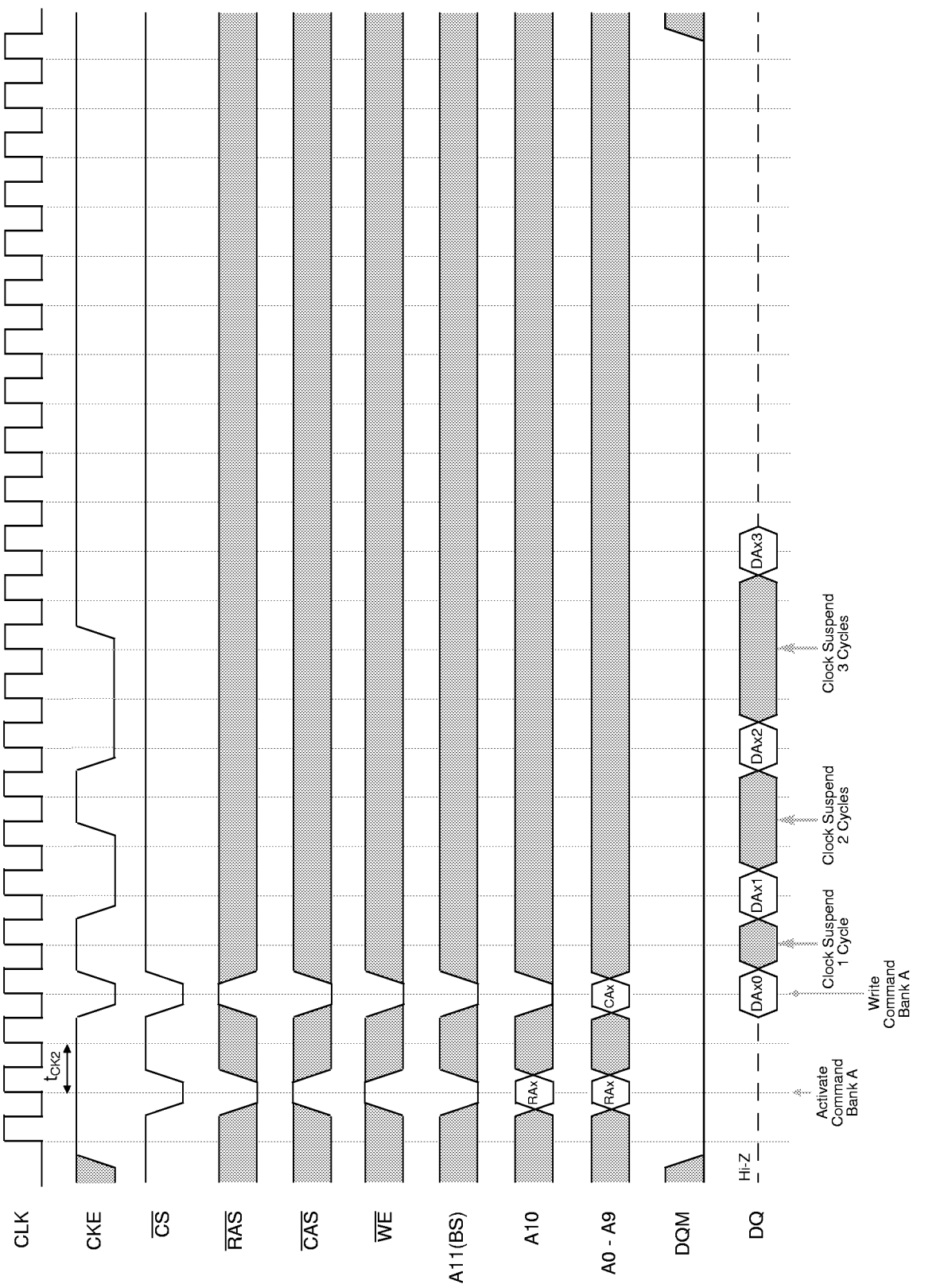
Clock Suspension During Burst Write (Using CKE) (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



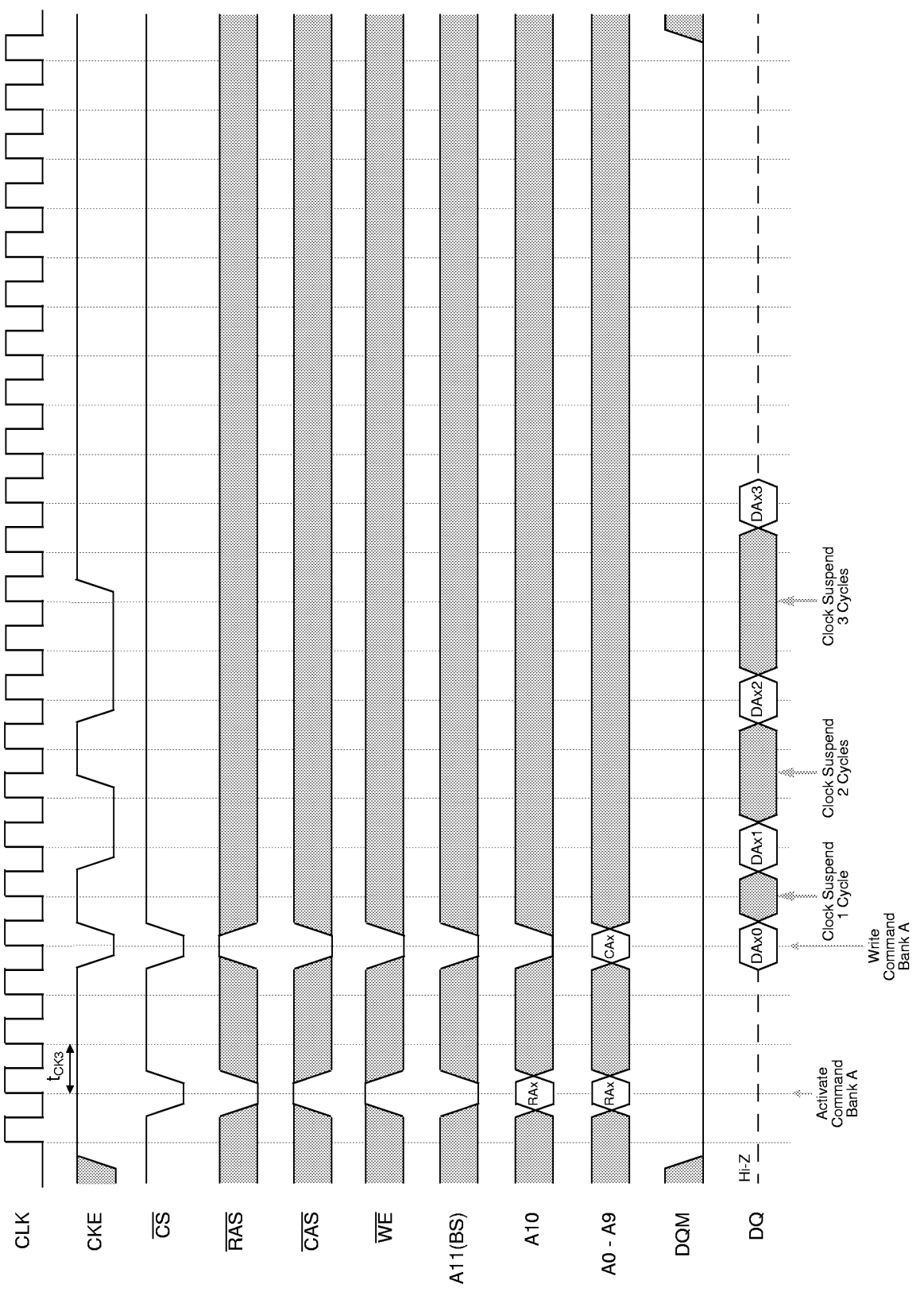
Clock Suspension During Burst Write (Using CKE) (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2

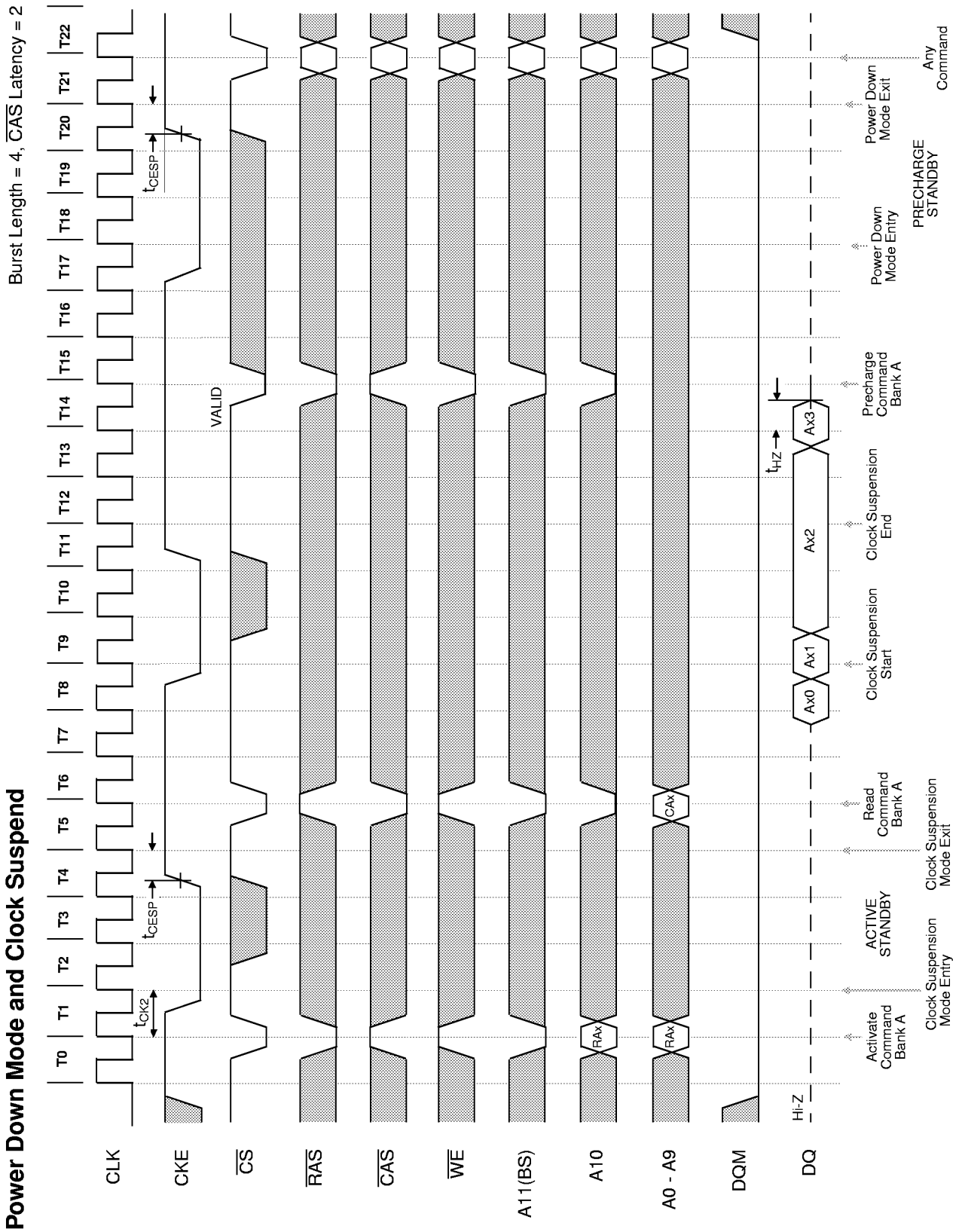


Clock Suspension During Burst Write (Using CKE) (3 of 3)

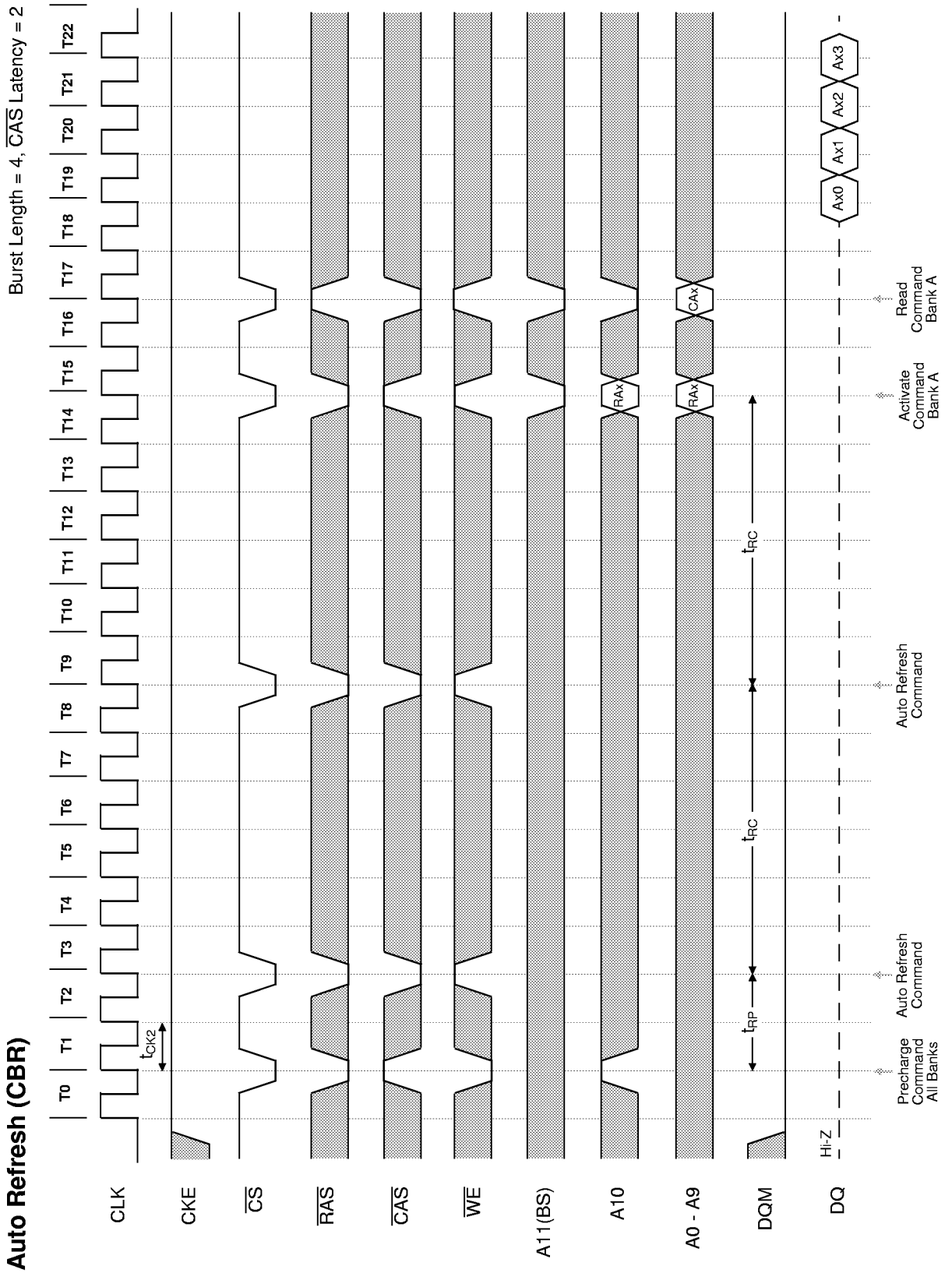
Burst Length = 4, $\overline{CAS}$ Latency = 3



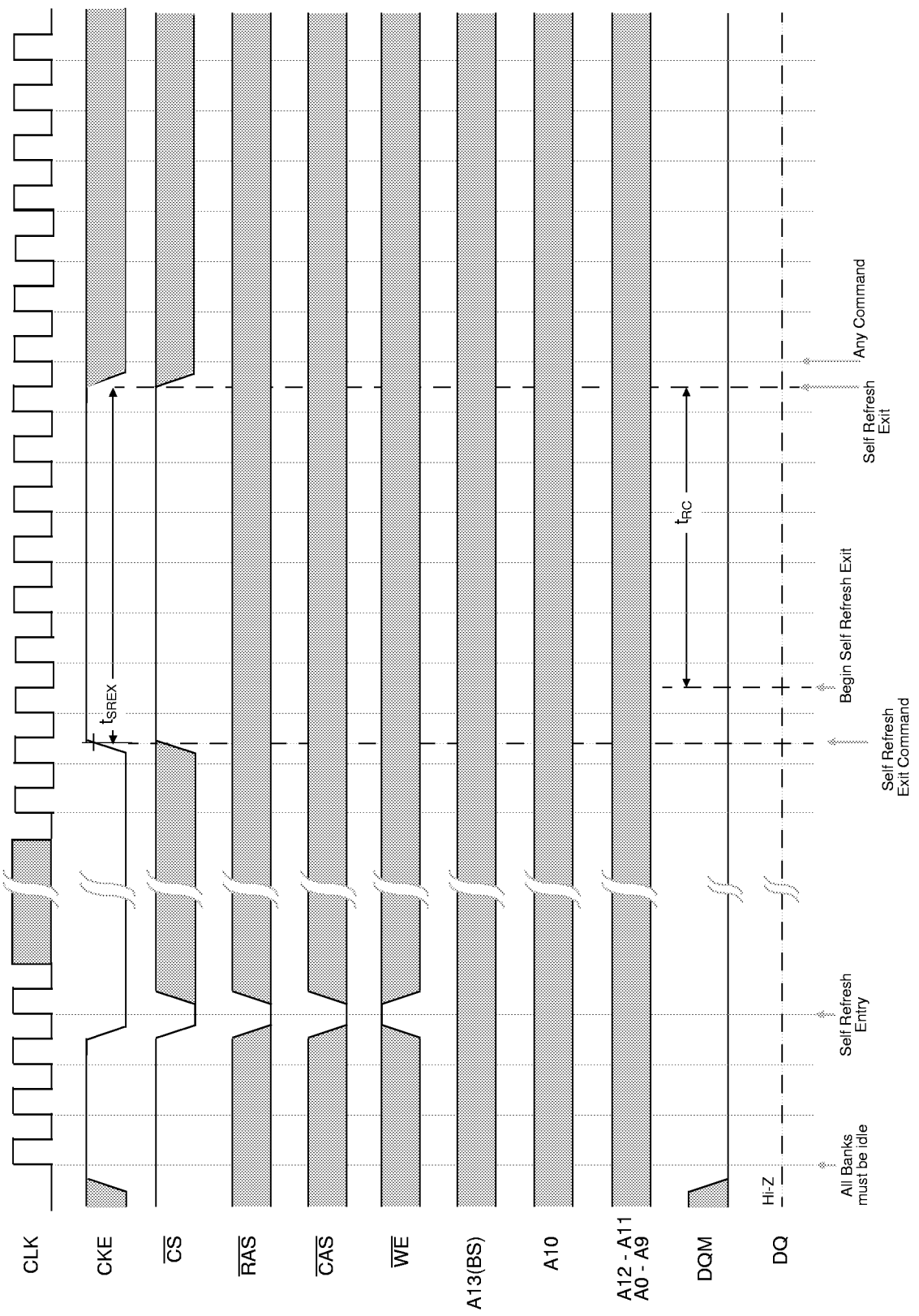
Power Down Mode and Clock Suspend



Auto Refresh (CBR)

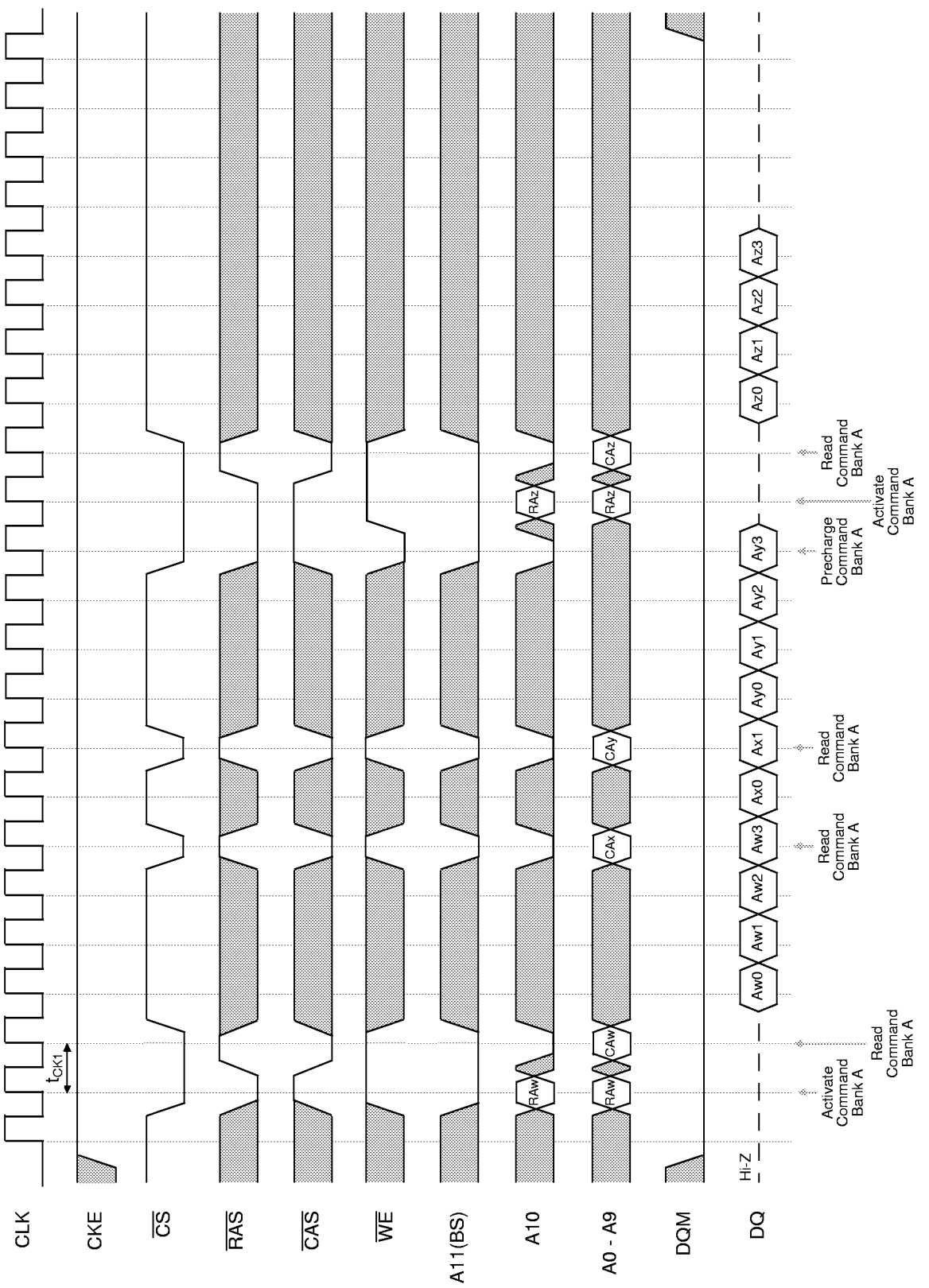


Self Refresh (Entry and Exit) ***Note: The CLK signal must be reestablished prior to CKE returning high.



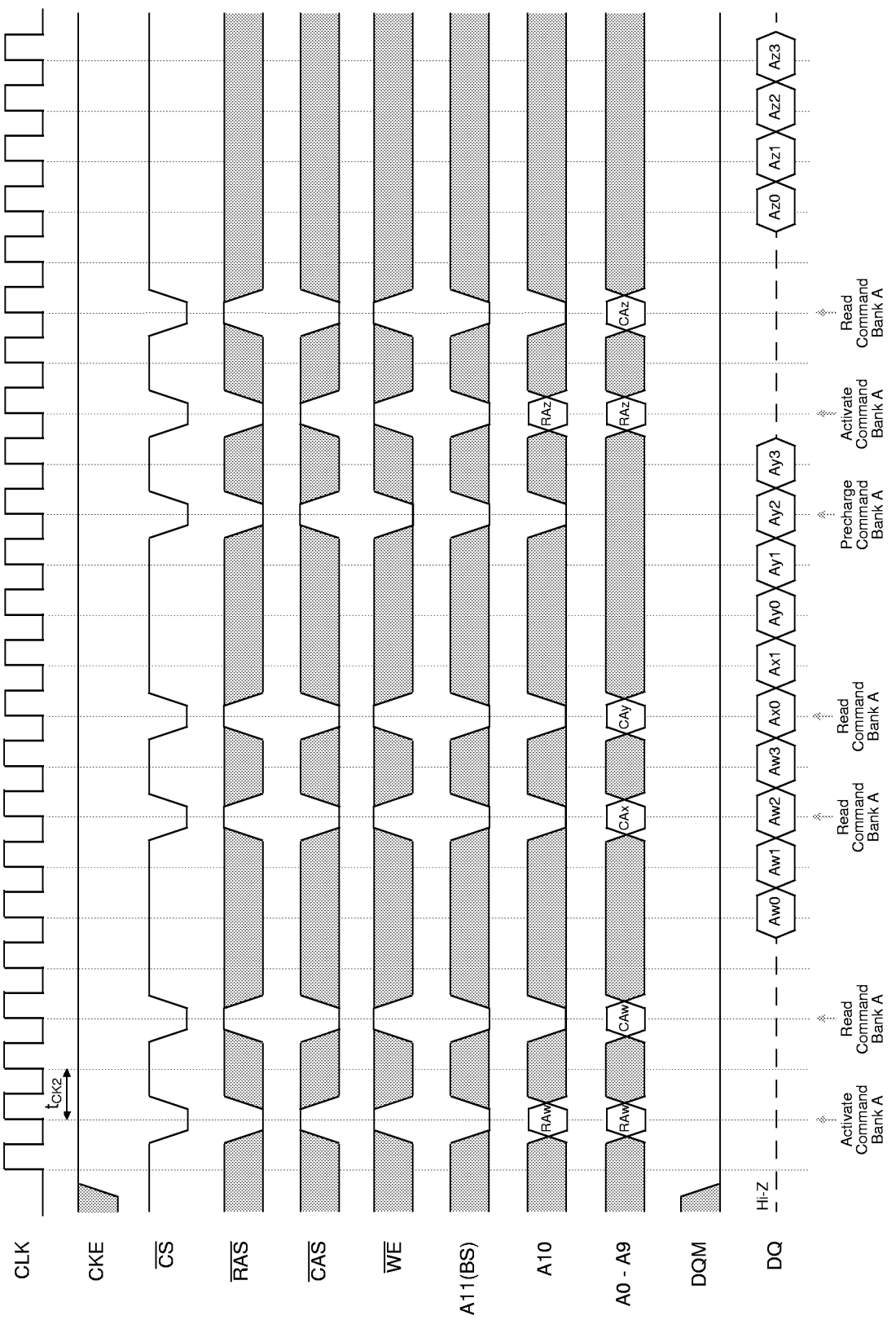
Random Column Read (Page within same Bank) (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



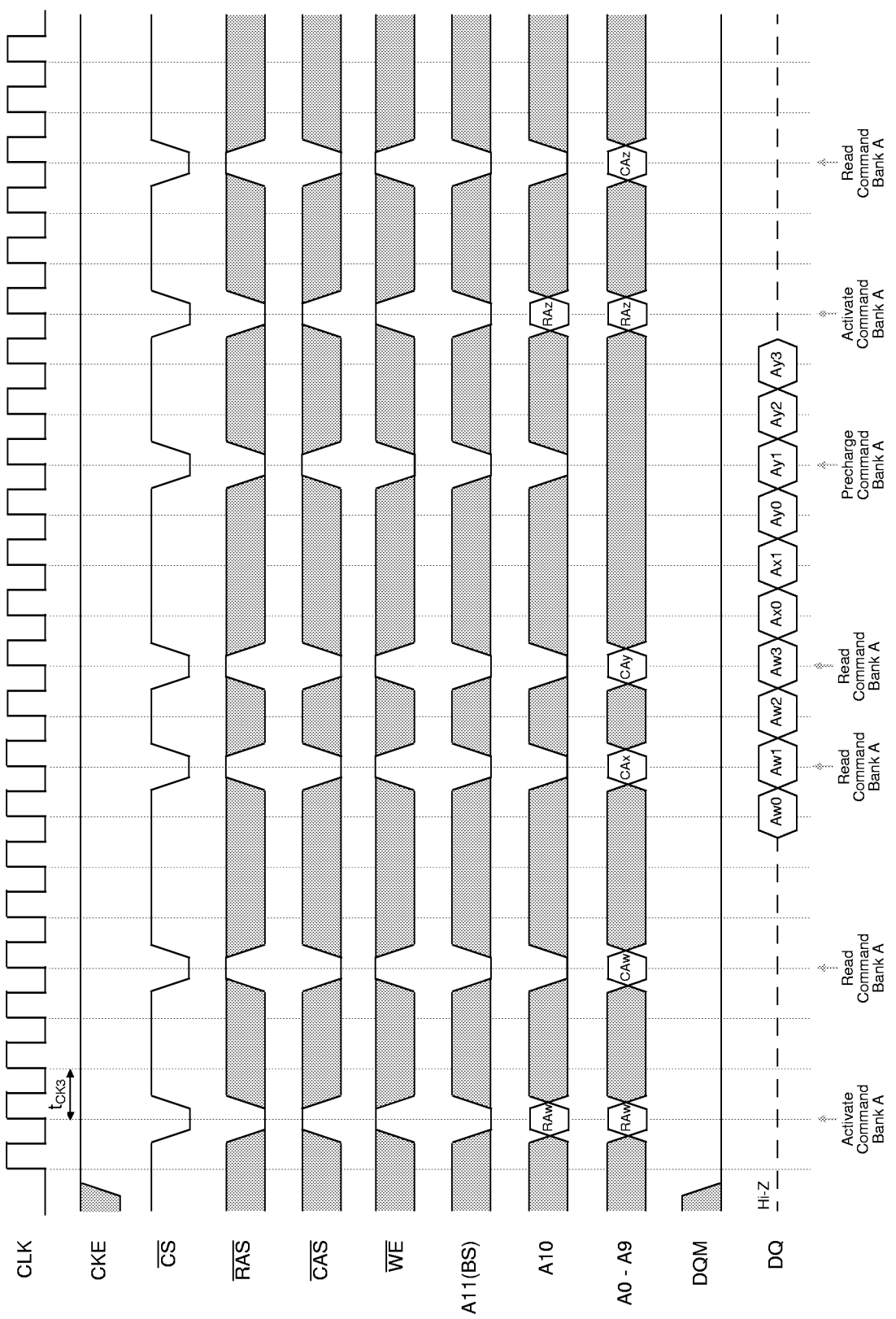
Random Column Read (Page within same Bank) (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2



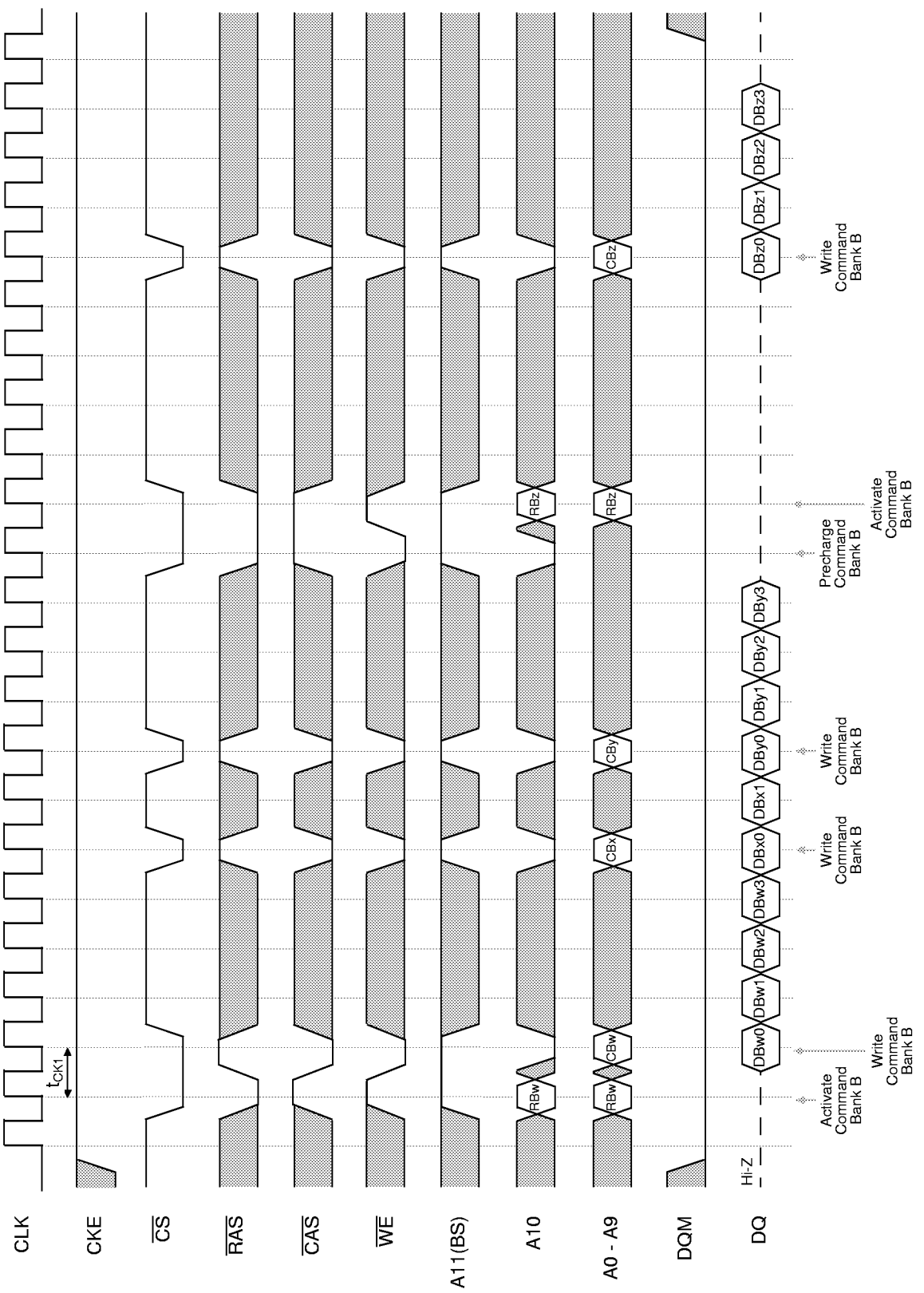
Random Column Read (Page within same Bank) (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3



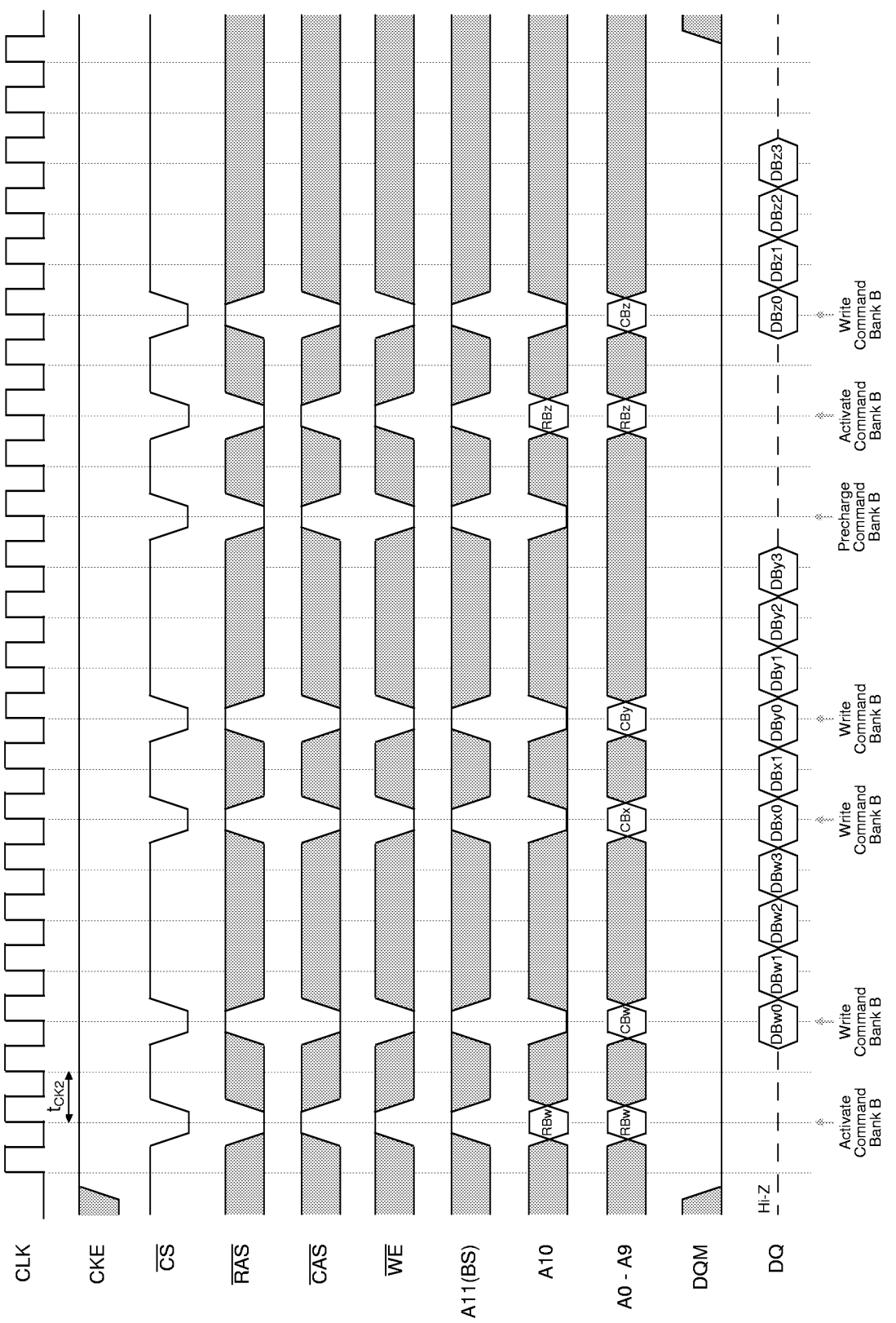
Random Column Write (Page within same Bank) (1 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 1



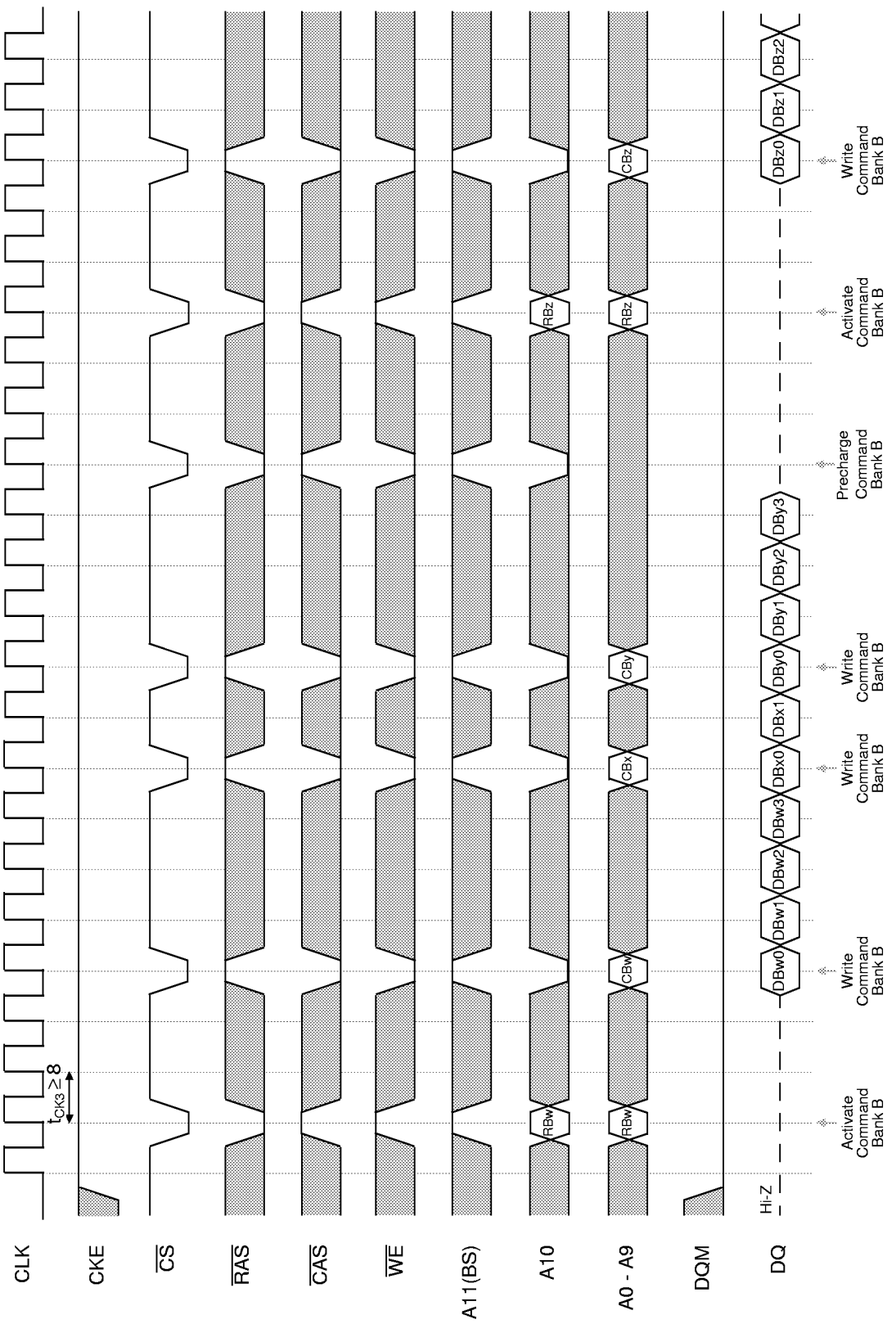
Random Column Write (Page within same Bank) (2 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 2



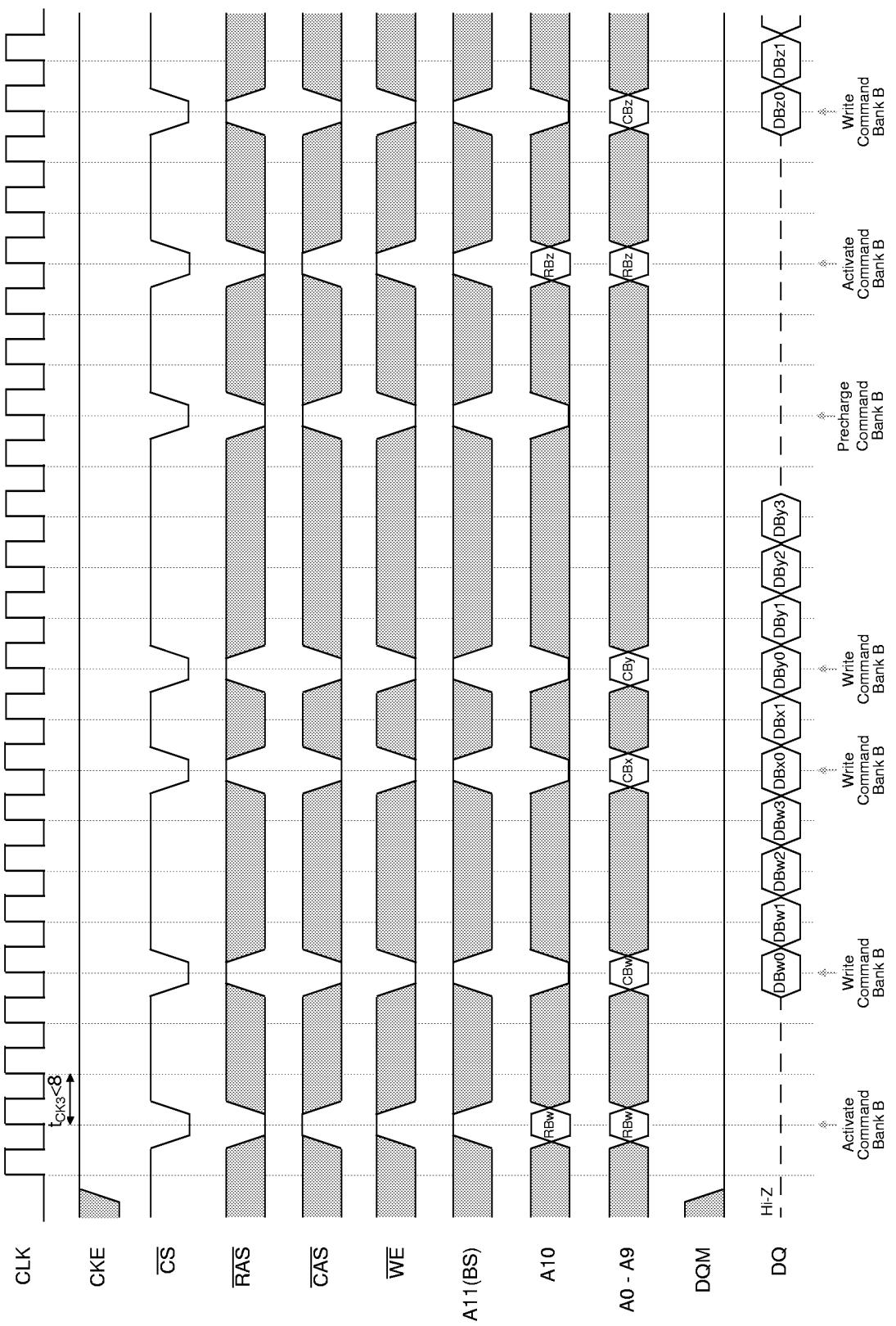
Random Column Write (Page within same Bank) (3 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 3, $t_{CK3} \geq 8$

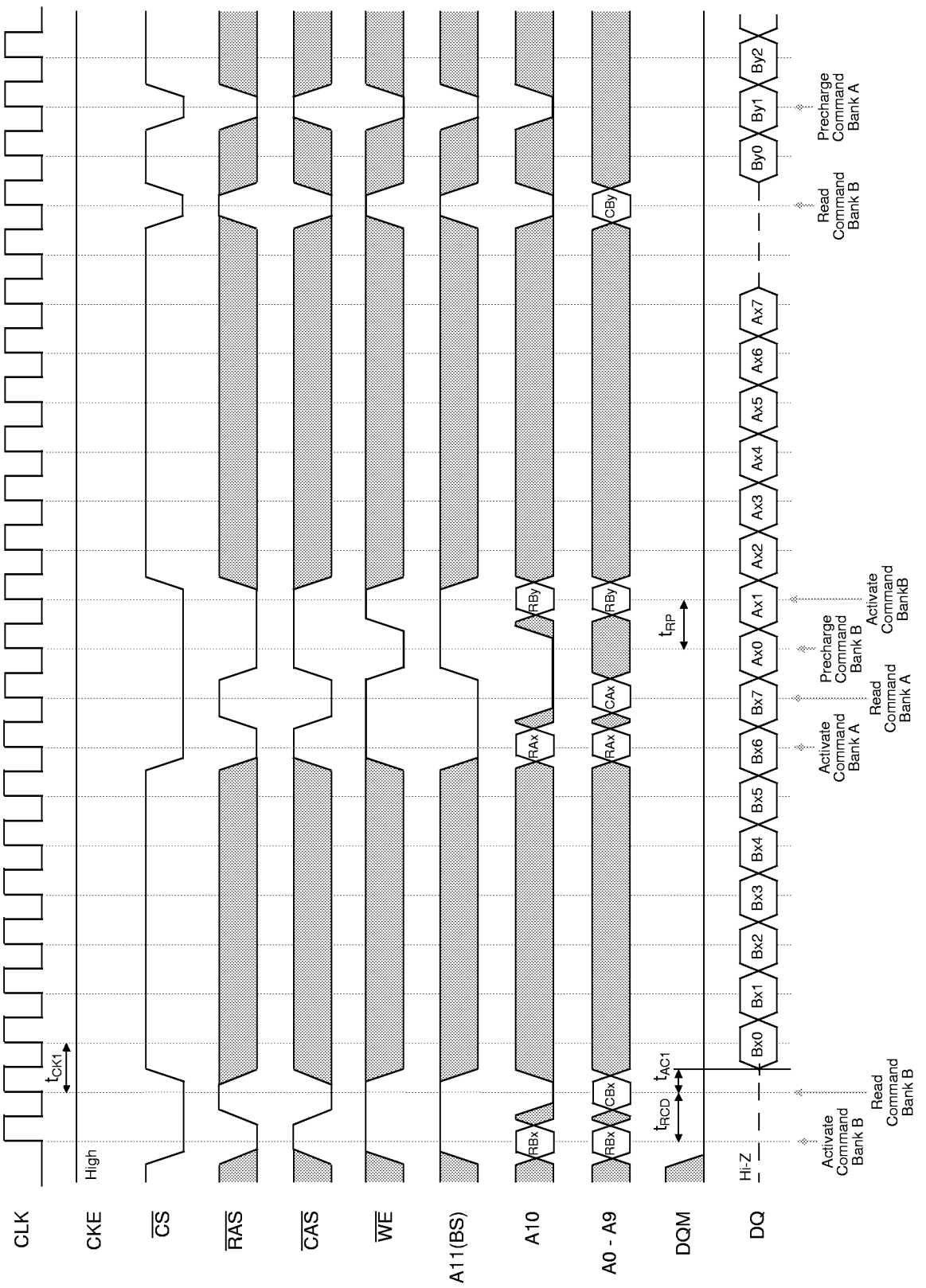


Random Column Write (Page within same Bank) (4 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 3, $t_{CK3} < 8$

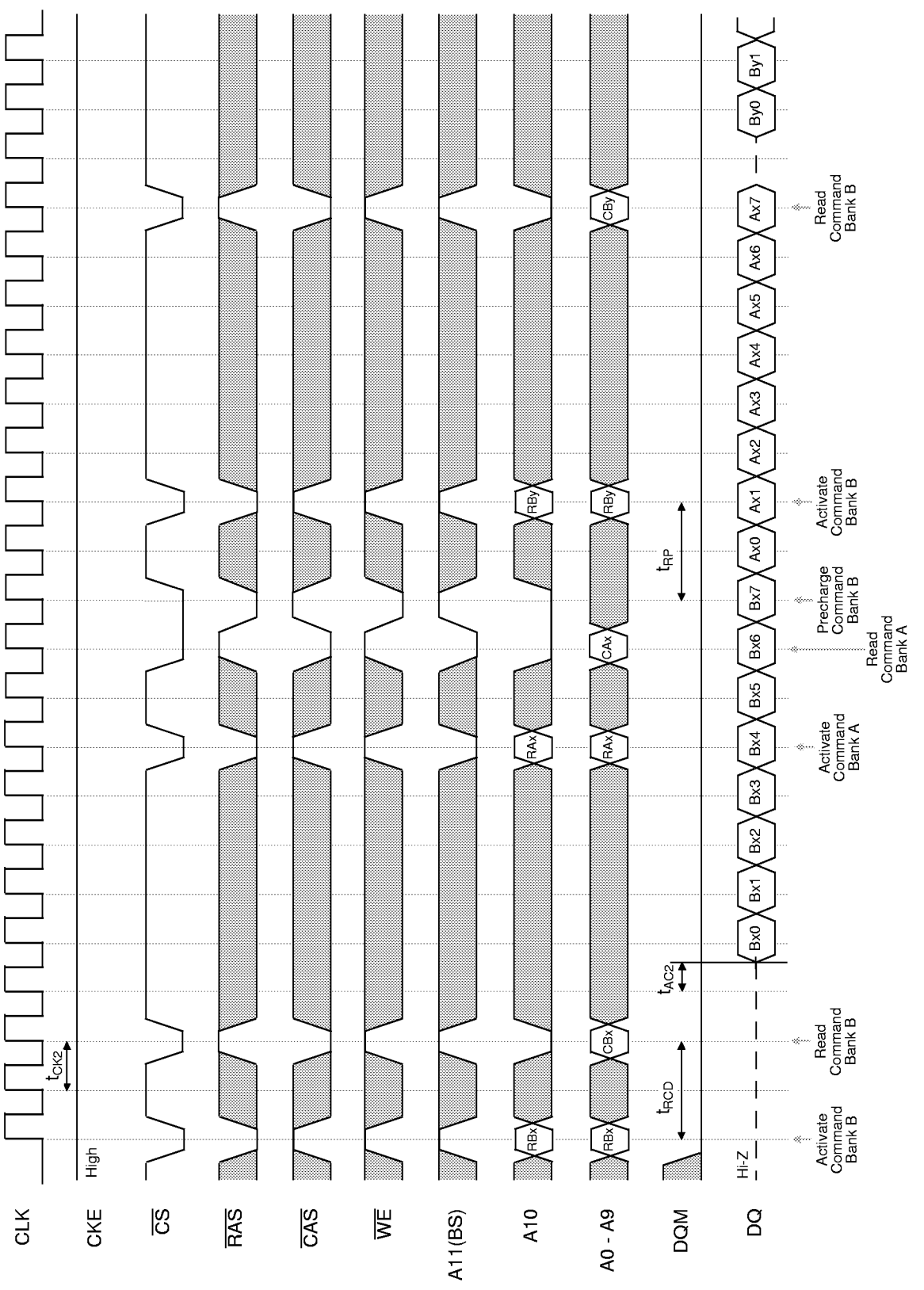


Random Row Read (Interleaving Banks) (1 of 3)



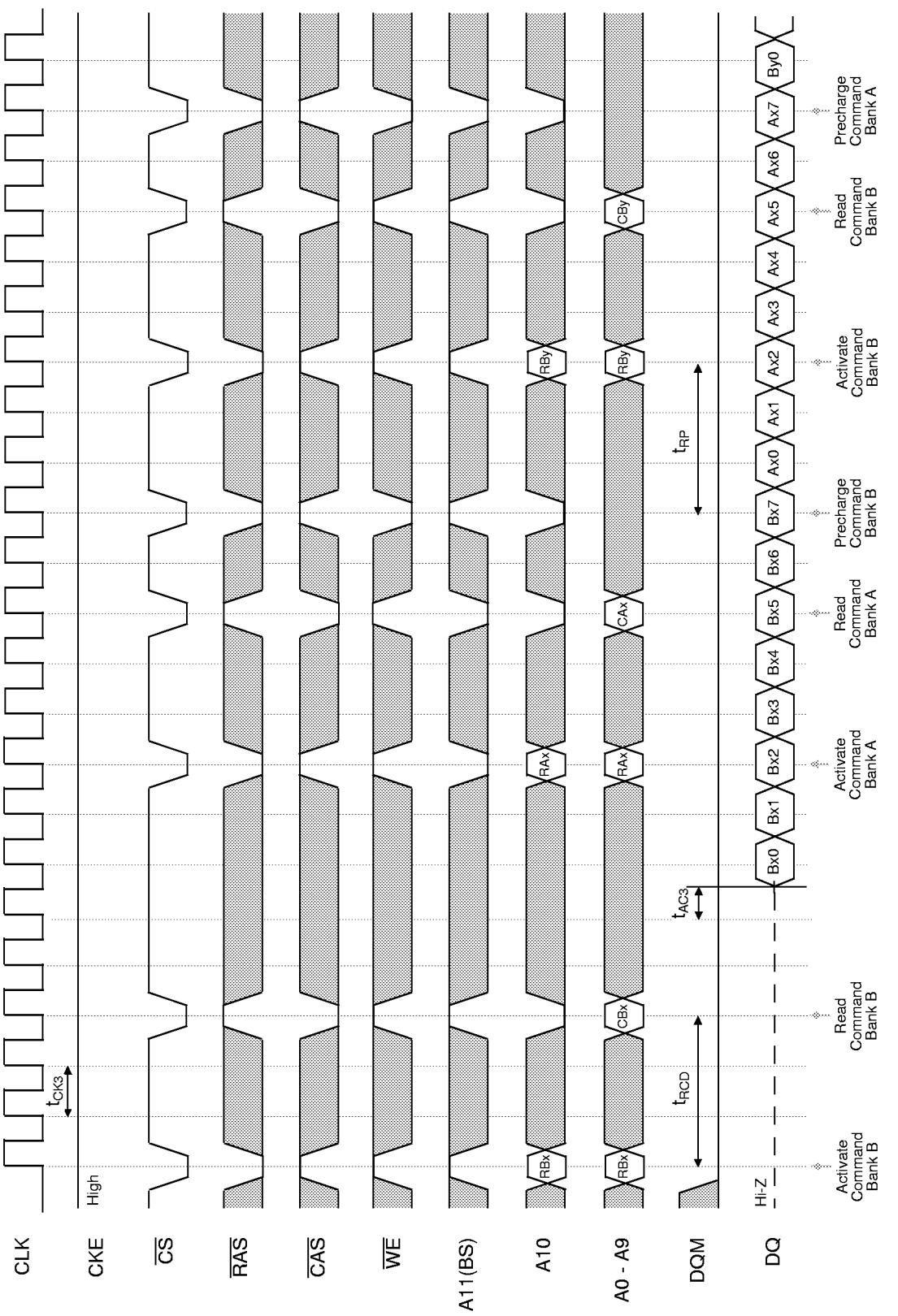
Random Row Read (Interleaving Banks) (2 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 2



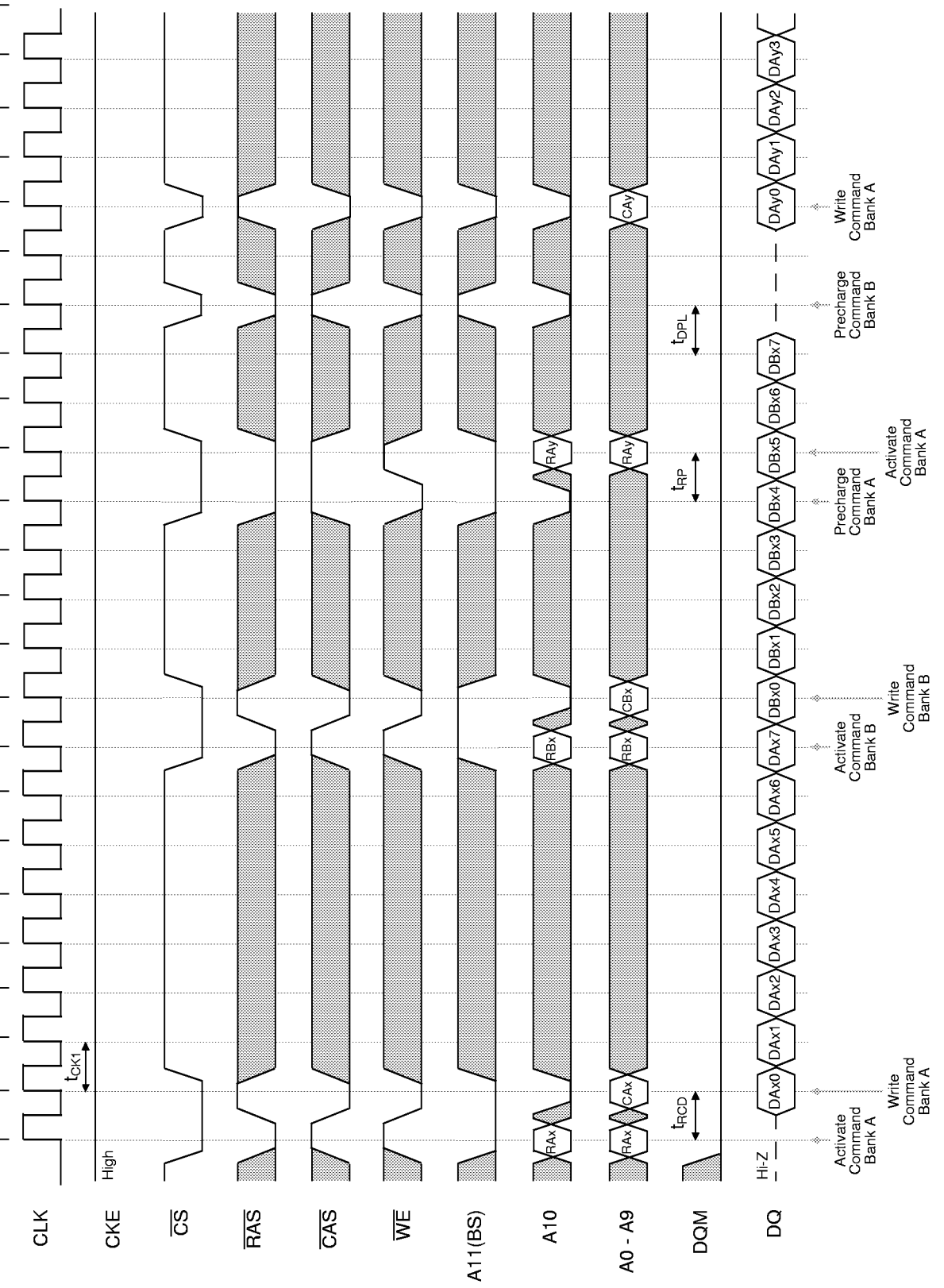
Random Row Read (Interleaving Banks) (3 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 3



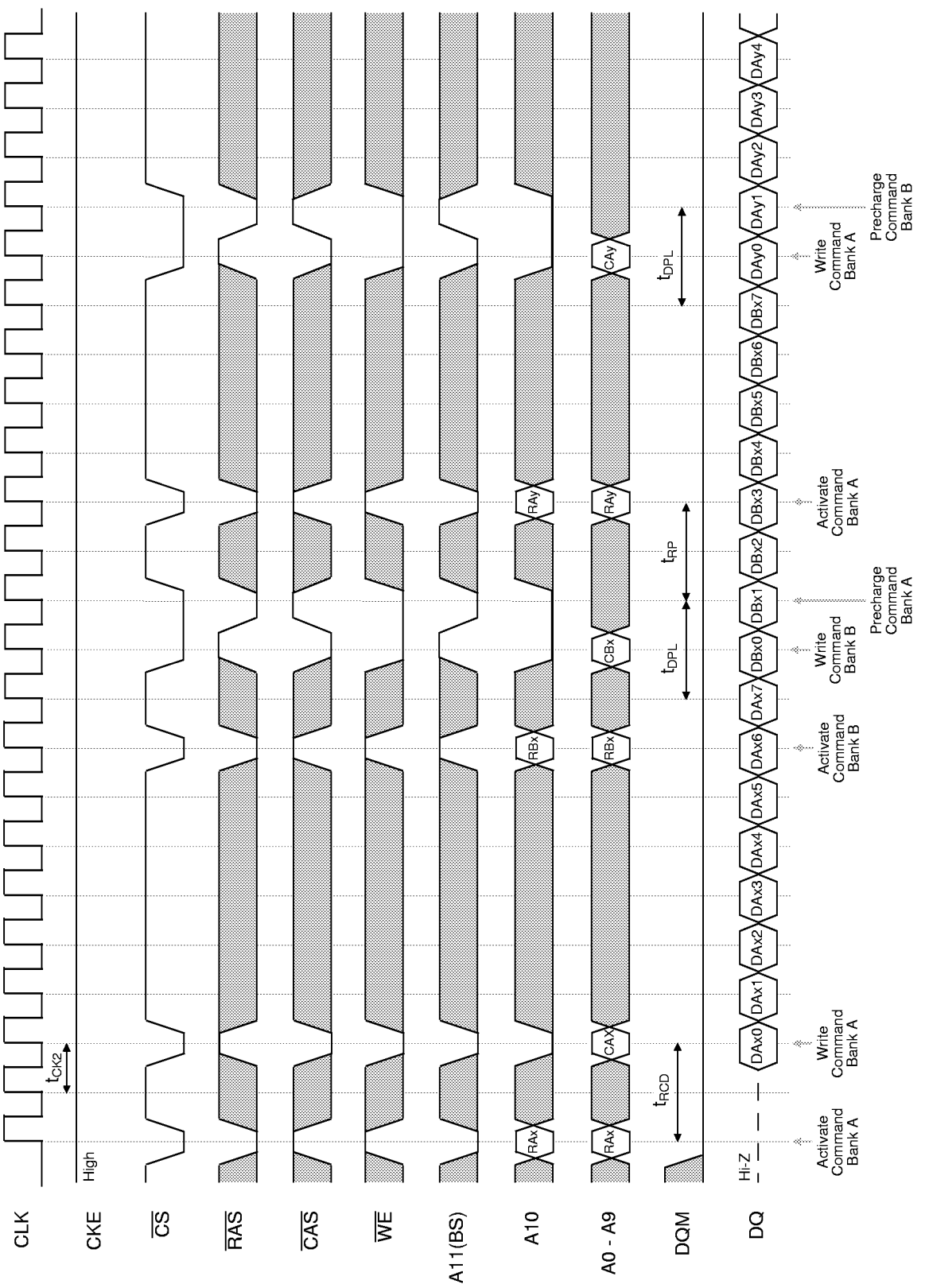
Random Row Write (Interleaving Banks) (1 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 1



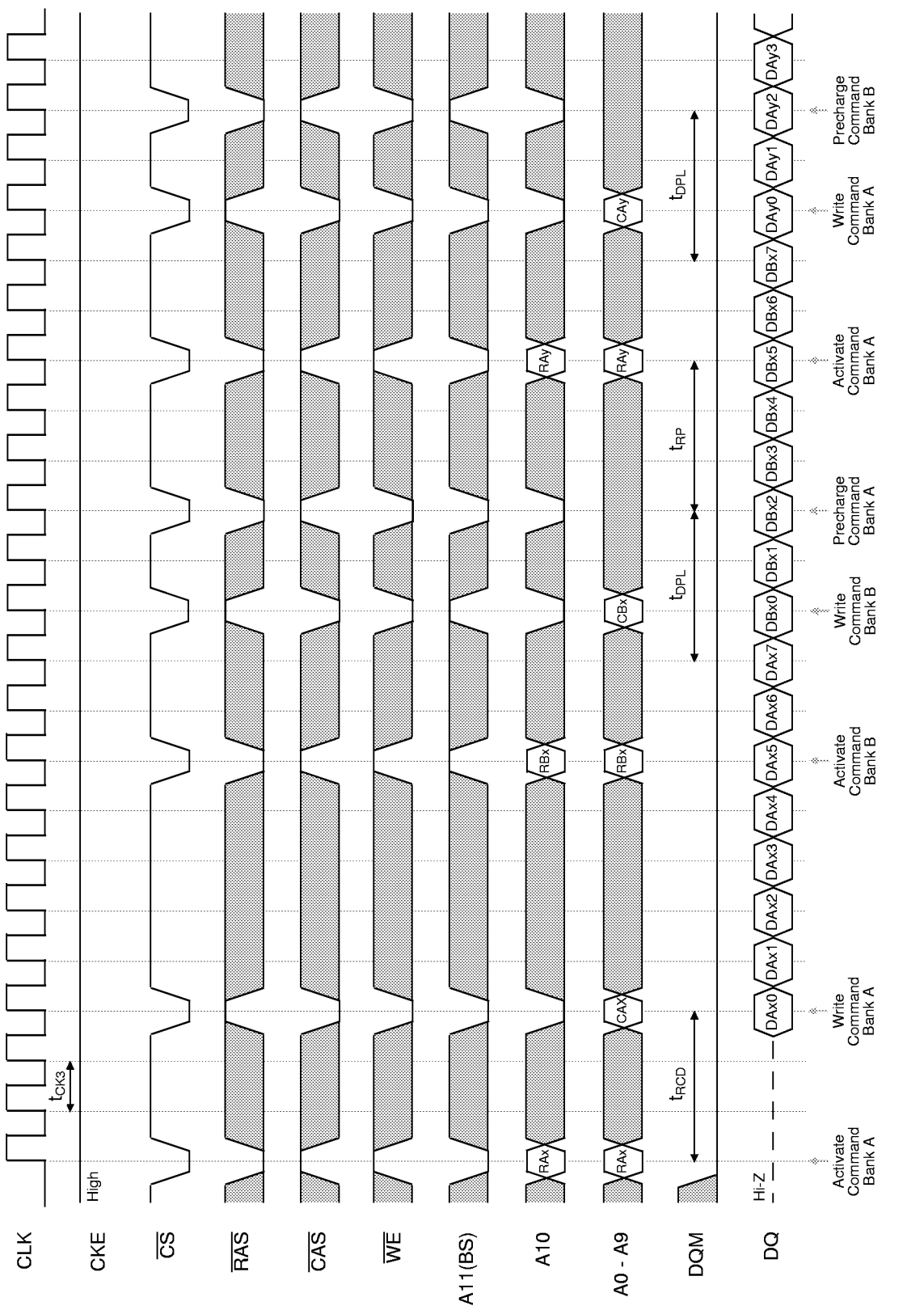
Random Row Write (Interleaving Banks) (2 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 2



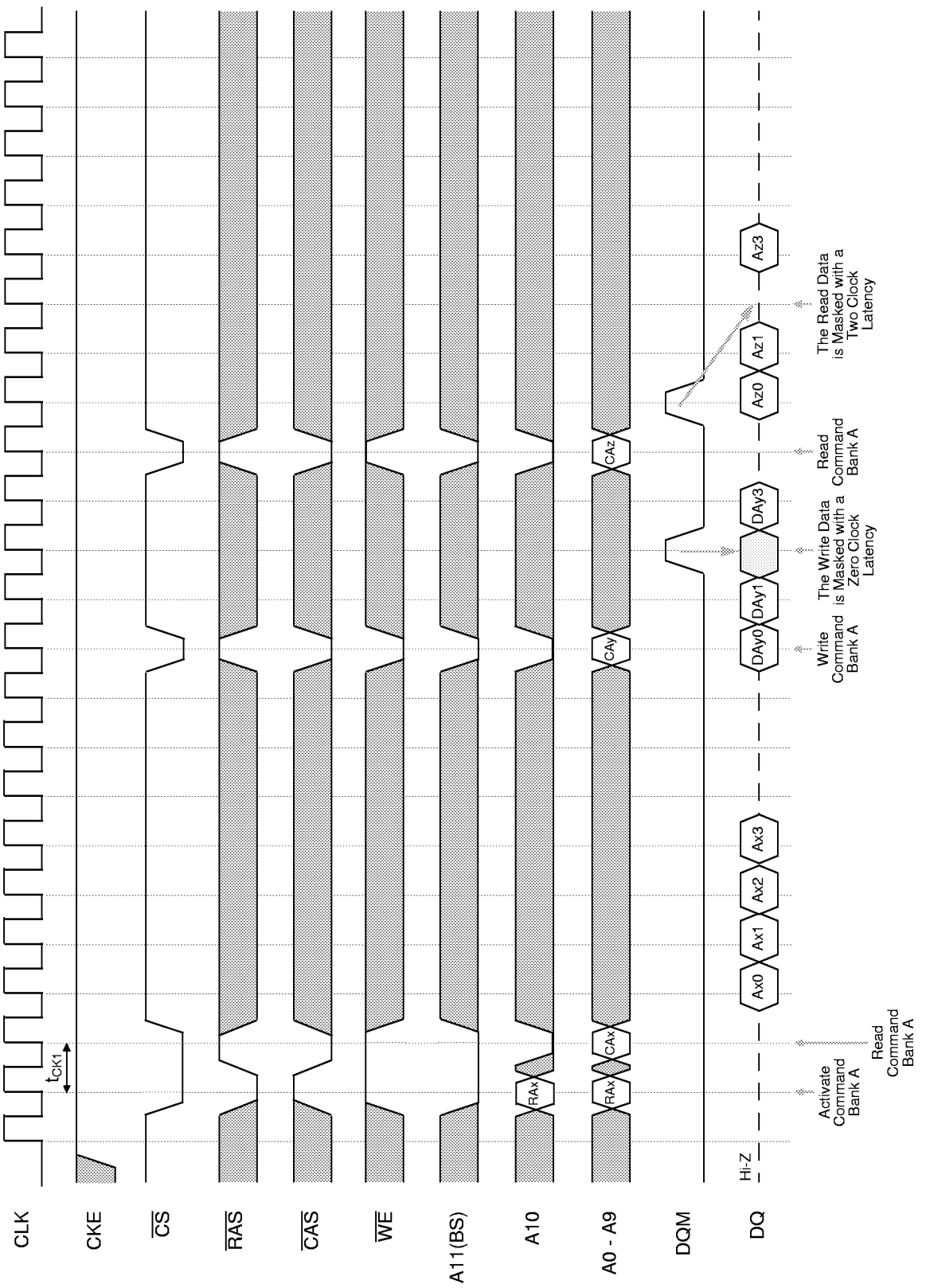
Random Row Write (Interleaving Banks) (3 of 3)

Burst Length = 8, $\overline{CAS}$ Latency = 3



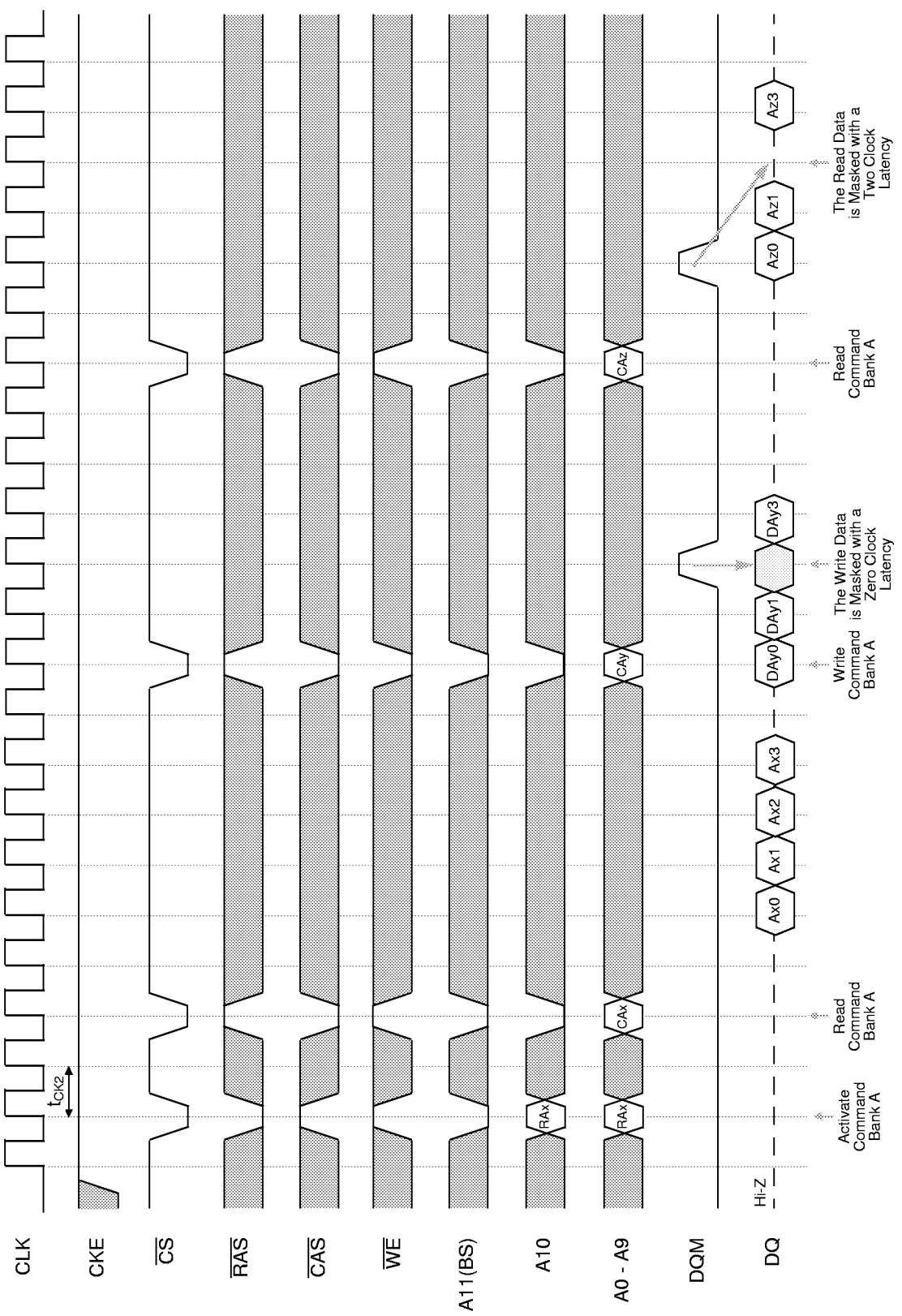
Read and Write Cycle (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



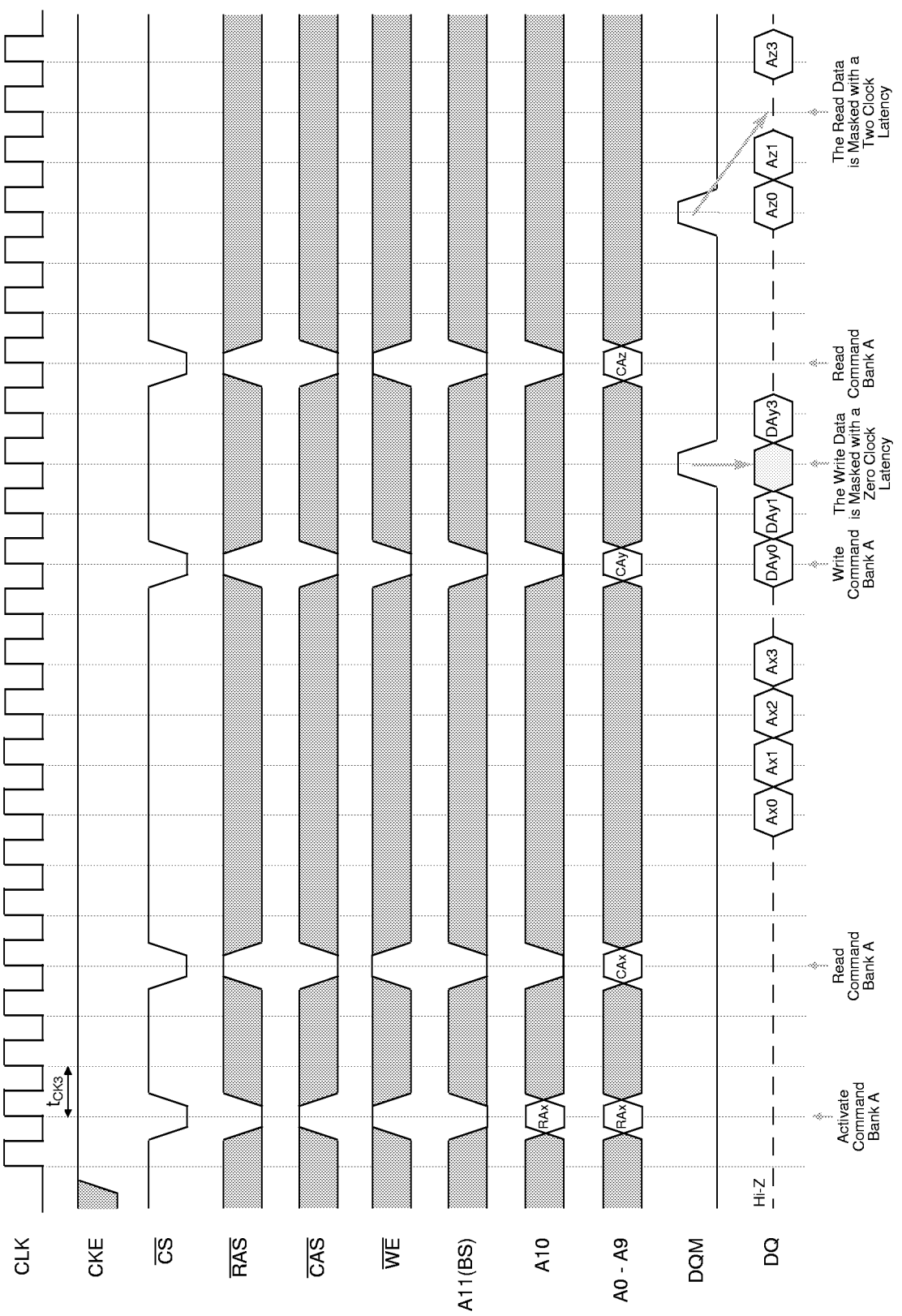
Read and Write Cycle (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2



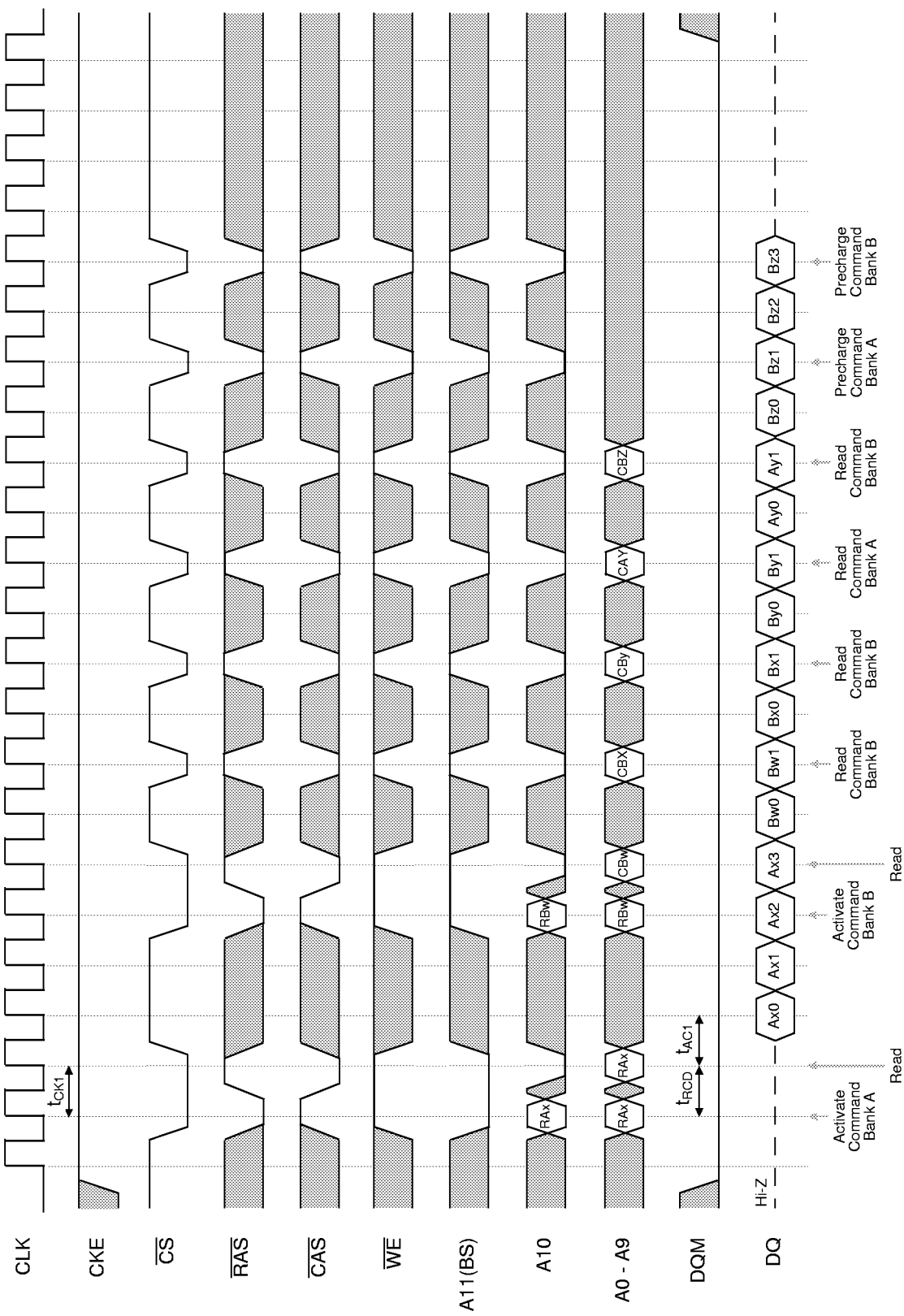
Read and Write Cycle (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3

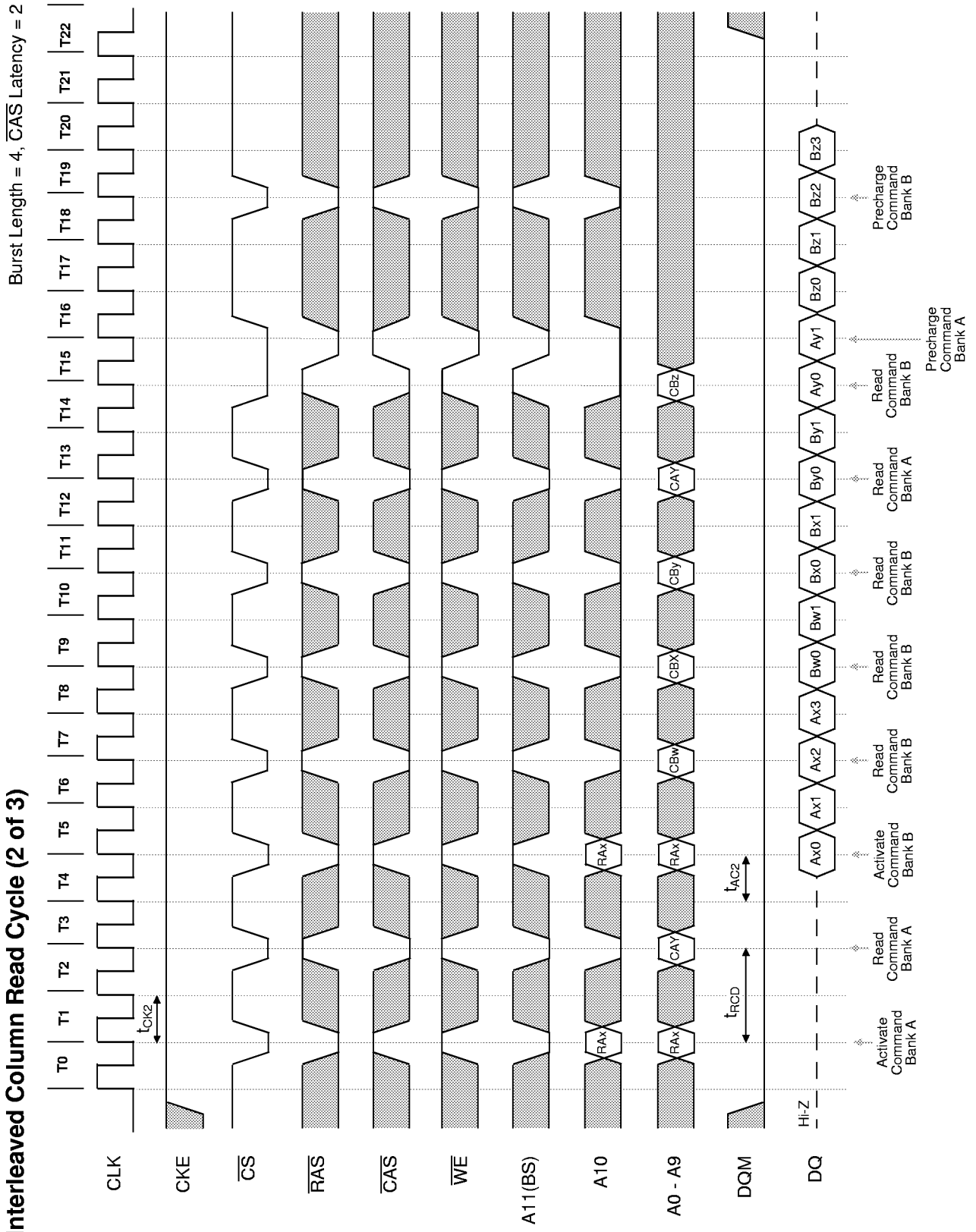


Interleaved Column Read Cycle (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1

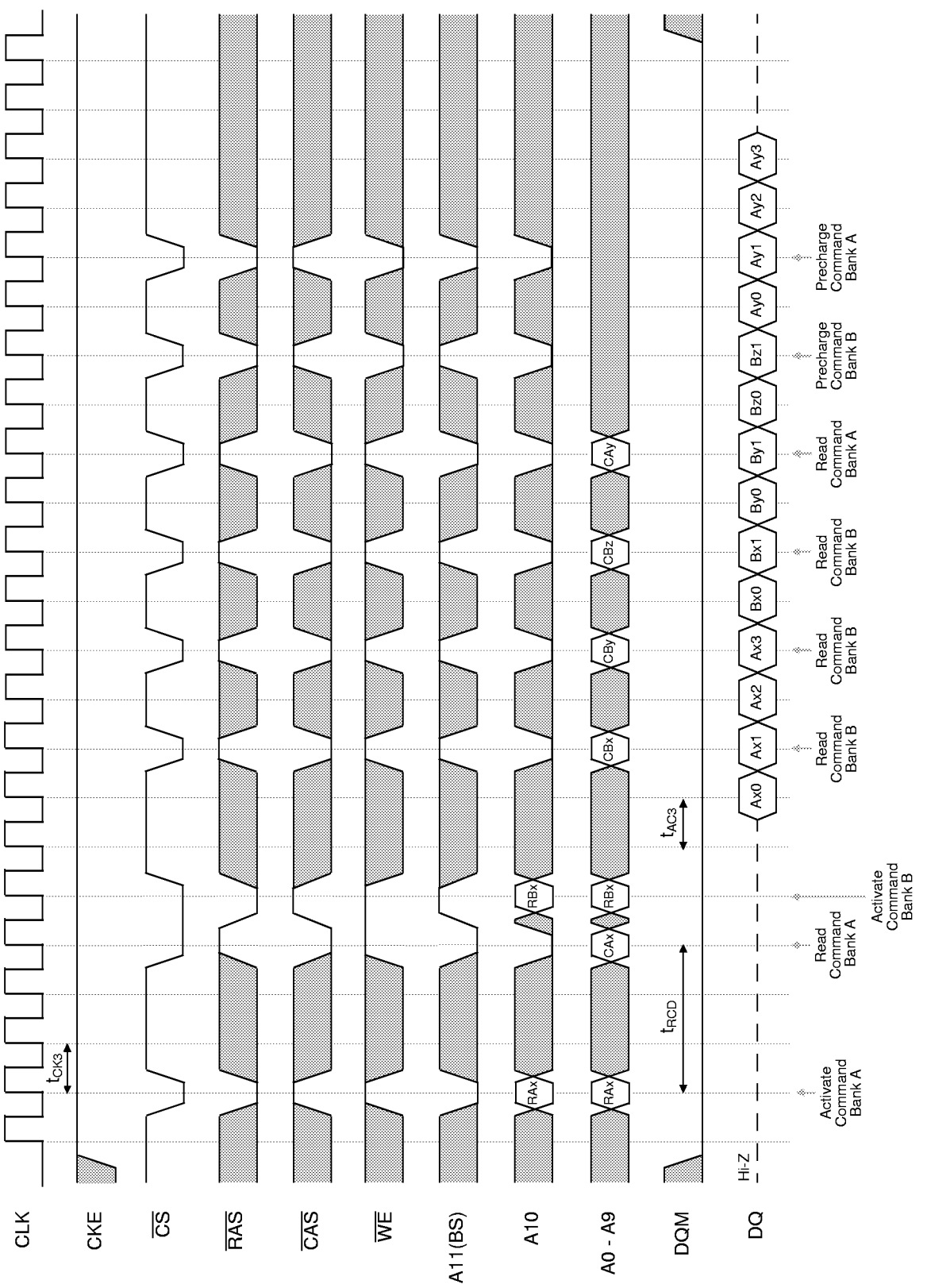


Interleaved Column Read Cycle (2 of 3)

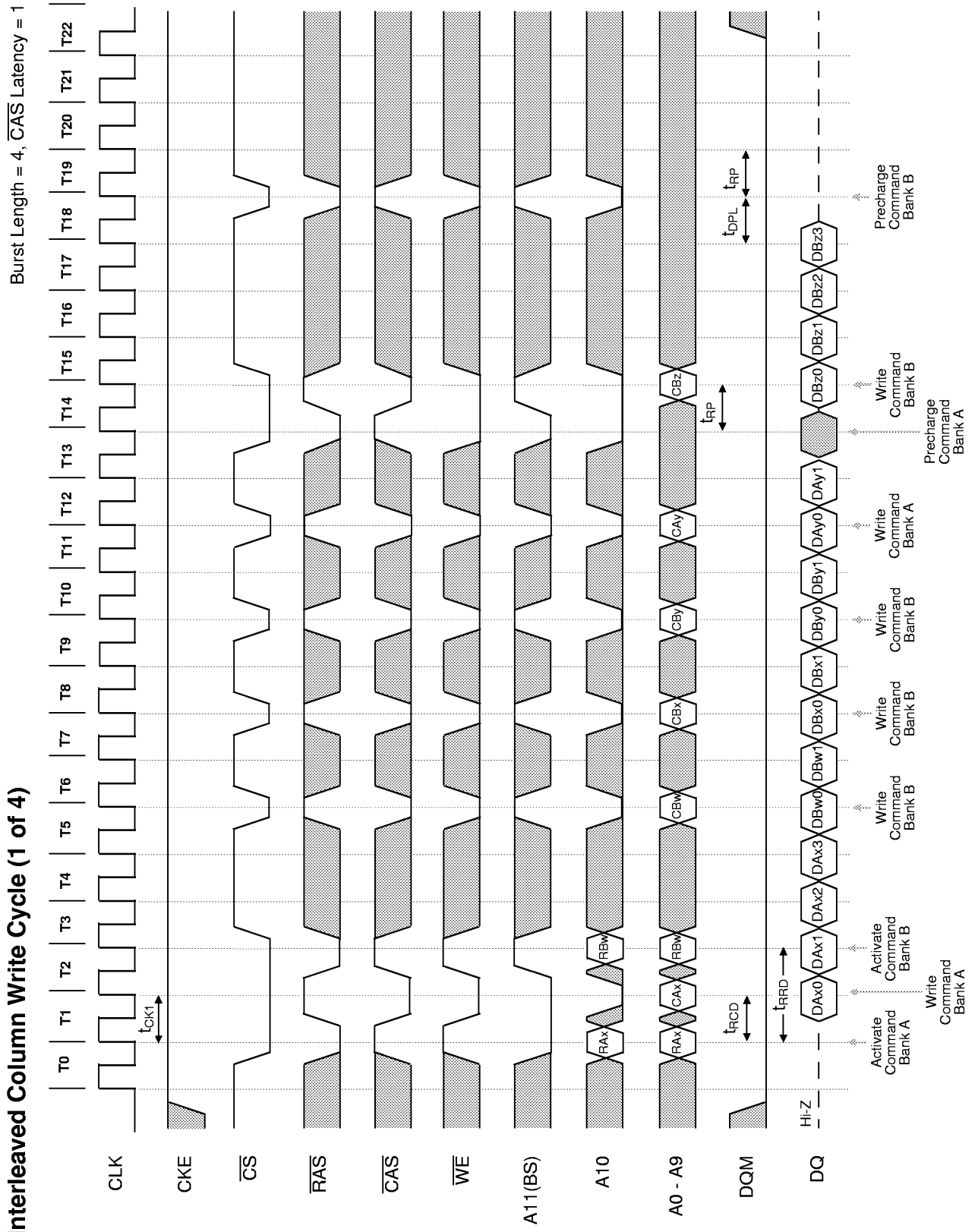


Interleaved Column Read Cycle (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3

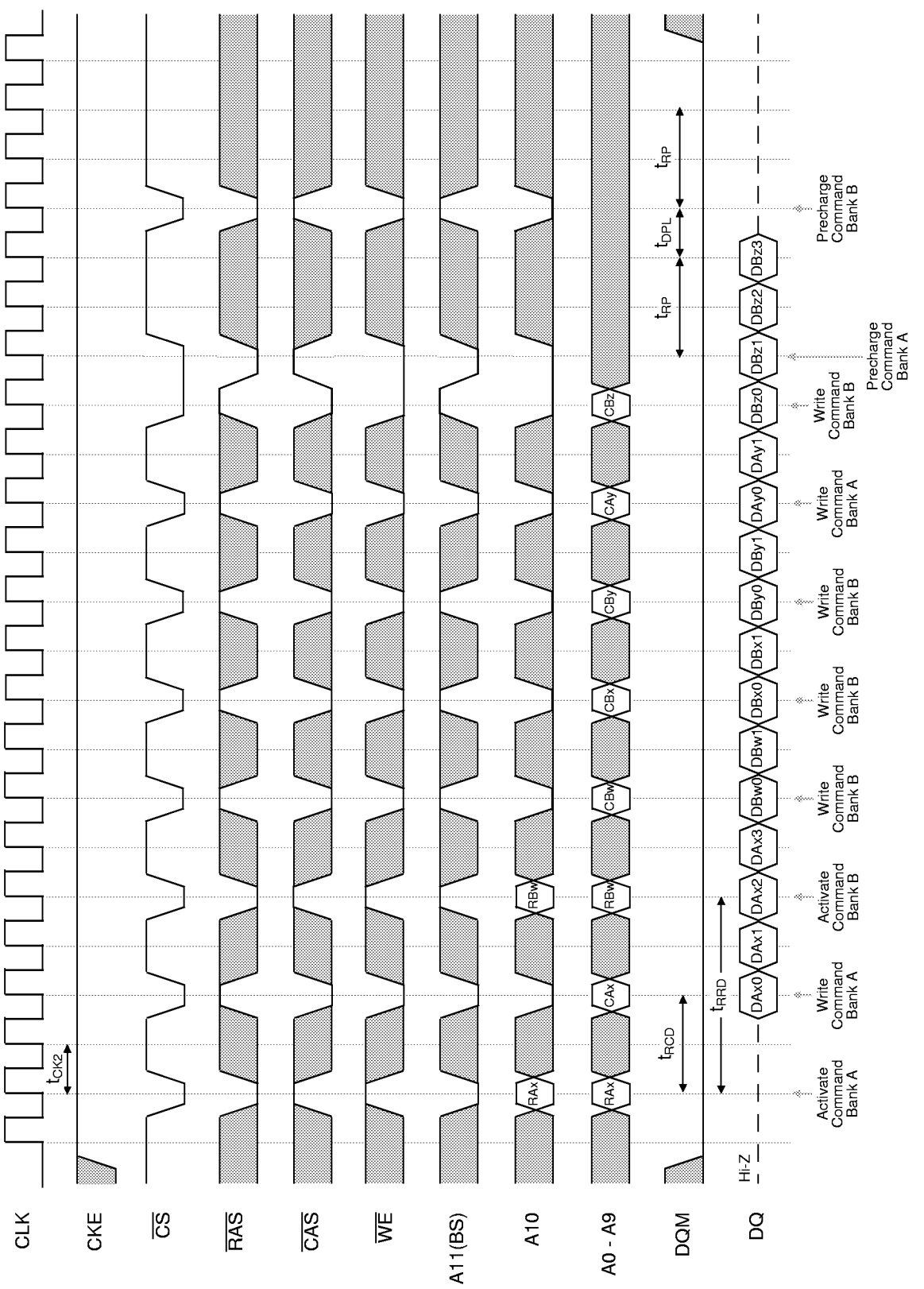


Interleaved Column Write Cycle (1 of 4)



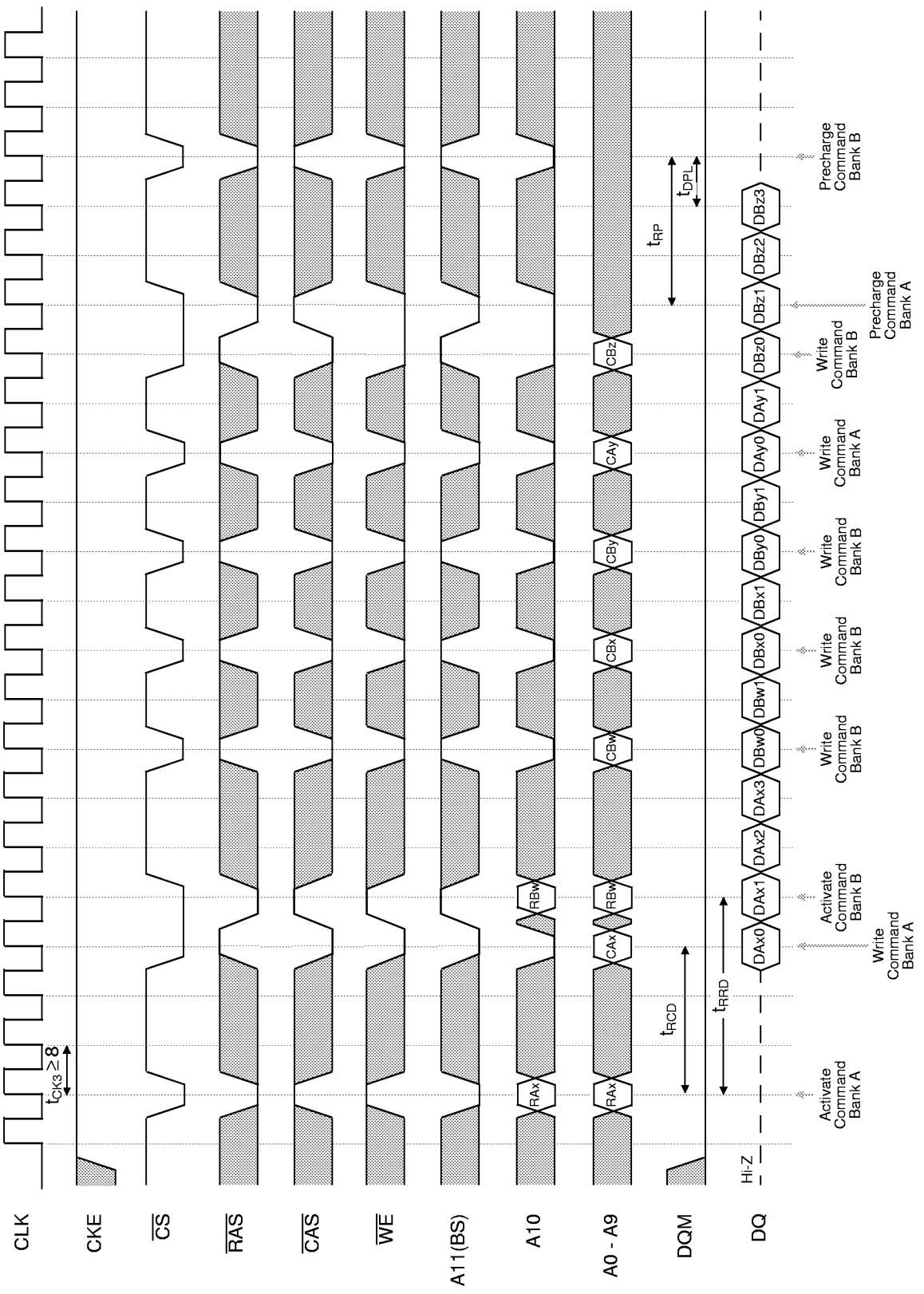
Interleaved Column Write Cycle (2 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 2



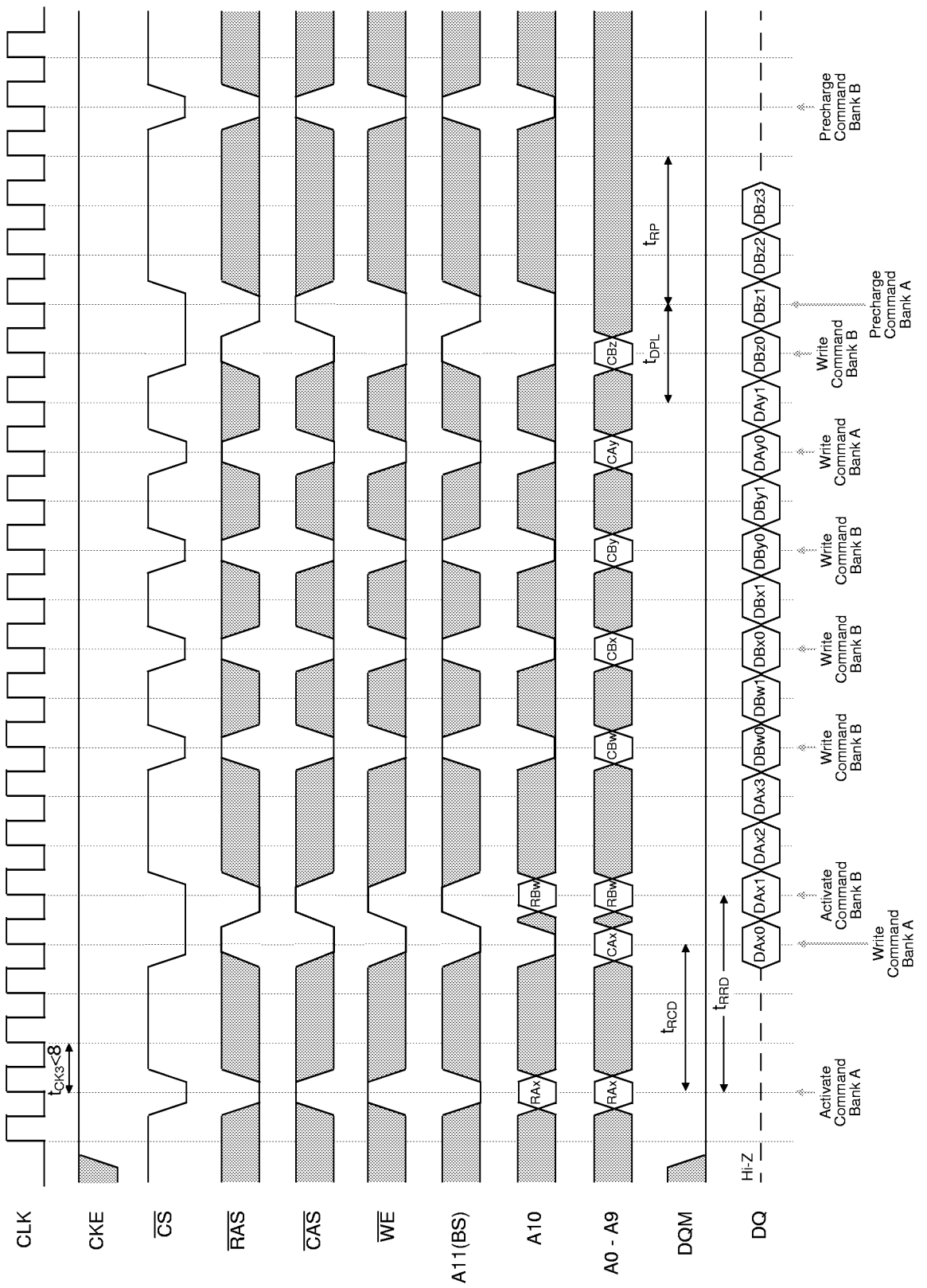
Interleaved Column Write Cycle (3 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 3, $t_{CK3} \geq 8$



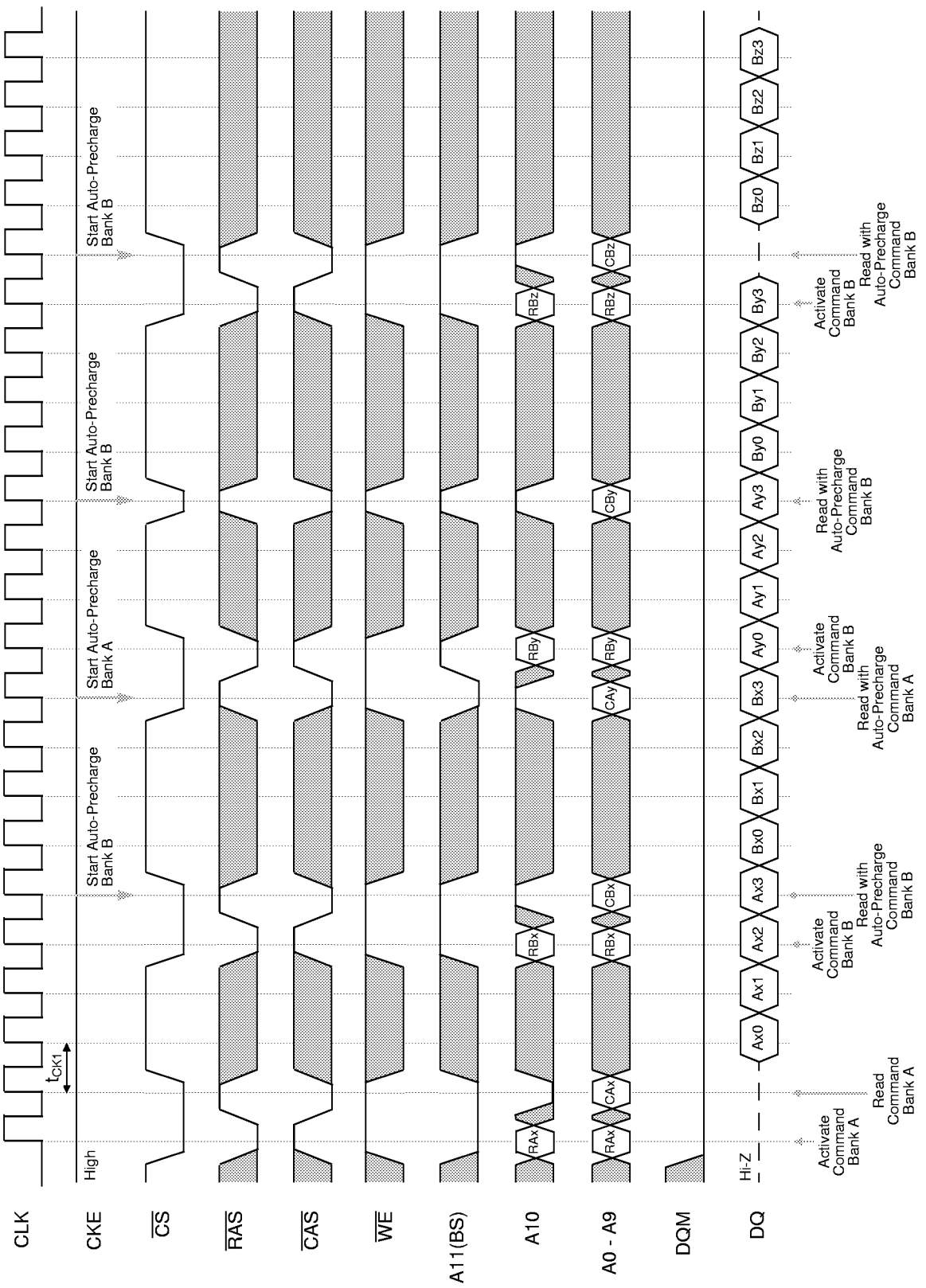
Interleaved Column Write Cycle (4 of 4)

Burst Length = 4, $\overline{CAS}$ Latency = 3, $t_{CK3} < 8$



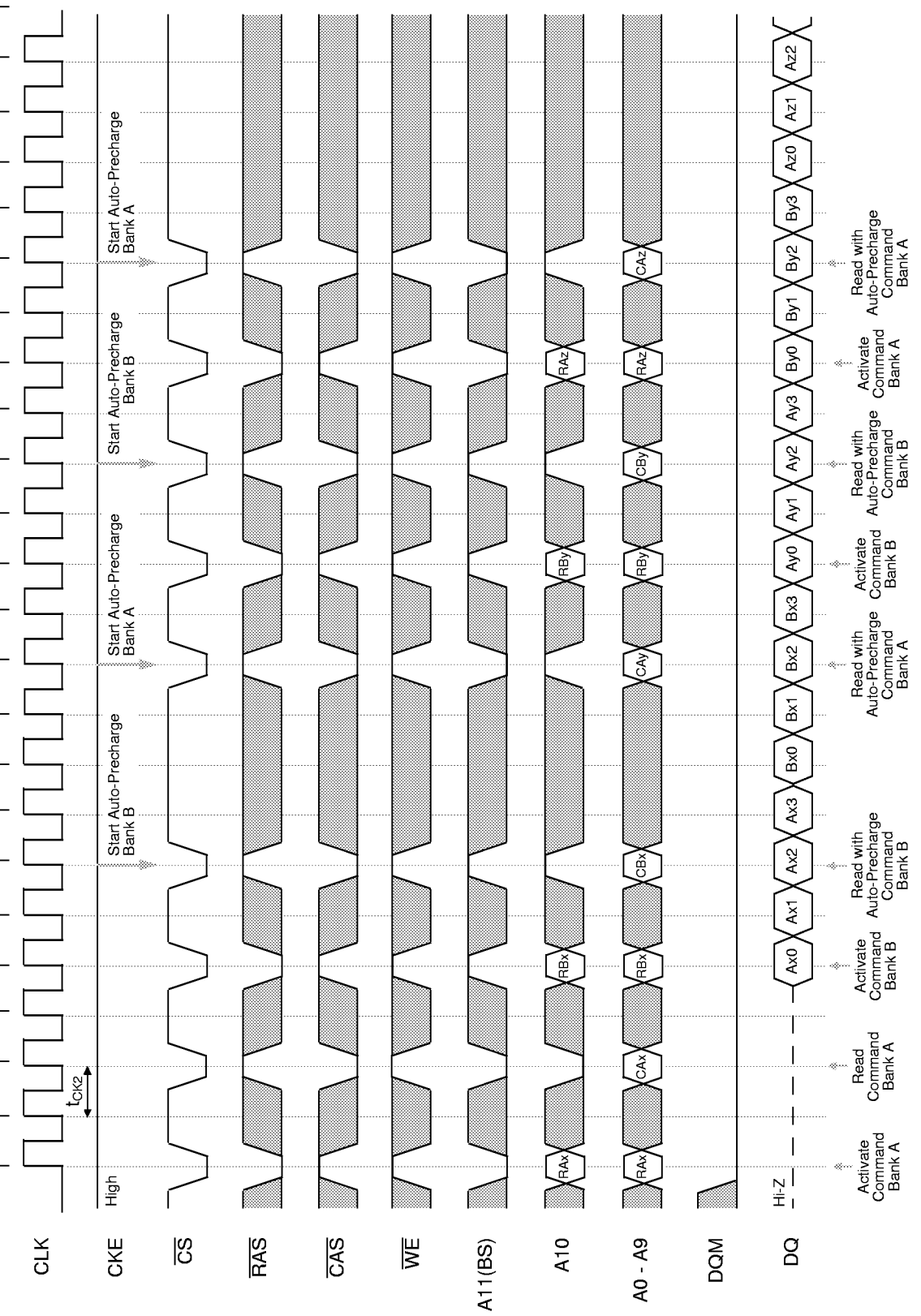
Auto-Precharge after Read Burst (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1

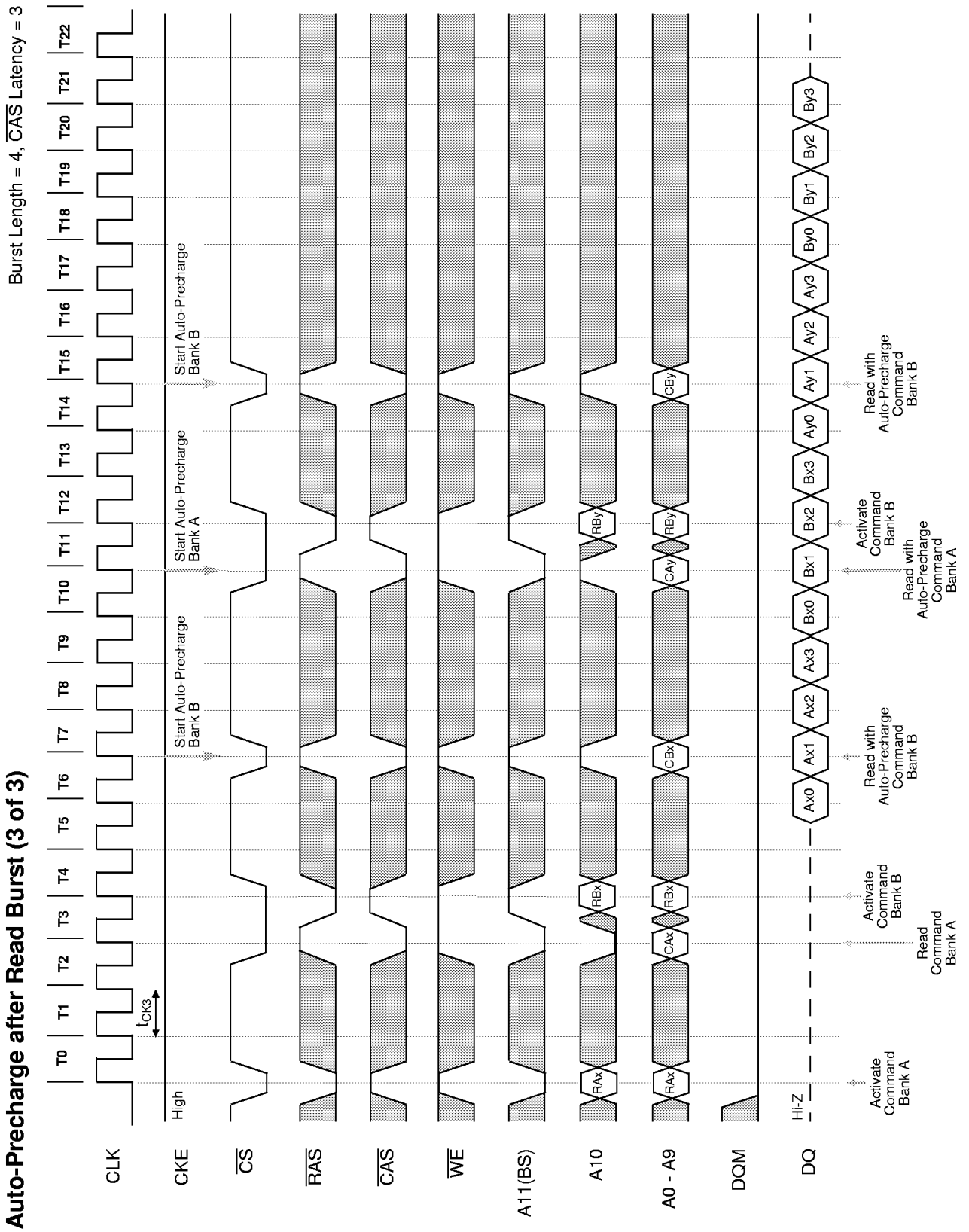


Auto-Precharge after Read Burst (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2

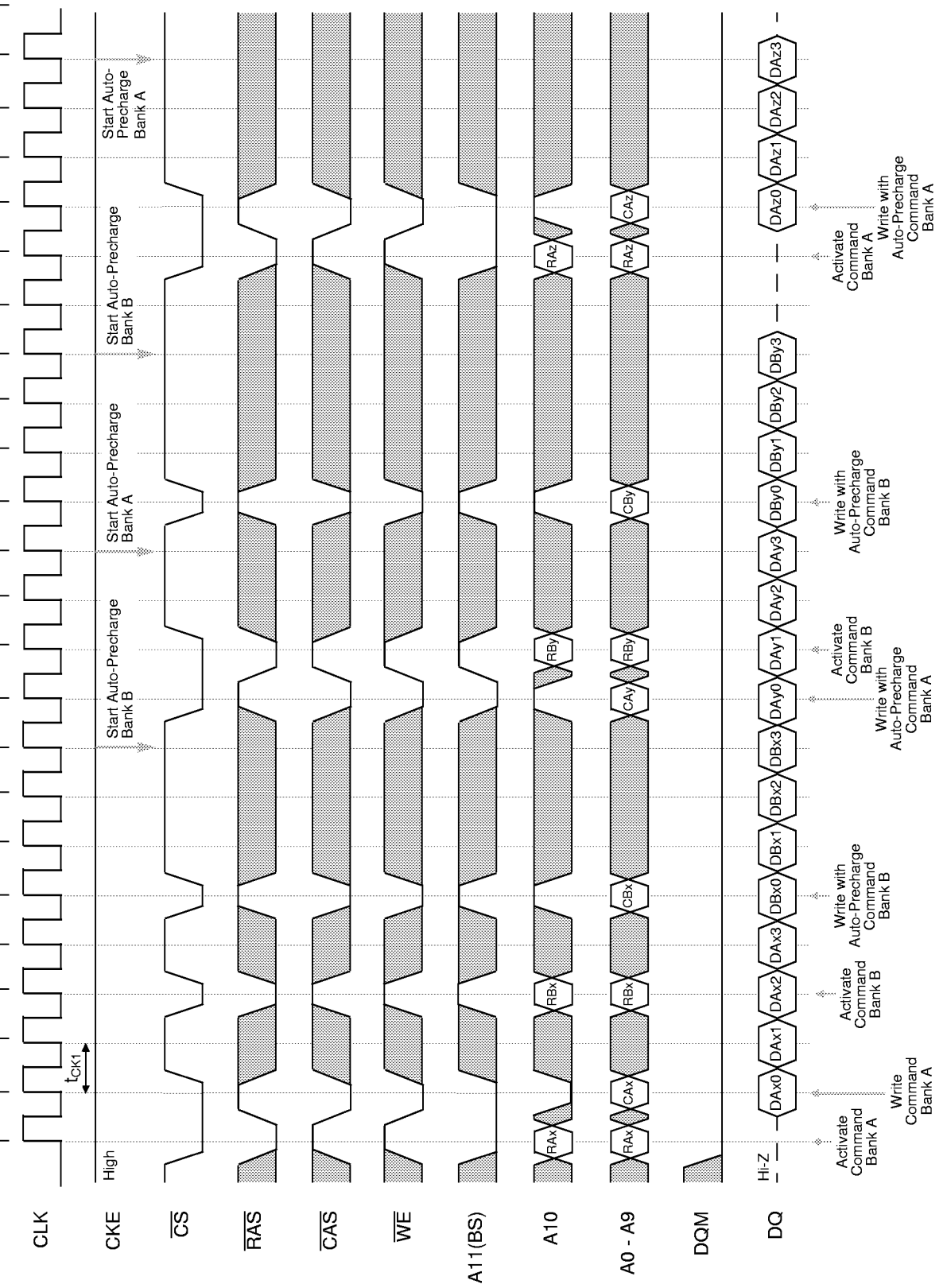


Auto-Precharge after Read Burst (3 of 3)



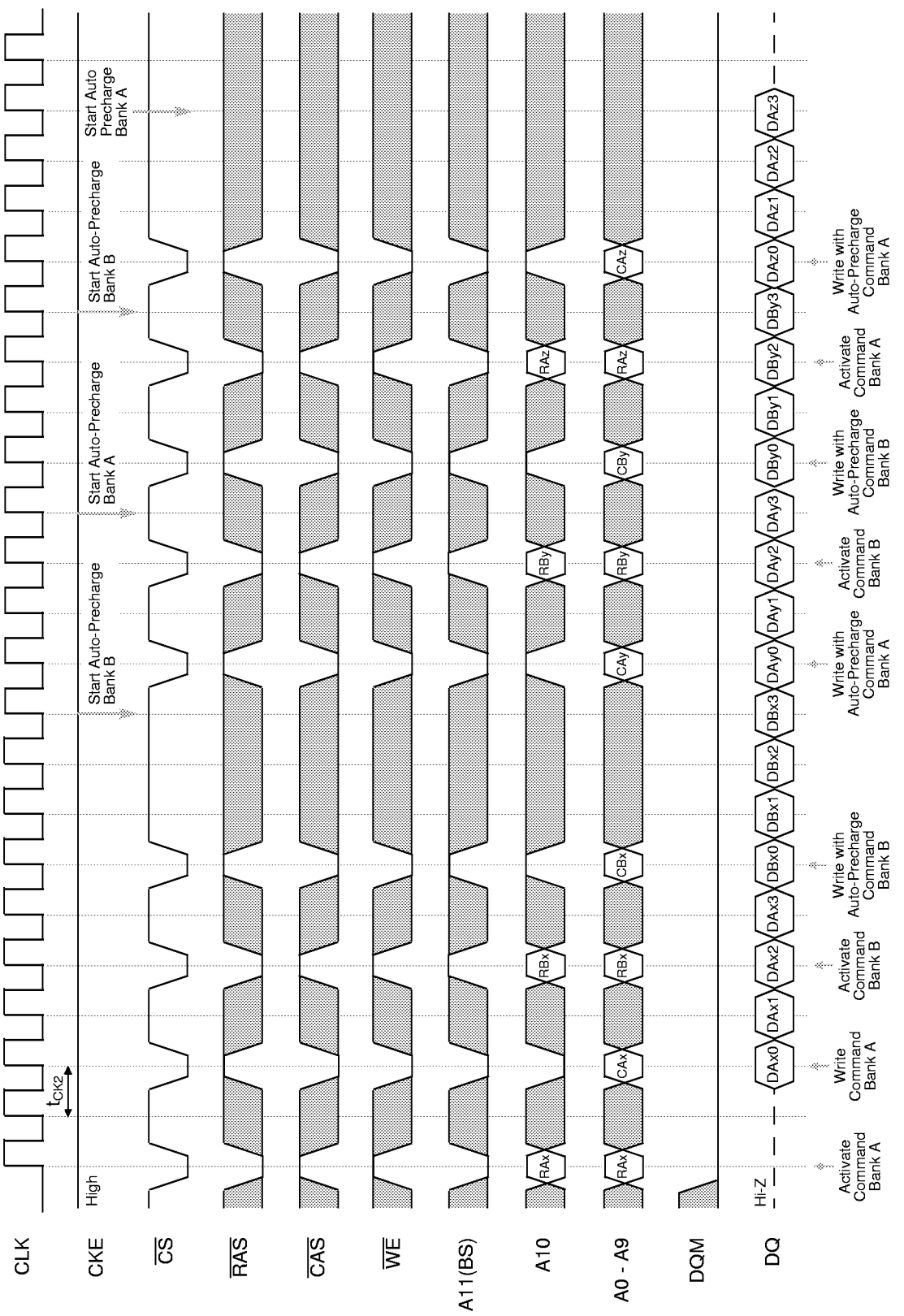
Auto-Precharge after Write Burst (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1



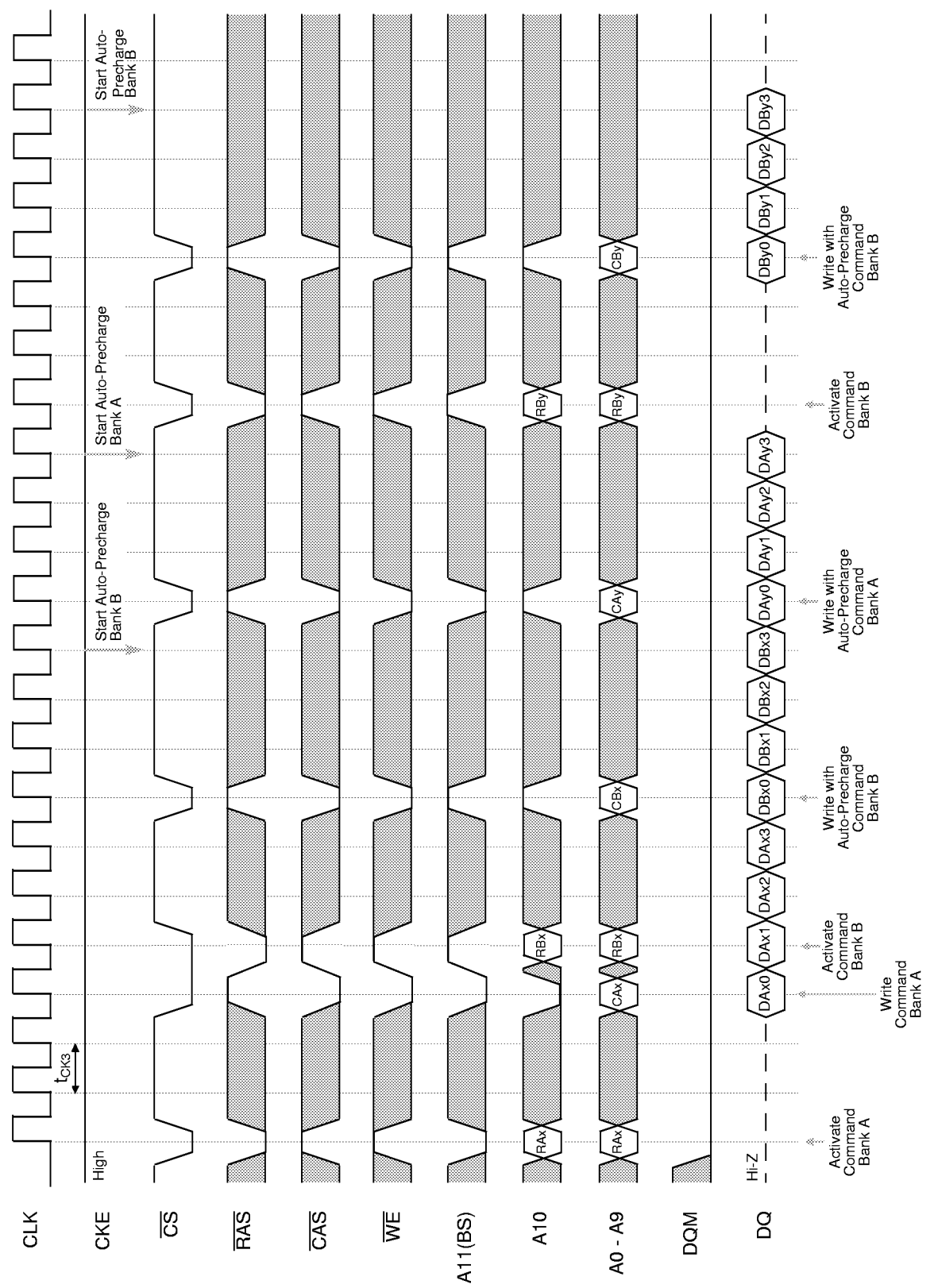
Auto-Precharge after Write Burst (2 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 2

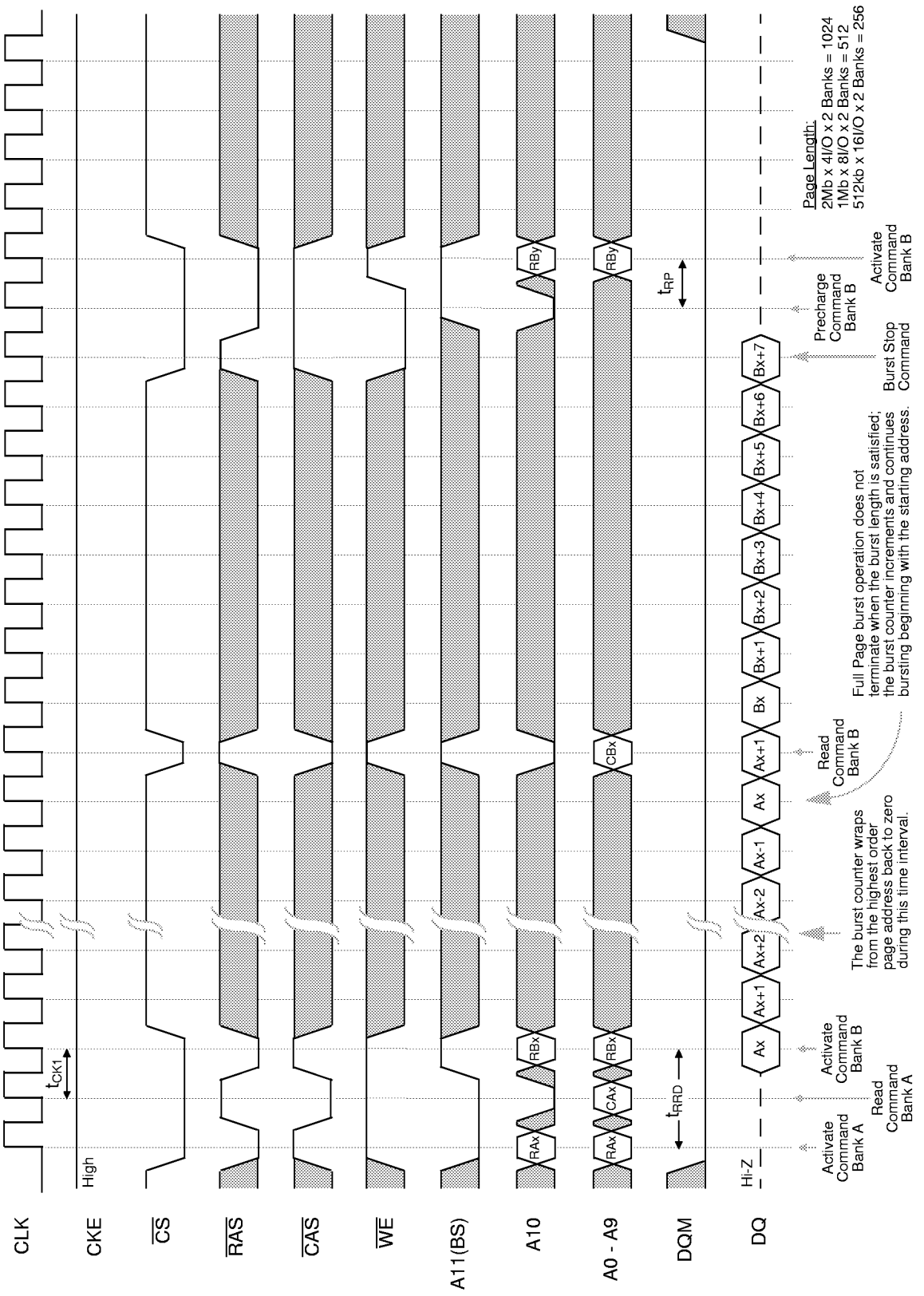


Auto-Precharge after Write Burst (3 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 3

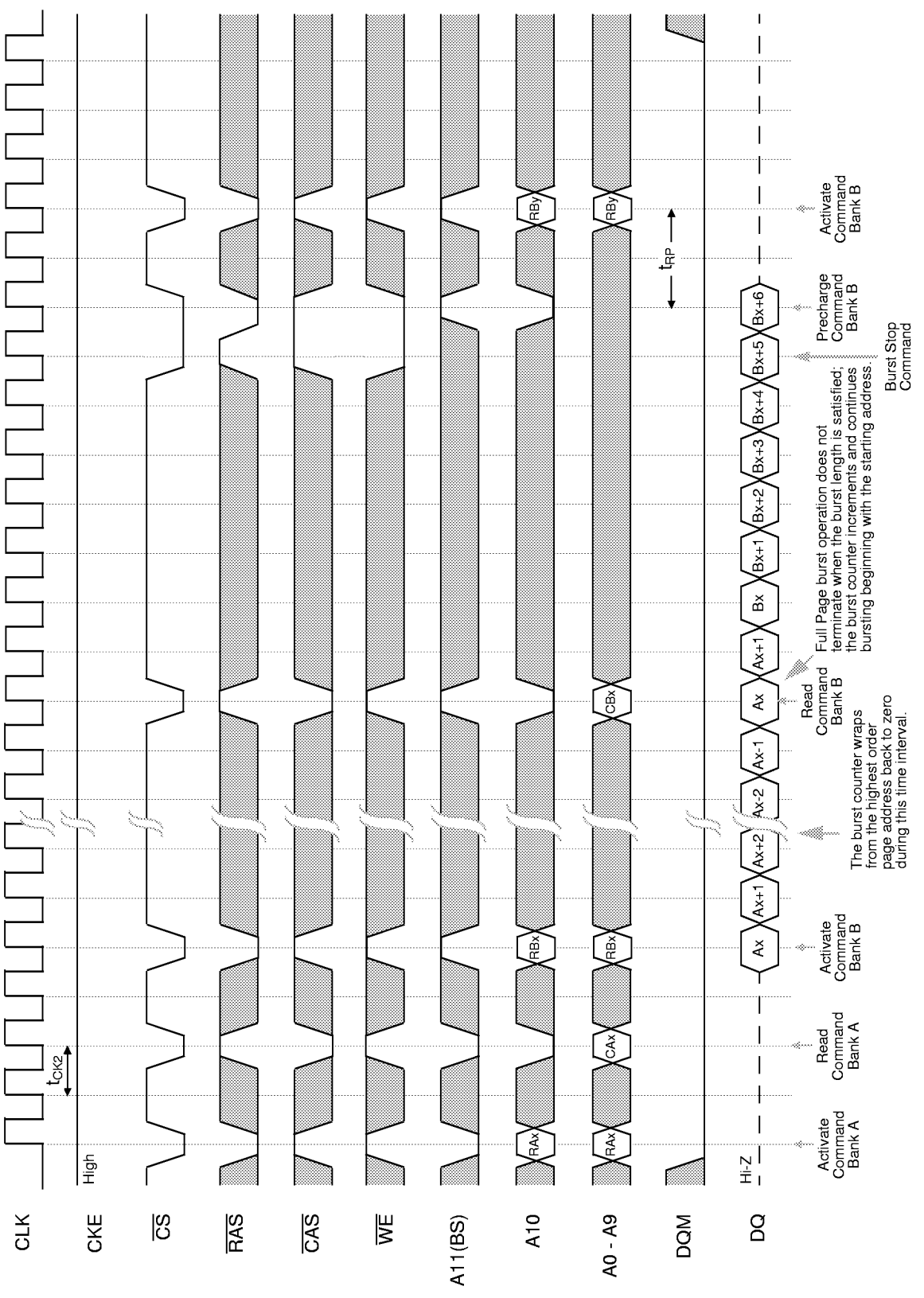


Full Page Read Cycle (1 of 3)



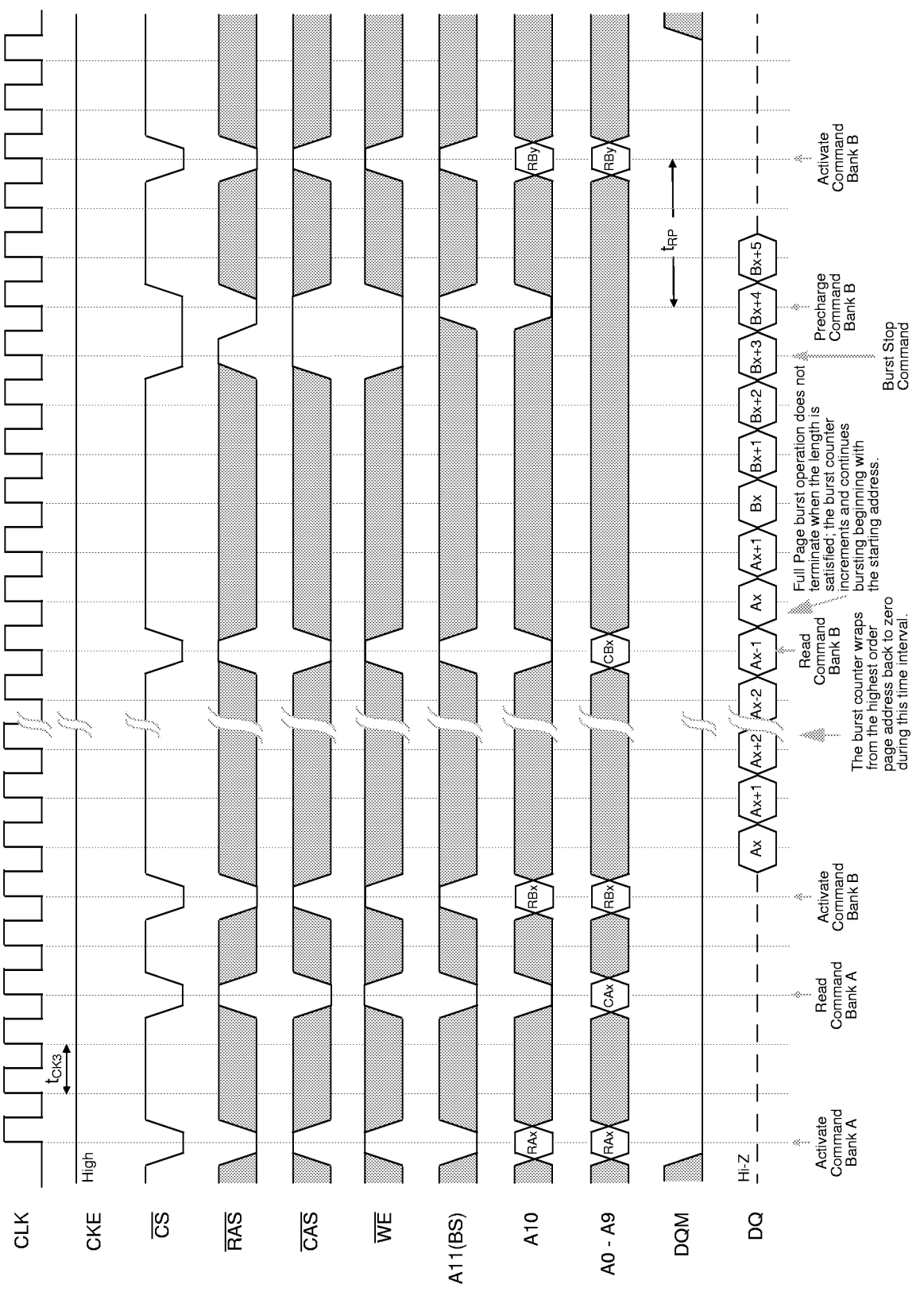
Full Page Read Cycle (2 of 3)

Burst Length = Full Page, $\overline{CAS}$ Latency = 2

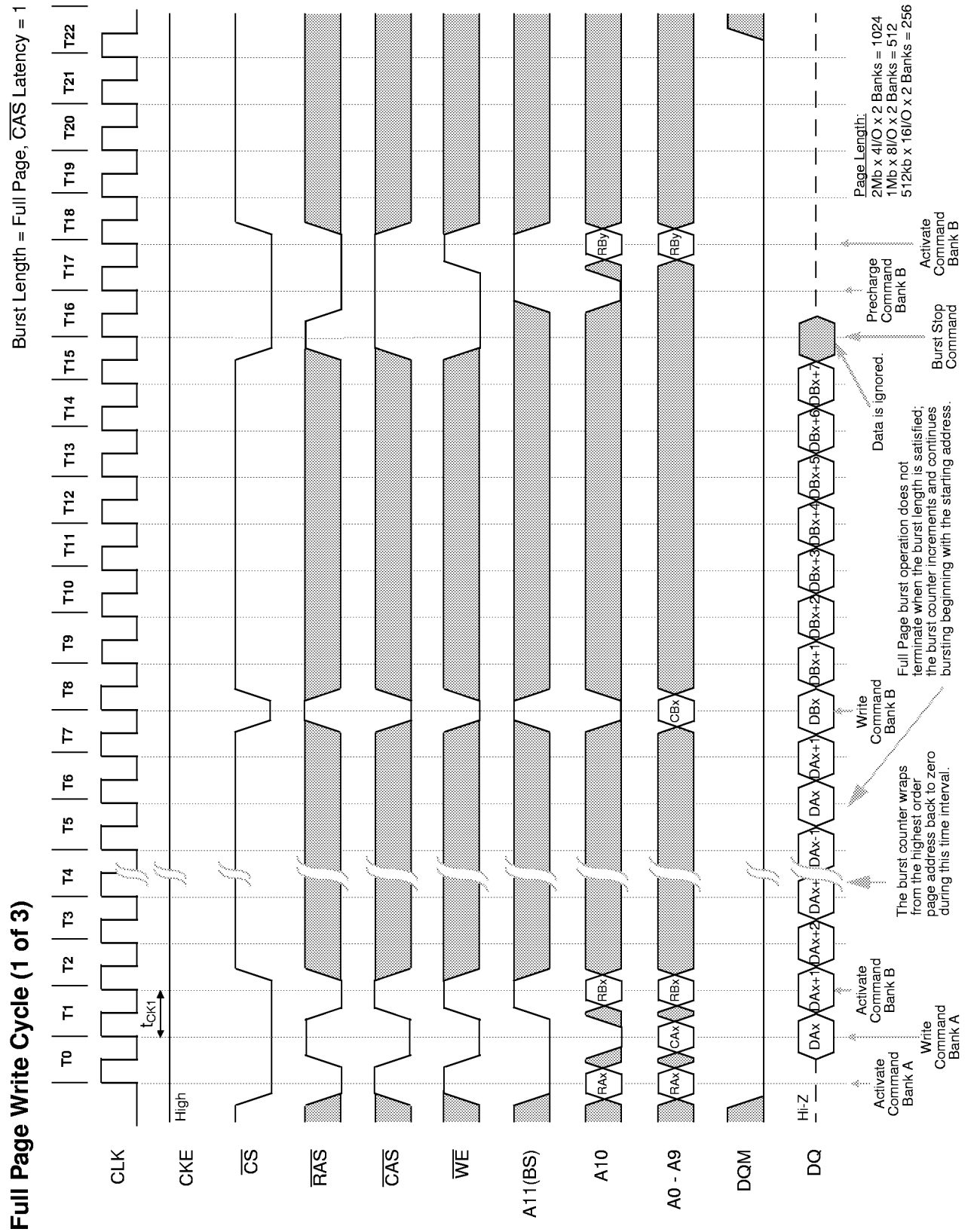


Full Page Read Cycle (3 of 3)

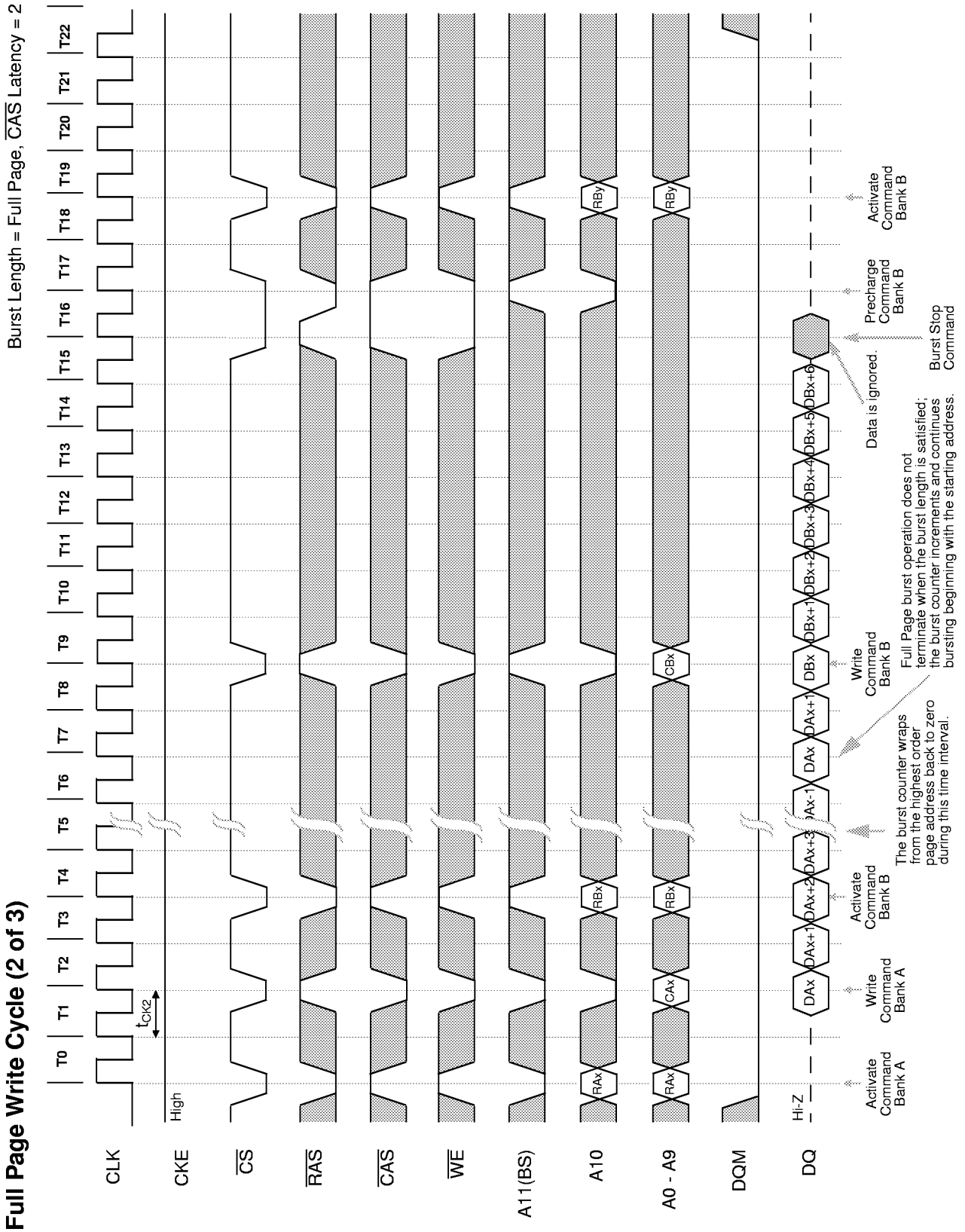
Burst Length = Full Page, $\overline{CAS}$ Latency = 3



Full Page Write Cycle (1 of 3)

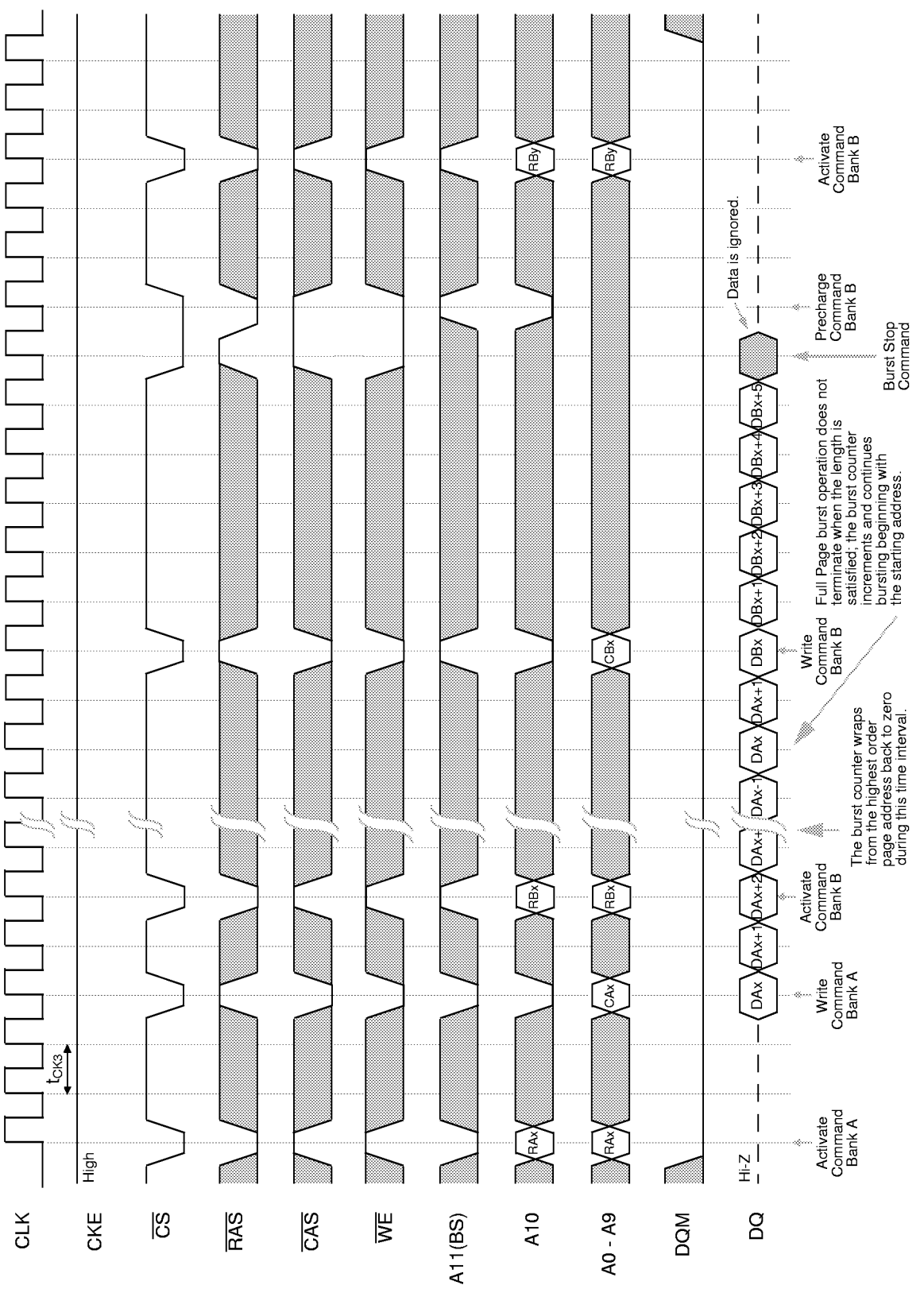


Full Page Write Cycle (2 of 3)



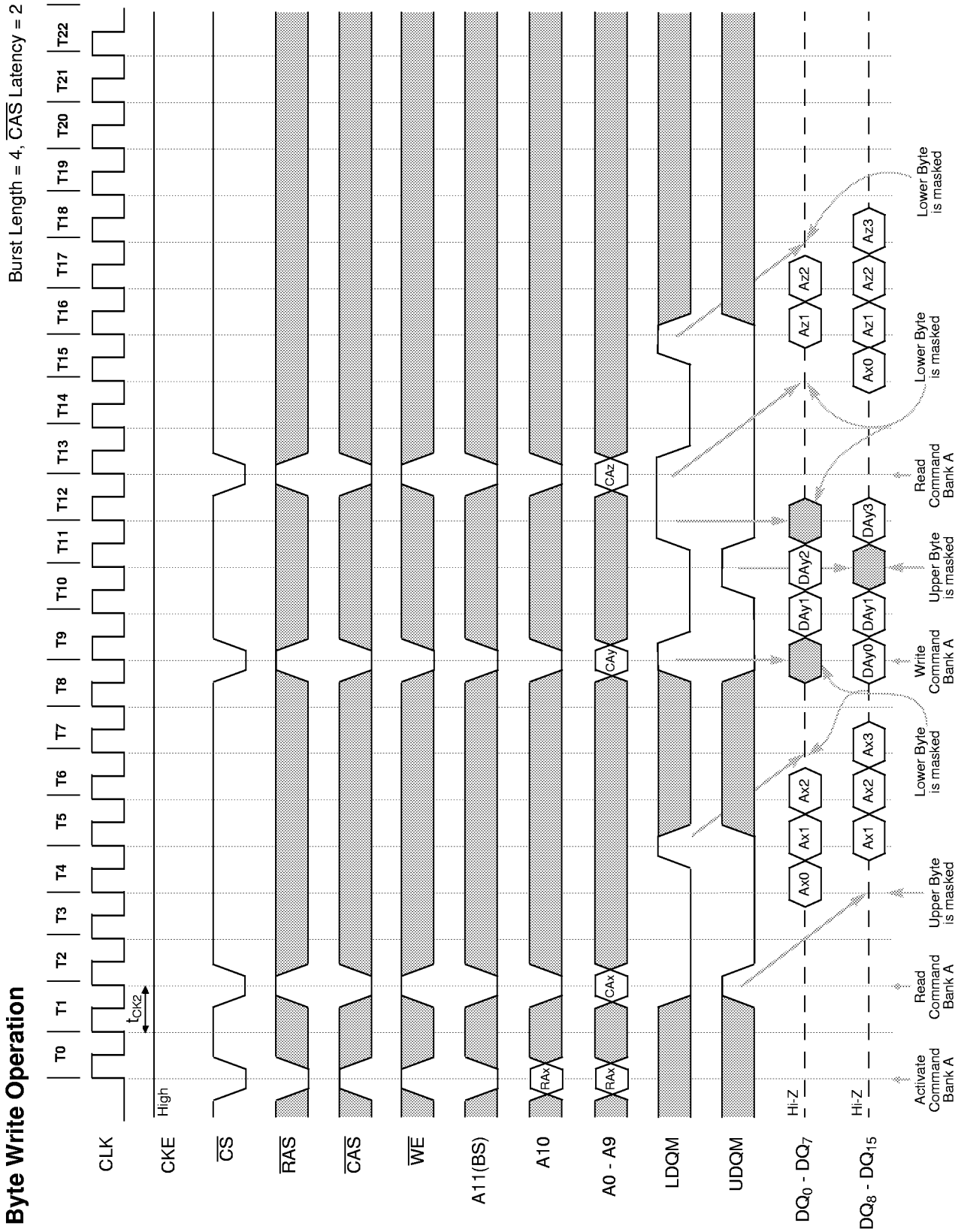
Full Page Write Cycle (3 of 3)

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



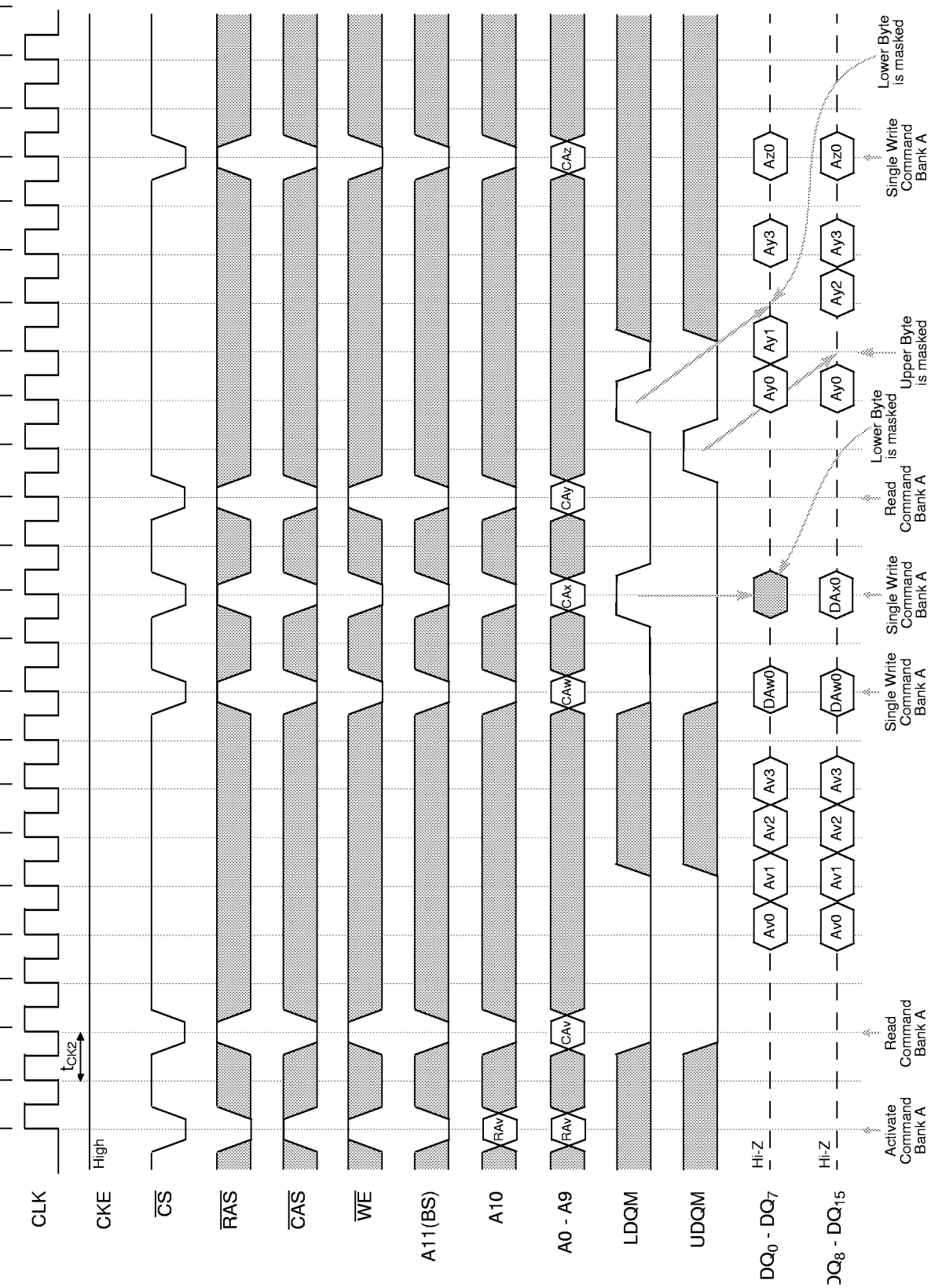
Byte Write Operation

Burst Length = 4, $\overline{CAS}$ Latency = 2



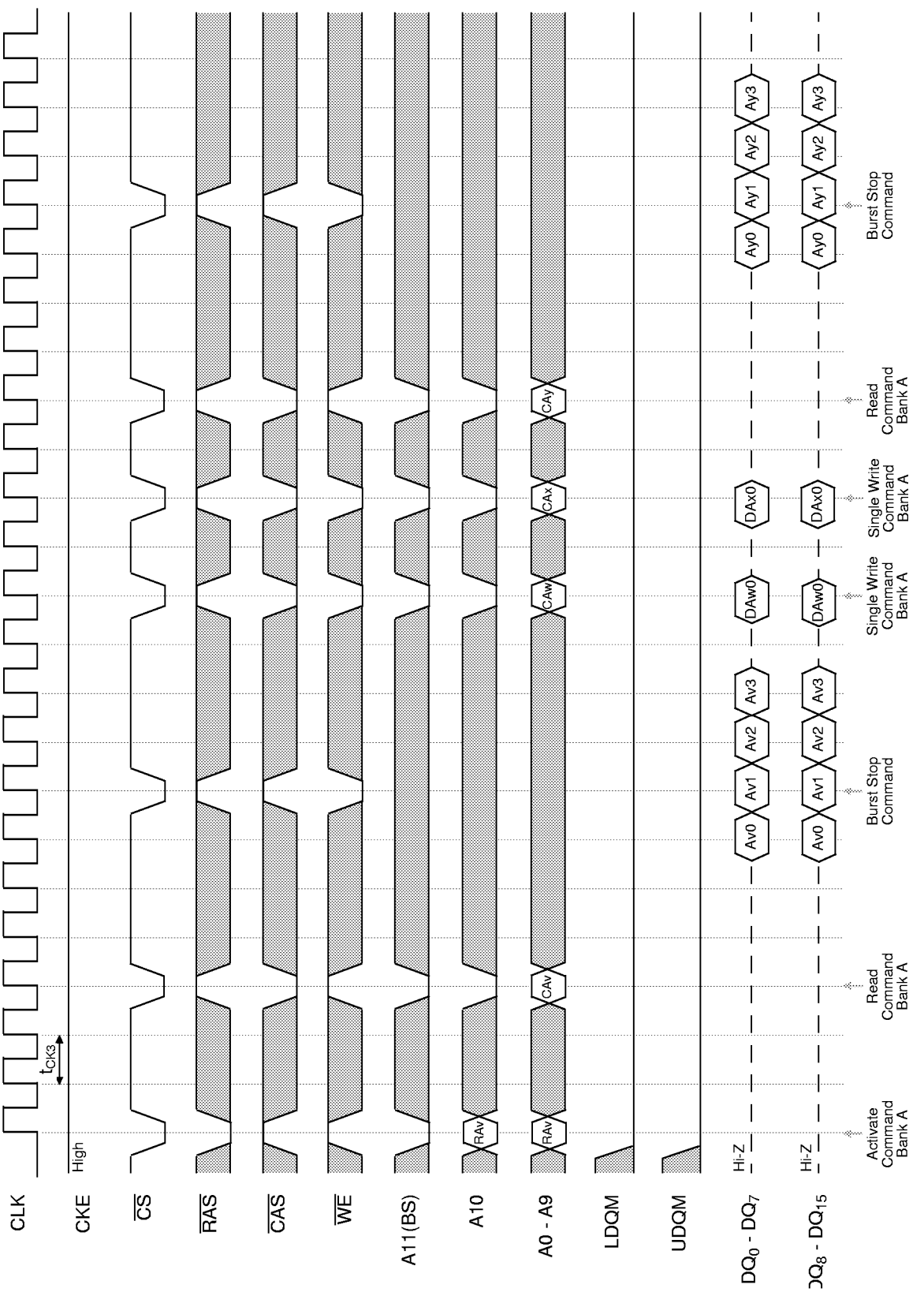
Burst Read and Single Write Operation

Burst Length = 4, $\overline{CAS}$ Latency = 2



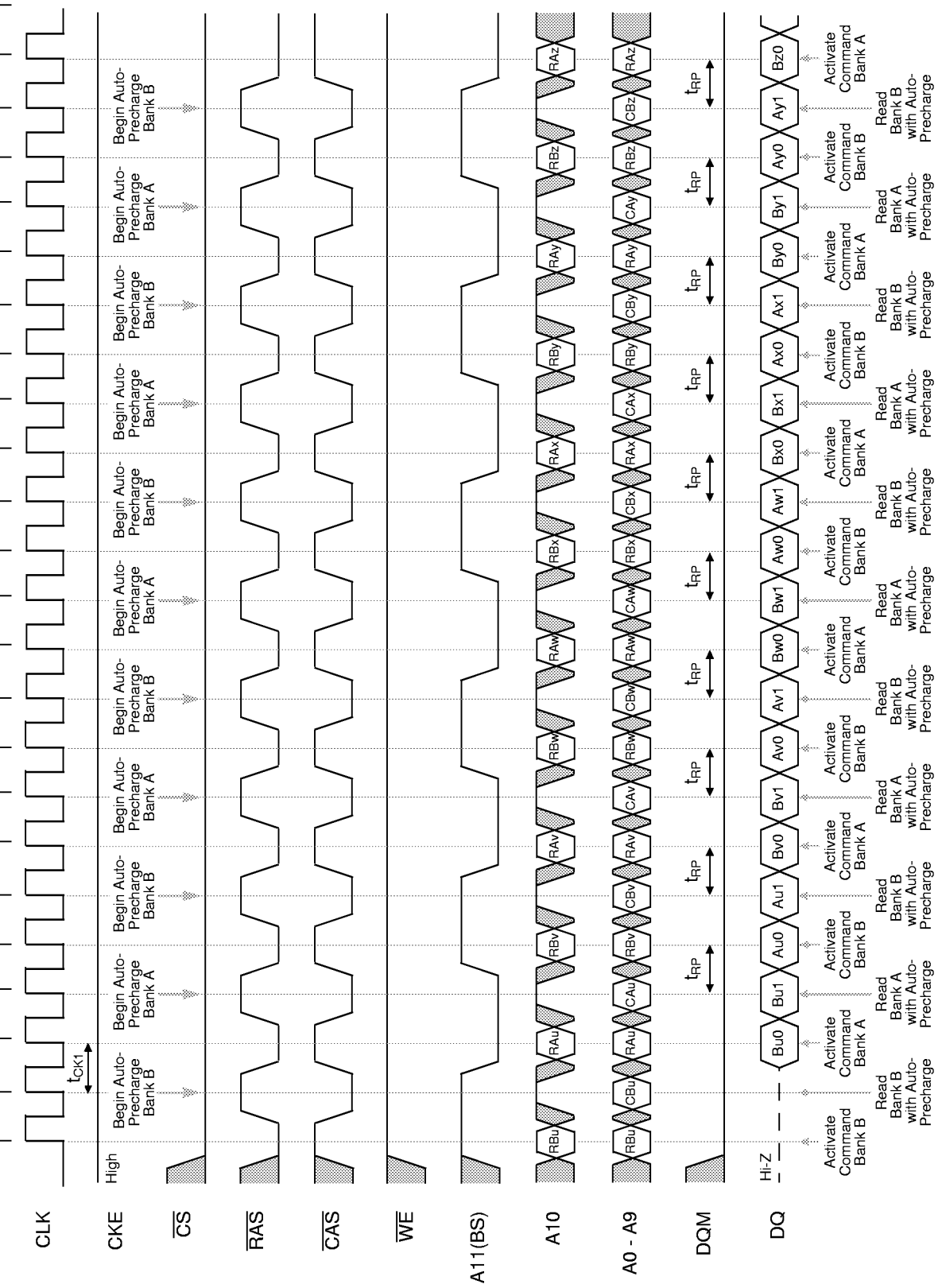
Full Page Burst Read and Single Write Operation

Burst Length = Full Page, $\overline{CAS}$ Latency = 3



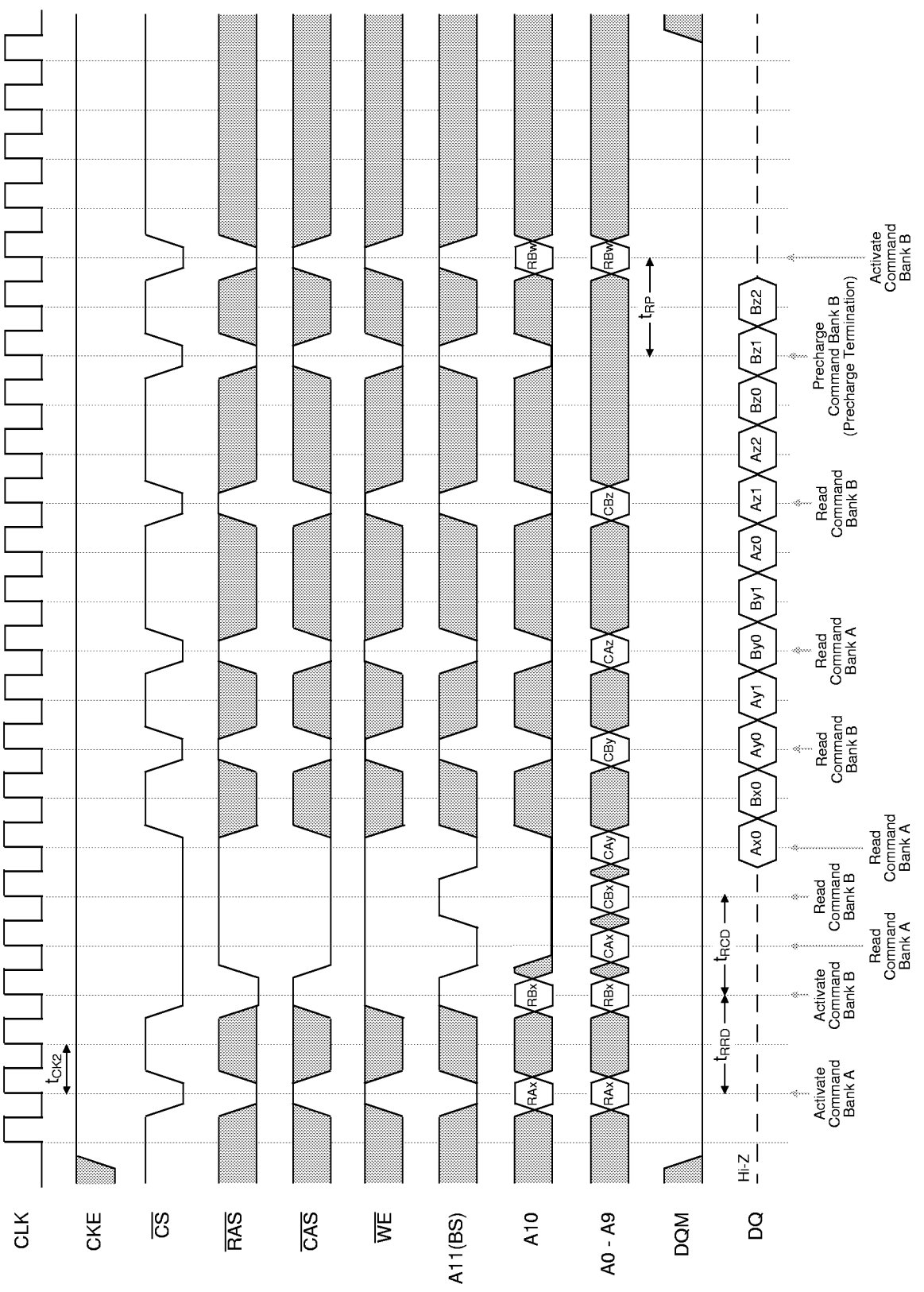
Random Row Read (Interleaving Banks)

Burst Length = 2, $\overline{CAS}$ Latency = 1



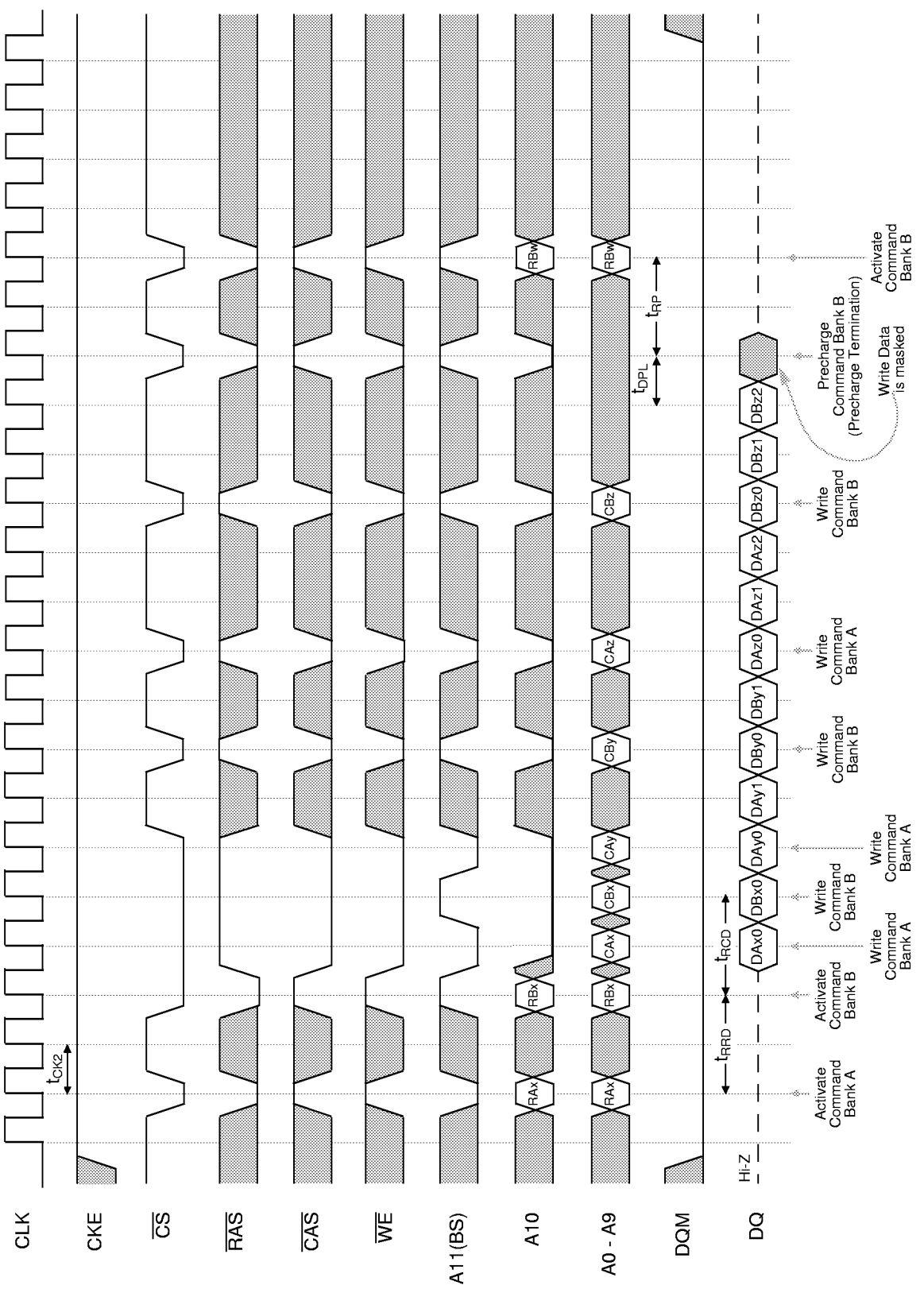
Full Page Random Column Read

Burst Length = Full Page, $\overline{CAS}$ Latency = 2



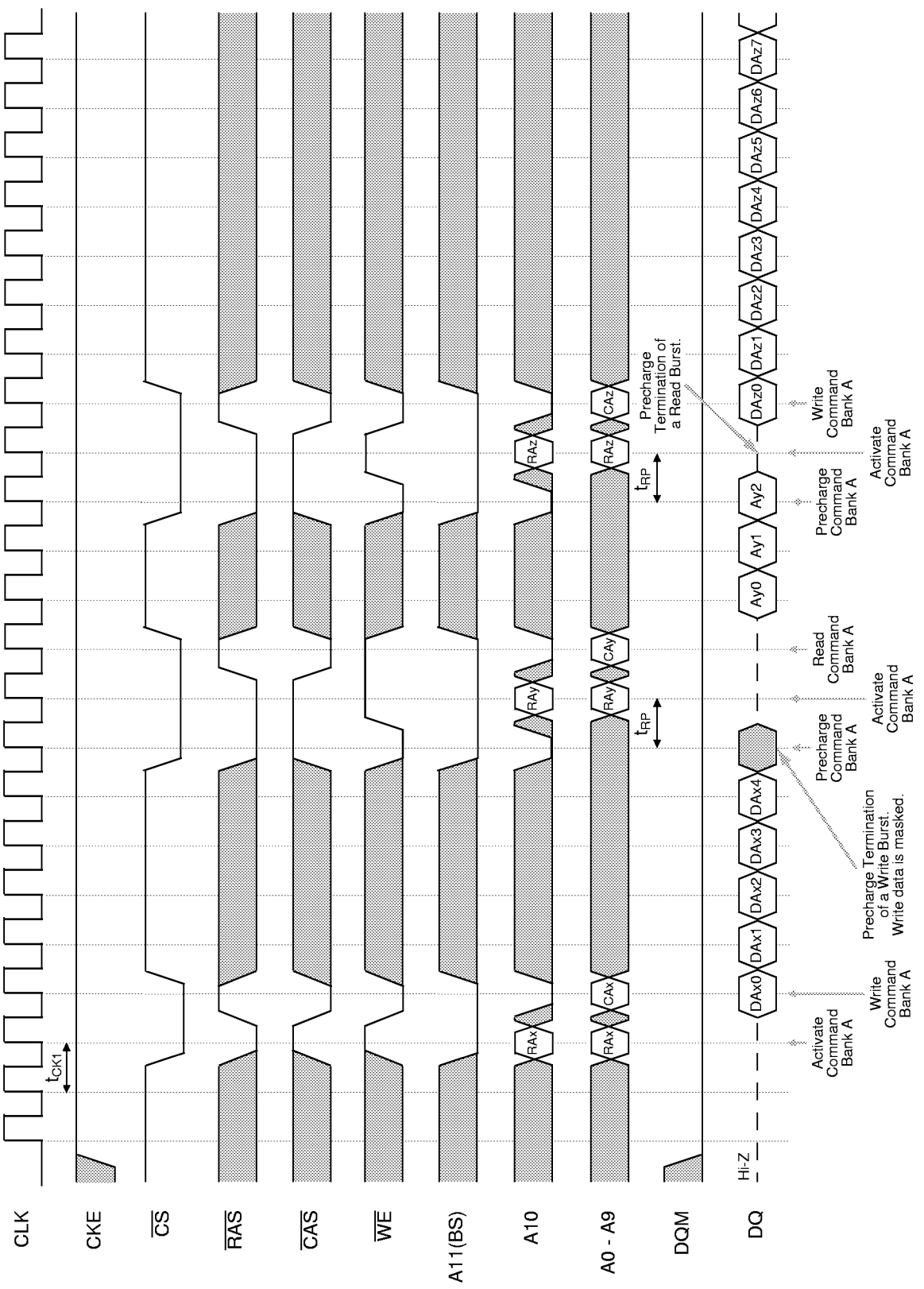
Full Page Random Column Write

Burst Length = Full Page, $\overline{CAS}$ Latency = 2



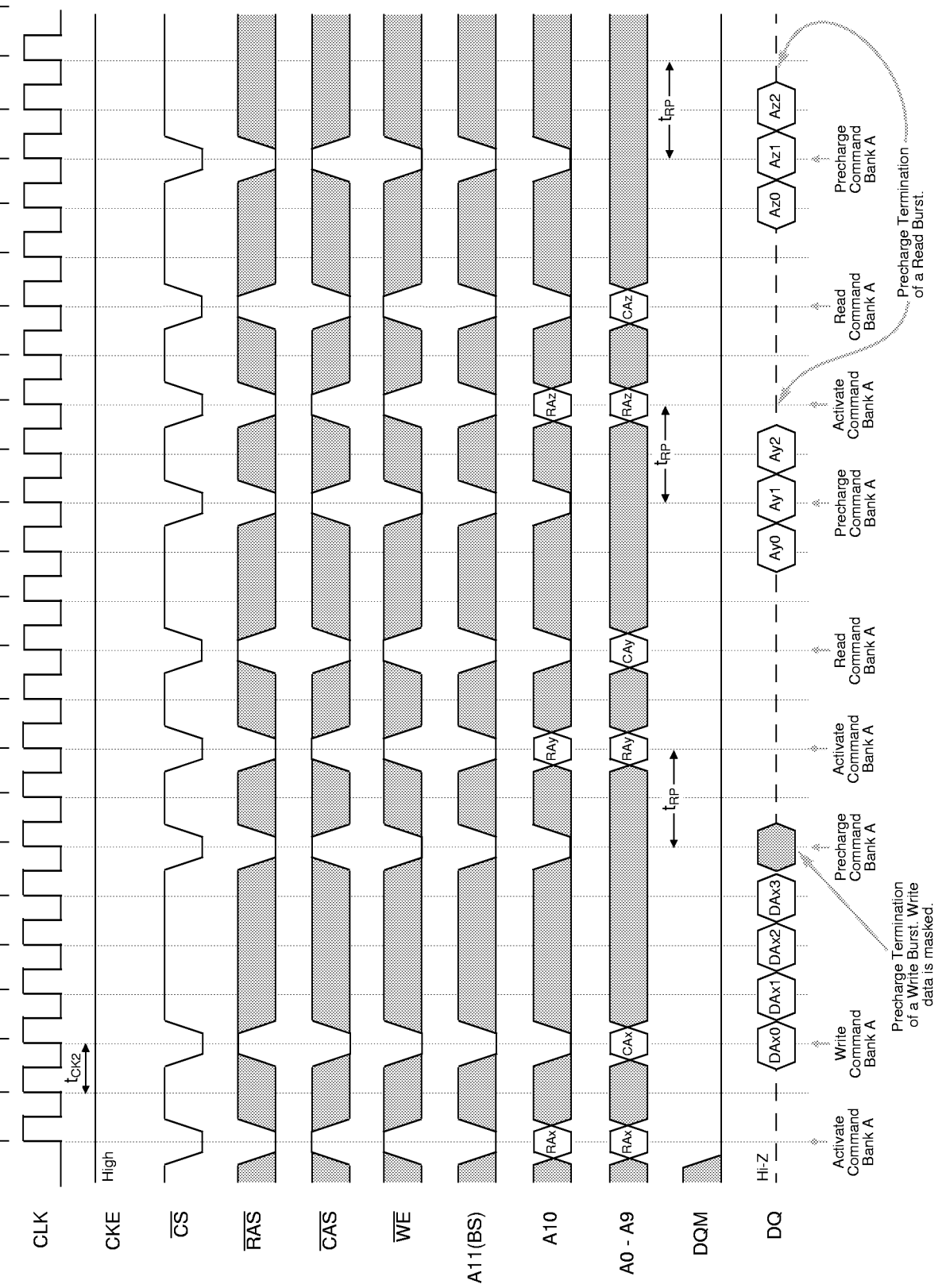
Precharge Termination of a Burst (1 of 4)

Burst Length = Full Page, $\overline{CAS}$ Latency = 1



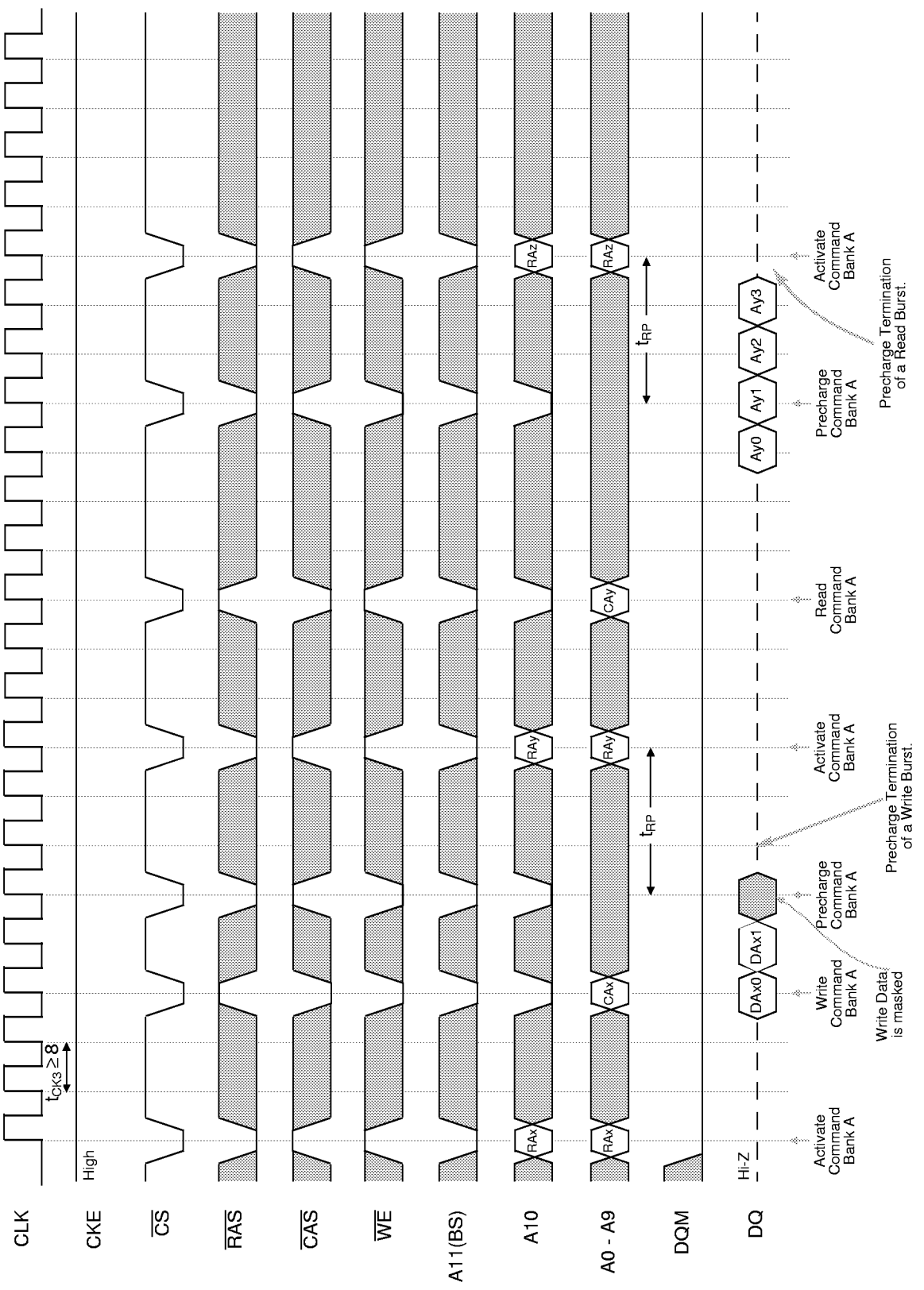
Precharge Termination of a Burst (2 of 4)

Burst Length = 8 or Full Page, $\overline{CAS}$ Latency = 2



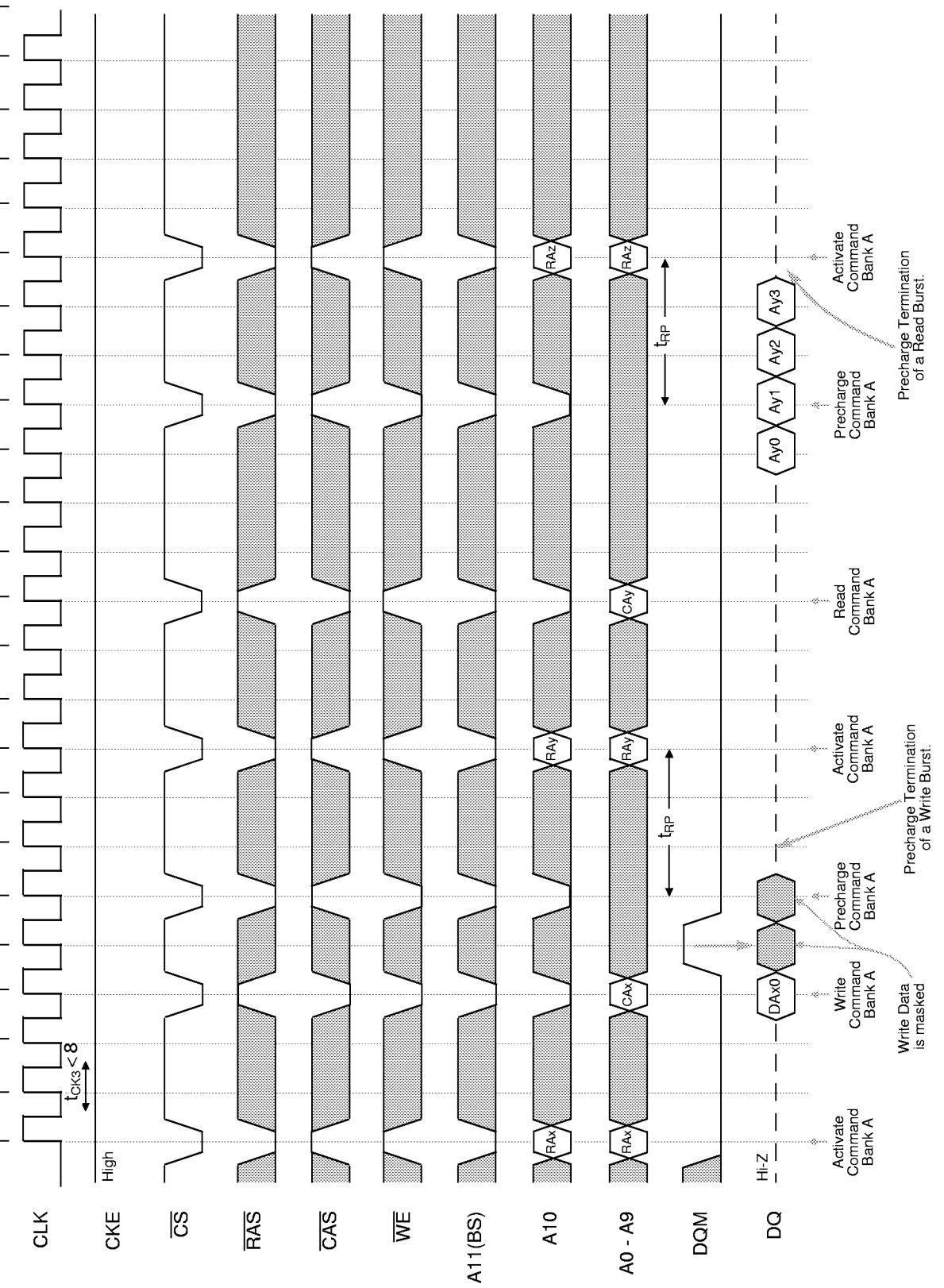
Precharge Termination of a Burst (3 of 4)

Burst Length = 4,8 or Full Page, $\overline{CAS}$ Latency = 3, $t_{CK3} \geq 8$



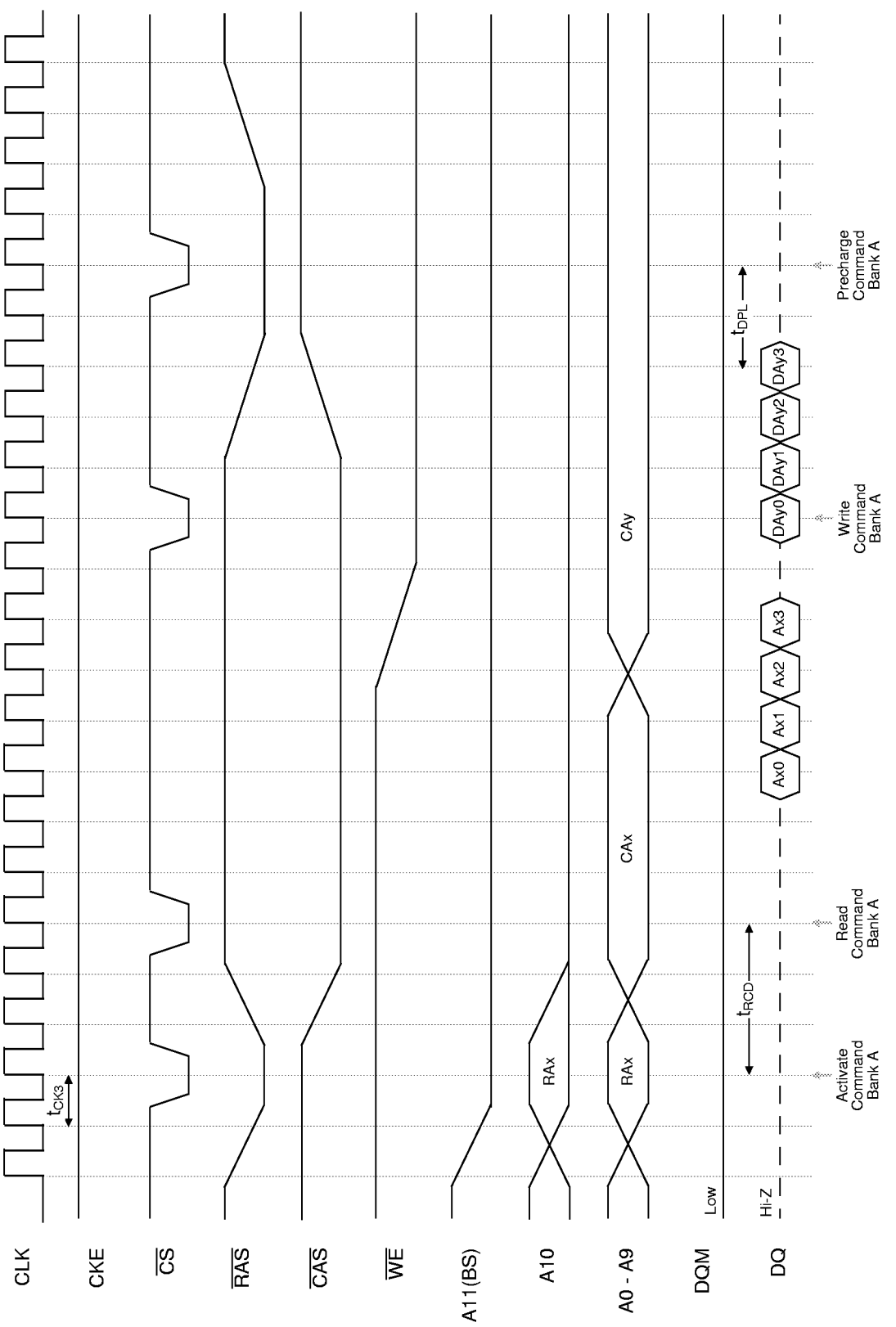
Precharge Termination of a Burst (4 of 4)

Burst Length = 4,8 or Full Page, $\overline{CAS}$ Latency = 3, $t_{CK3} < 8$

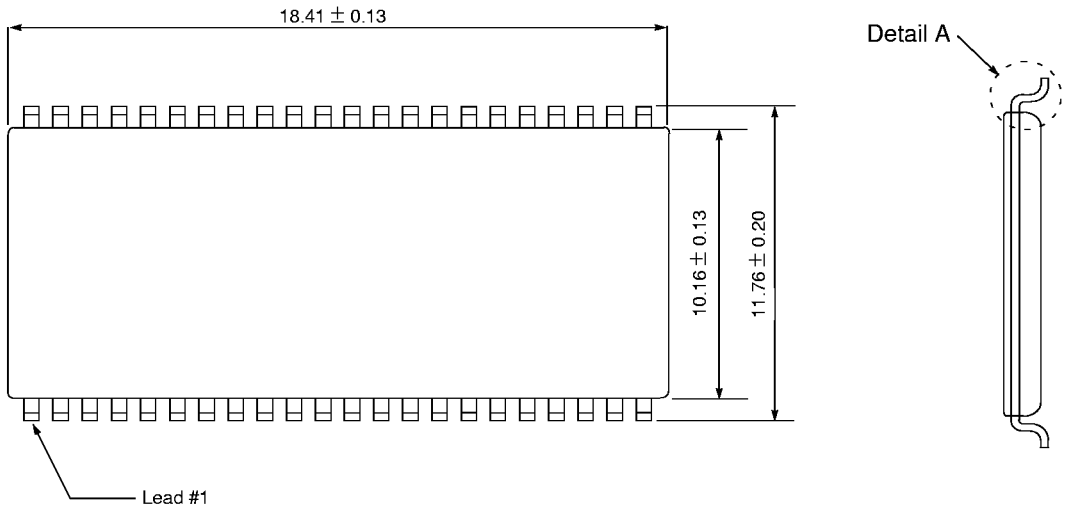


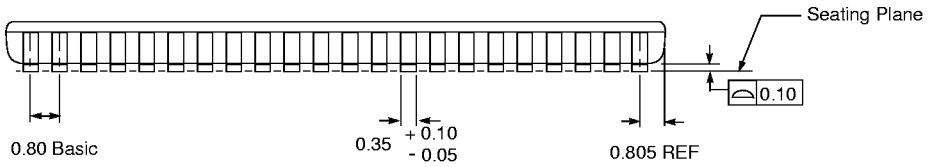
$\overline{CS}$ Function (Only $\overline{CS}$ signal needs to be asserted at minimum rate)

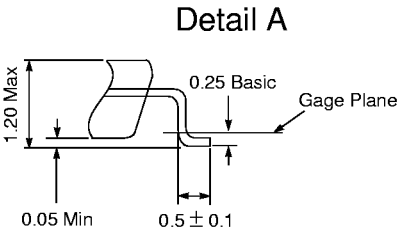
at 100MHz Burst Length = 4, $\overline{CAS}$ Latency = 3



PACKAGE DIMENSIONS (400mil; 44 lead; Thin Small Outline Package)

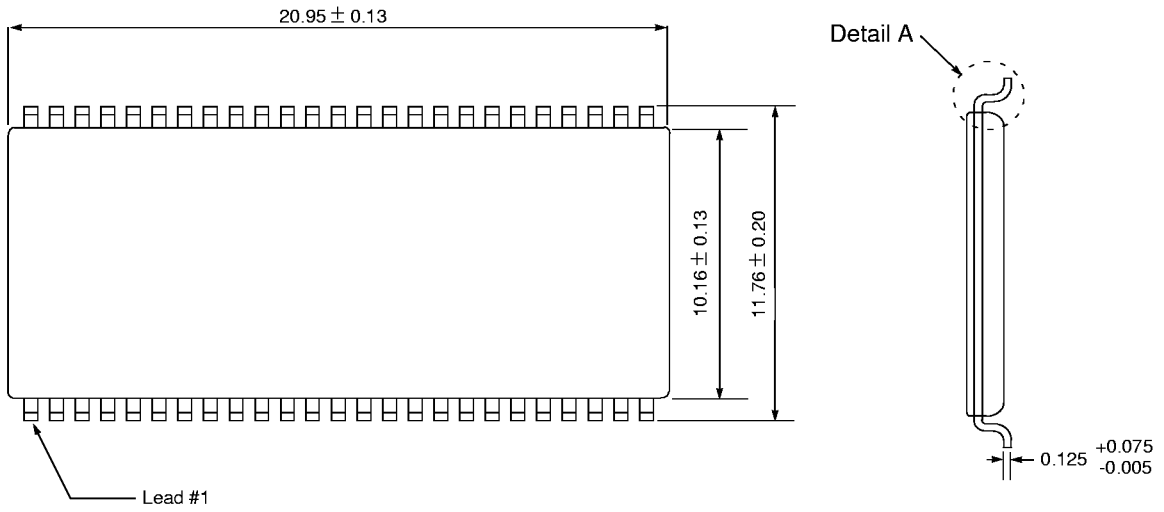


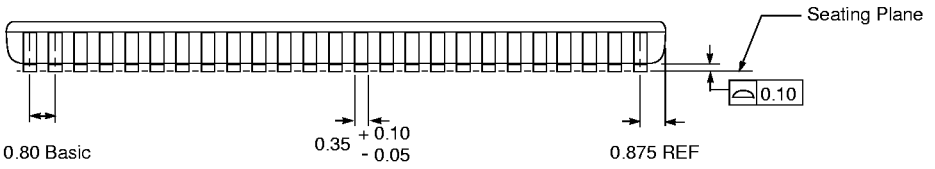


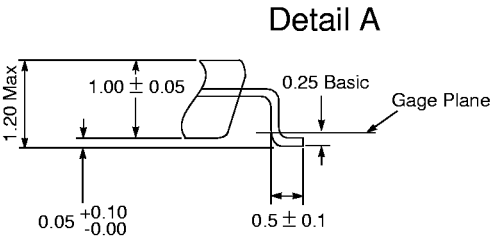


NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

PACKAGE DIMENSIONS (400mil; 50 lead; Thin Small Outline Package)

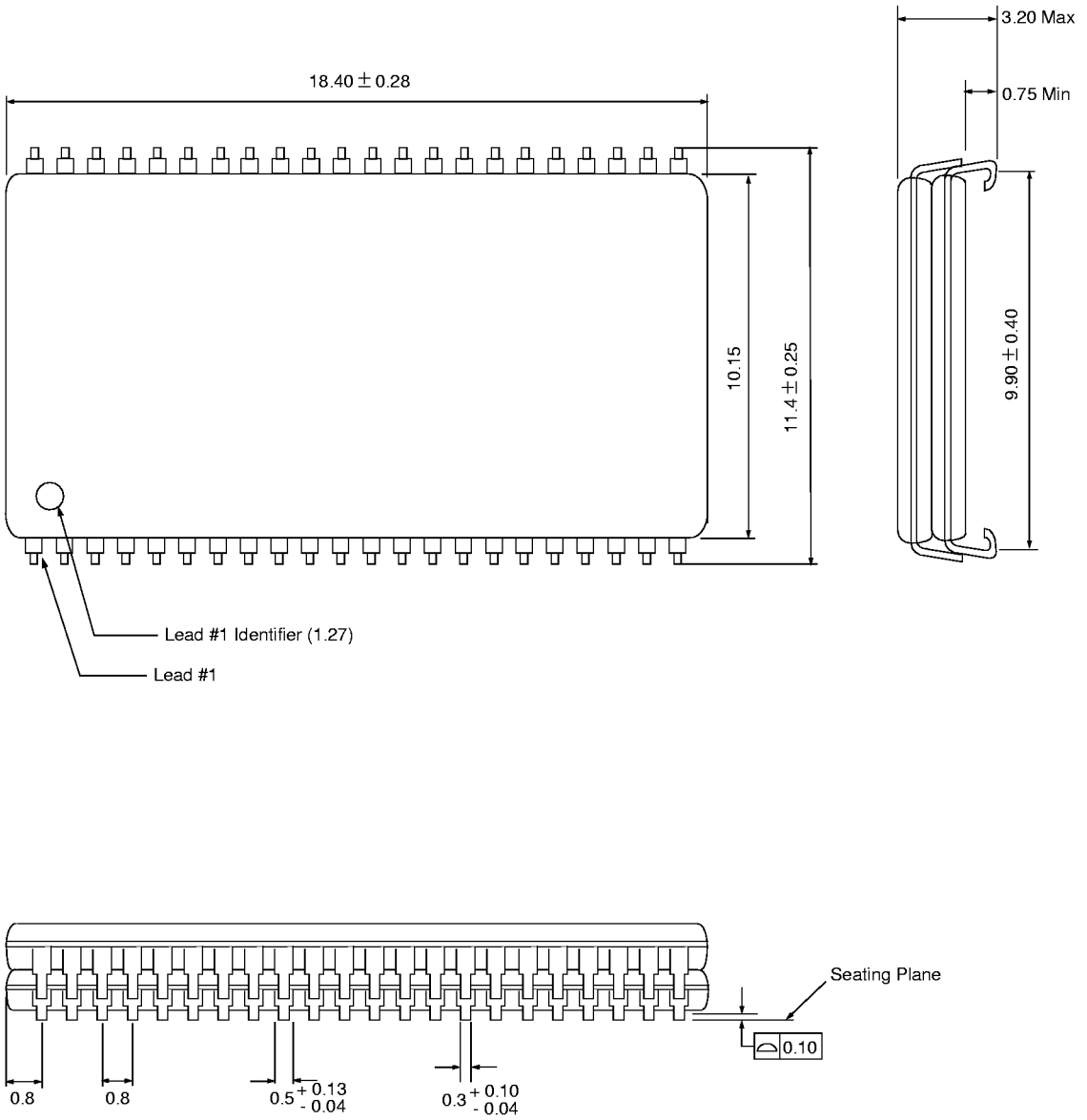






NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

PACKAGE DIMENSIONS (400mil; 44 lead; 2 High Stack; Thin Small Outline J Lead Package)



NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

Revision Log

Revision	Contents Of Modification	
2/10/97	Initial Release (Preliminary)	
5/16/97	page 23	Correction to Auto-precharge description/diagram notes. (Page 23, 24)
	page 49	Change t_{DPL} from 8ns to 10ns for -10.
	page 66	Correct CKE transition.
	page 43	Correction of note regarding total stack current (CBR current).
7/14/97	page 23	Precharge Termination changed (now similar to burst stop).
	page 24	
	page 26	
	page 27	
	page 65	Correct $\overline{WE}$ - Read Command.
	page 69	Precharge Termination changed: precharge and subsequent commands 1 clock sooner.
	page 69	Correct A10 - Precharge Command A.
	page 85	Precharge Termination changed: last precharge 1 clock sooner.
	page 93	Fix numbering of data - address Az.
	page 94	Fix numbering of data - address Az.
	page 96	Correct A10 - Read Command.
	page 99	Correct A10 - first Write Command.
	page 108	Correct A10 - Write and Read Commands.
	page 110	Precharge Termination: number of data bits after command changed.
	page 111	Precharge Termination: number of data bits after command changed.

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