

256Mbit GDDR SDRAM

**Revision 1.6
March 2005**

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Revision History**Revision 1.6 (May 26, 2005)**

- Added CL3 of MRS table

Revision 1.5 (March 16, 2005)

- Corrected the spec revision history from 1.1 ~ 1.4 as below.

Revision 1.4 (March 10, 2005)

- Added a tCK(min) value for -GC33@CL=3

Revision 1.3 (March 04, 2005)

- Removed K4D553235F-GC22 from the datasheet

Revision 1.2 (February 03, 2005)

- Removed -GJ from the spec which is no longer valid.
- Added a couple of note below AC timing table.

Revision 1.1 (December 14, 2004)

- Removed K4D553235F-GC20 from the specification.
- Dualized the 400MHz part's part number by its operating voltage. Newly added -GJ25 operating voltage is equal to 2.0V(typical) which is in mass production now. The 400MHz part with VDD & VDDQ= 1.8V(typical) which represented as -GC25 will be available by the 2nd quarter of '05
- Added a couple of note below AC timing table.

Revision 1.0 (September 21, 2004)

- Defined DC specification

Revision 0.1 (June 16, 2004) - Target Spec

- Defined target specification

Revision 0.0 (May 07, 2004) - Target Spec

- Defined target specification

**2M x 32Bit x 4 Banks Graphic Double Data Rate Synchronous DRAM
with Bi-directional Data Strobe and DLL****FEATURES**

- 1.8V ± 0.1V power supply for device operation
- 1.8V ± 0.1V power supply for I/O interface
- SSTL_18 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 4, 5 and 6 (clock)
 - Burst length (2, 4 and 8)
 - Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
- 4 DQS's (1DQS / Byte)
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- 144-Ball FBGA
- Maximum clock frequency up to 450MHz
- Maximum data rate up to 900Mbps/pin

ORDERING INFORMATION

| Part NO. | Max Freq. | Max Data Rate | Interface | Package |
|-----------------|-----------|---------------|-----------|---------------|
| K4D553235F-GC25 | 400MHz | 800Mbps/pin | SSTL_18 | 144-Ball FBGA |
| K4D553235F-GC2A | 350MHz | 700Mbps/pin | | |
| K4D553235F-GC33 | 300MHz | 600Mbps/pin | | |

* K4D553235F-VC is the Lead Free package part number.

GENERAL DESCRIPTION**FOR 2M x 32Bit x 4 Bank DDR SDRAM**

The K4D553235F is 268,435,456 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 2,097,152 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 3.6GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION (Top View)

| | | | | | | | | | | | | |
|----------|-------------------------|------------------------|----------|----------|-------------|-------------|-------------|------------------|------------------|-----------|------------------------|-----------|
| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| B | DQS0 | DM0 | VSSQ | DQ3 | DQ2 | DQ0 | DQ31 | DQ29 | DQ28 | VSSQ | DM3 | DQS3 |
| C | DQ4 | VDDQ | NC | VDDQ | DQ1 | VDDQ | VDDQ | DQ30 | VDDQ | NC | VDDQ | DQ27 |
| D | DQ6 | DQ5 | VSSQ | VSSQ | VSSQ | VDD | VDD | VSSQ | VSSQ | VSSQ | DQ26 | DQ25 |
| E | DQ7 | VDDQ | VDD | VSS | VSSQ | VSS | VSS | VSSQ | VSS | VDD | VDDQ | DQ24 |
| F | DQ17 | DQ16 | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal | VSSQ | VDDQ | DQ15 | DQ14 |
| G | DQ19 | DQ18 | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal | VSSQ | VDDQ | DQ13 | DQ12 |
| H | DQS2 | DM2 | NC | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal | VSSQ | NC | DM1 | DQS1 |
| J | DQ21 | DQ20 | VDDQ | VSSQ | VSS Thermal | VSS Thermal | VSS Thermal | VSS Thermal | VSSQ | VDDQ | DQ11 | DQ10 |
| K | DQ22 | DQ23 | VDDQ | VSSQ | VSS | VSS | VSS | VSS | VSSQ | VDDQ | DQ9 | DQ8 |
| L | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | VDD | VSS | A10 | VDD | VDD | RFU ₁ | VSS | VDD | NC | NC |
| M | $\overline{\text{RAS}}$ | NC | NC | BA1 | A2 | A11 | A9 | A5 | RFU ₂ | CK | $\overline{\text{CK}}$ | MCL |
| N | $\overline{\text{CS}}$ | NC | BA0 | A0 | A1 | A3 | A4 | A6 | A7 | A8/AP | CKE | VREF |

NOTE:

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. VSS Thermal balls are optional

PIN DESCRIPTION

| | | | |
|----------------------------|--------------------------|------------|---------------------|
| CK, $\overline{\text{CK}}$ | Differential Clock Input | BA0, BA1 | Bank Select Address |
| CKE | Clock Enable | A0 ~ A11 | Address Input |
| $\overline{\text{CS}}$ | Chip Select | DQ0 ~ DQ31 | Data Input/Output |
| $\overline{\text{RAS}}$ | Row Address Strobe | VDD | Power |
| $\overline{\text{CAS}}$ | Column Address Strobe | VSS | Ground |
| WE | Write Enable | VDDQ | Power for DQ's |
| DQS | Data Strobe | VSSQ | Ground for DQ's |
| DM | Data Mask | NC | No Connection |
| RFU | Reserved for Future Use | MCL | Must Connect Low |

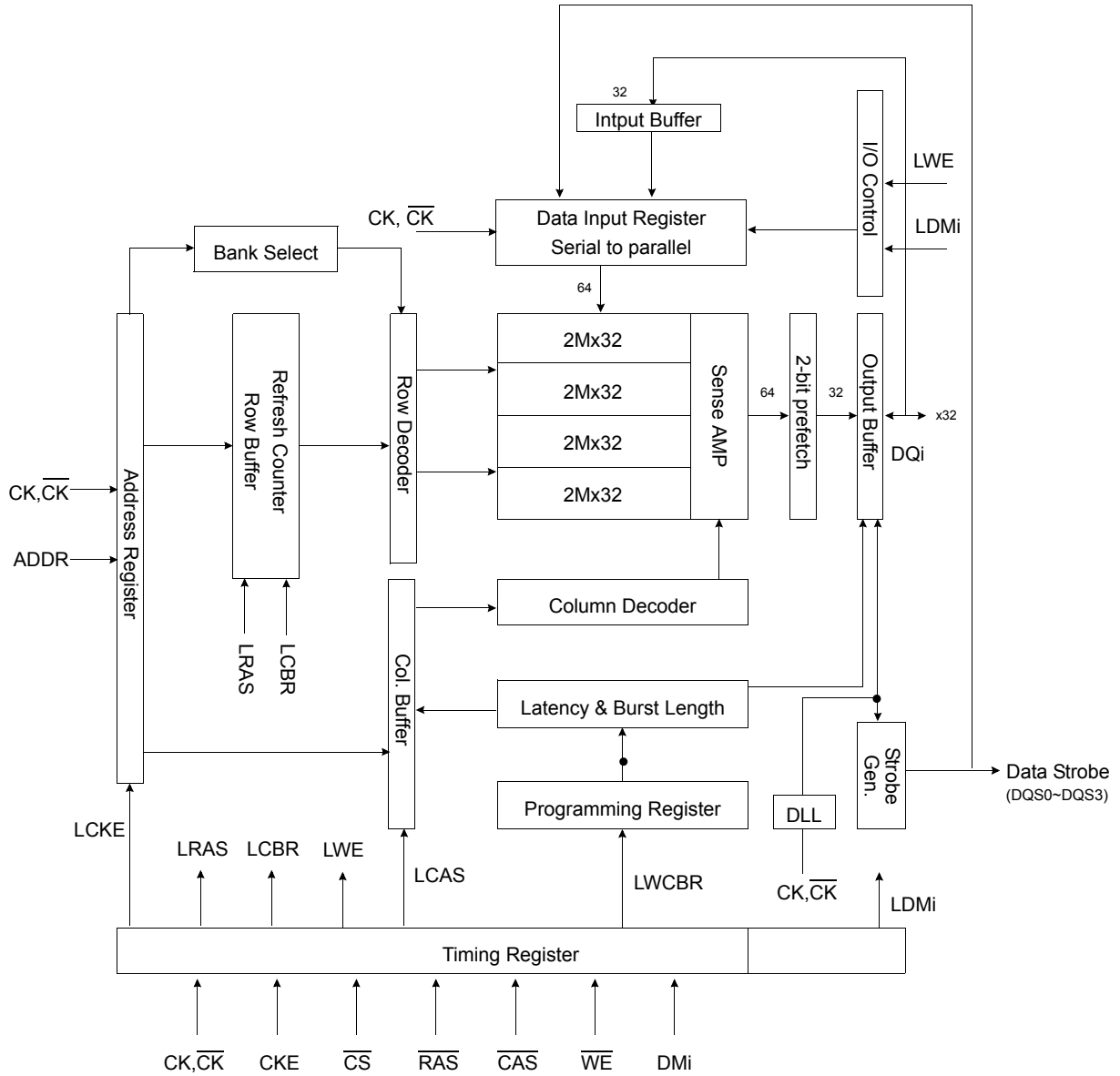
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

| Symbol | Type | Function |
|-------------------------------|---|--|
| CK, $\overline{\text{CK}}^*1$ | Input | The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS. |
| CKE | Input | Activates the CK signal when high and deactivates the $\overline{\text{CK}}$ signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode. |
| $\overline{\text{CS}}$ | Input | $\overline{\text{CS}}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{\text{RAS}}$ | Input | Latches row addresses on the positive going edge of the CK with $\overline{\text{RAS}}$ low. Enables row access & precharge. |
| $\overline{\text{CAS}}$ | Input | Latches column addresses on the positive going edge of the CK with $\overline{\text{CAS}}$ low. Enables column access. |
| $\overline{\text{WE}}$ | Input | Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active. |
| DQS0 ~ DQS3 | Input/Output | Data input and output are synchronized with both edge of DQS. DQS0 for DQ0 ~ DQ7, DQS1 for DQ8 ~ DQ15, DQS2 for DQ16 ~ DQ23, DQS3 for DQ24 ~ DQ31. |
| DM0 ~ DM3 | Input | Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM0 for DQ0 ~ DQ7, DM1 for DQ8 ~ DQ15, DM2 for DQ16 ~ DQ23, DM3 for DQ24 ~ DQ31. |
| DQ0 ~ DQ31 | Input/Output | Data inputs/Outputs are multiplexed on the same pins. |
| BA0, BA1 | Input | Selects which bank is to be active. |
| A0 ~ A11 | Input | Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7, CA9 Column address CA8 is used for auto precharge. |
| VDD/VSS | Power Supply | Power and ground for the input buffers and core logic. |
| VDDQ/VSSQ | Power Supply | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| VREF | Power Supply | Reference voltage for inputs, used for SSTL interface. |
| NC/RFU | No connection/ Reserved for future use | This pin is recommended to be left "No connection" on the device |
| MCL | Must Connect Low | Must connect low |

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{\text{CK}}$.

For any applications using the single ended clocking, apply VREF to $\overline{\text{CK}}$ pin.

BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



FUNCTIONAL DESCRIPTION

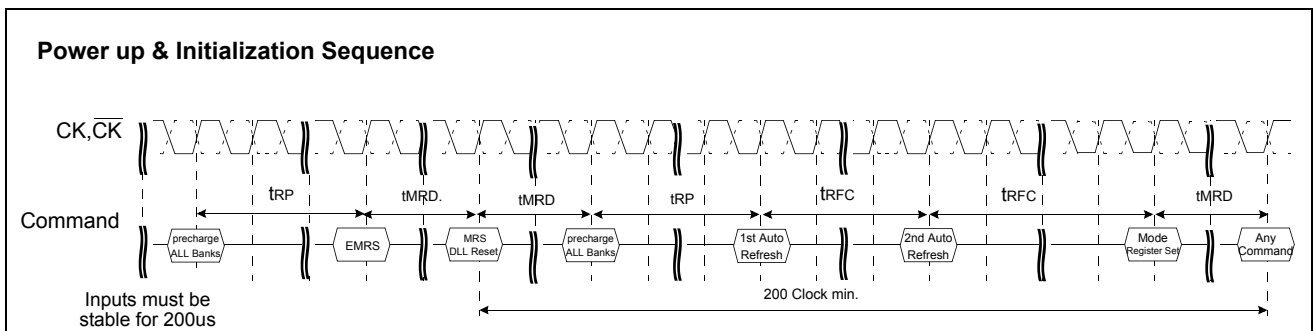
• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
 - Apply VDD before VDDQ .
 - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,CK $\bar{}$), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- *1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- *1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

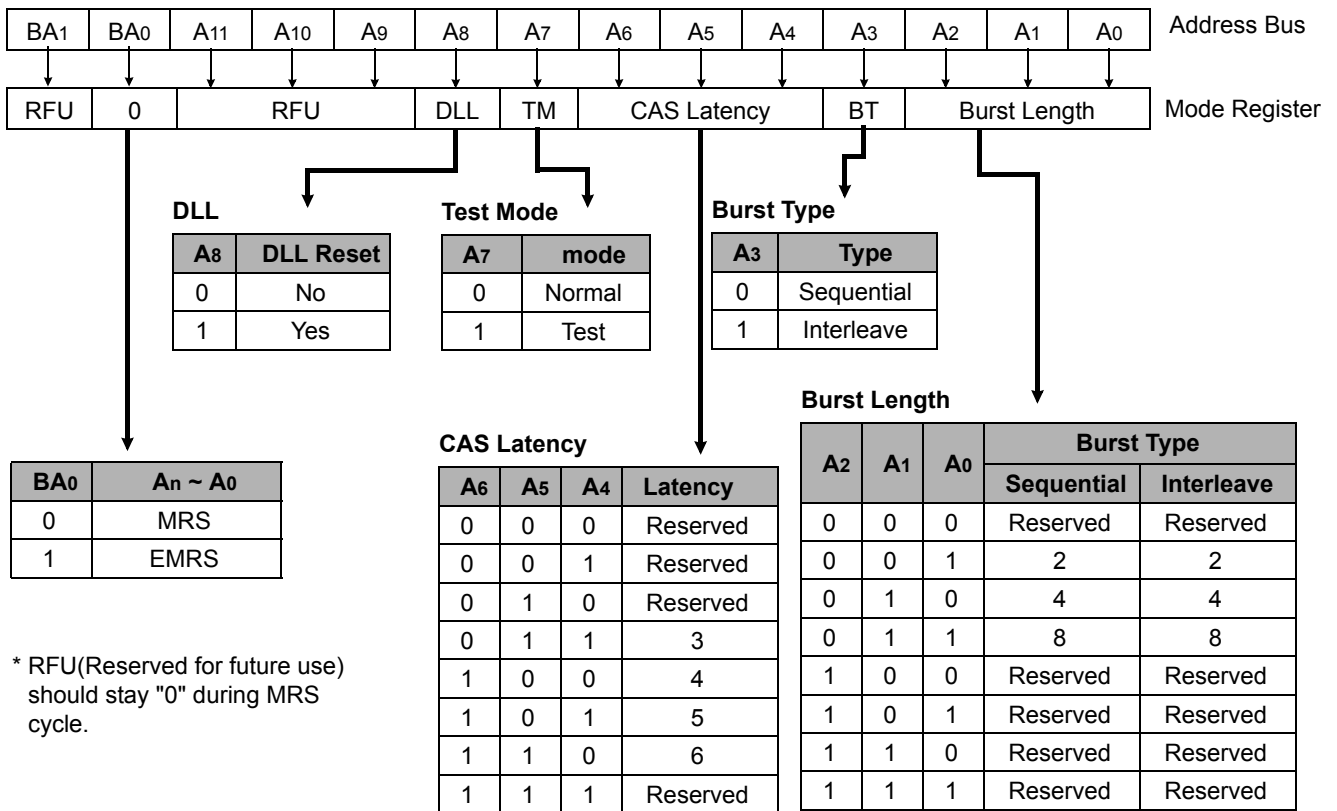
*2 Sequence of 6&7 is regardless of the order



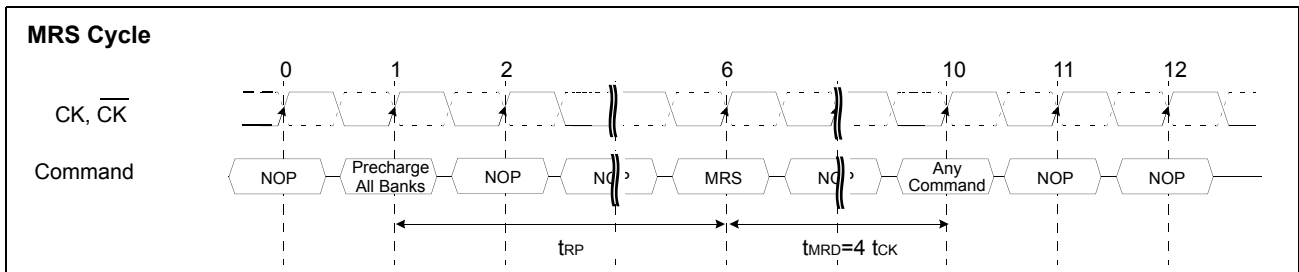
*** When the operating frequency is changed, DLL reset should be required again.
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.**

MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE (The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7,A8, BA0 and BA1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



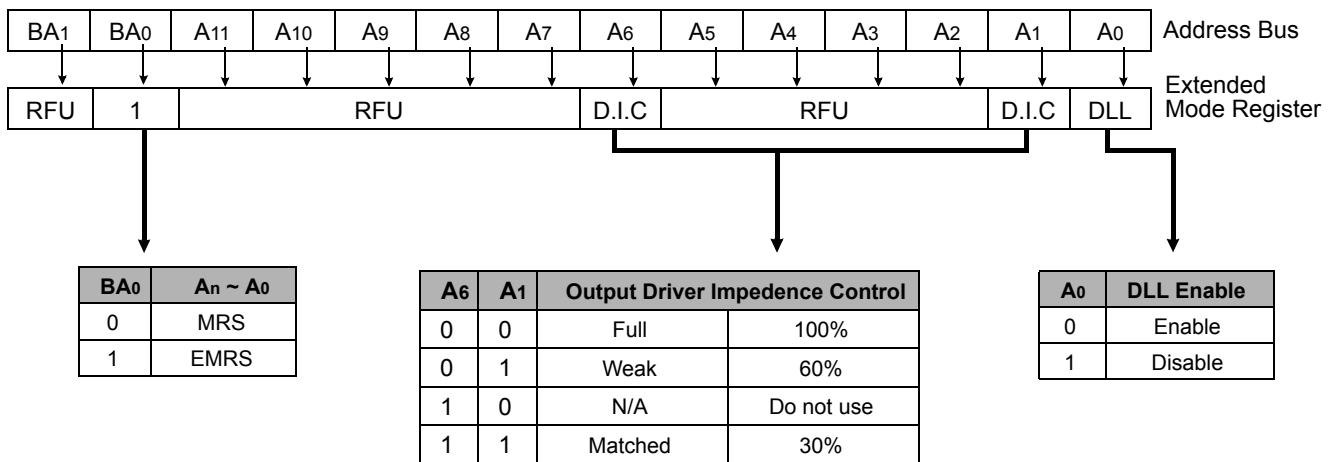
* RFU(Reserved for future use) should stay "0" during MRS cycle.



*1 : MRS can be issued only at all banks precharge state.
 *2 : Minimum trp is required to issue MRS command.

EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

Figure 7. Extended Mode Register set

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -0.5 ~ 3.6 | V |
| Voltage on VDD supply relative to Vss | VDD | -1.0 ~ 3.6 | V |
| Voltage on VDD supply relative to Vss | VDDQ | -0.5 ~ 3.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Power dissipation | P _D | 3.3 | W |
| Short circuit current | I _{OS} | 50 | mA |

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, T_A=0 to 65°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|---------------------|-----------------------|------|-----------------------|------|-----------------------------|
| Device Supply voltage | VDD | 1.7 | 1.8 | 1.9 | V | 1 |
| Output Supply voltage | VDDQ | 1.7 | 1.8 | 1.9 | V | 1 |
| Reference voltage | VREF | 0.49*VDDQ | - | 0.51*VDDQ | V | 2 |
| Termination voltage | V _{tt} | VREF-0.04 | VREF | VREF+0.04 | V | 3 |
| Input logic high voltage | V _{IH(DC)} | VREF+0.15 | - | VDDQ+0.30 | V | 4 |
| Input logic low voltage | V _{IL(DC)} | -0.30 | - | VREF-0.15 | V | 5 |
| Output logic high voltage | V _{OH} | V _{tt} +0.76 | - | - | V | I _{OH} =-15.2mA, 7 |
| Output logic low voltage | V _{OL} | - | - | V _{tt} -0.76 | V | I _{OL} =+15.2mA, 7 |
| Input leakage current | I _{IL} | -5 | - | 5 | uA | 6 |
| Output leakage current | I _{OL} | -5 | - | 5 | uA | 6 |

- Note** : 1. Under all conditions VDDQ must be less than or equal to VDD.
 2. VREF is expected to equal 0.50*VDDQ of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the VREF may not exceed + 2% of the DC value.
 3. V_{tt} of the transmitting device must track VREF of the receiving device.
 4. V_{IH(max.)}= VDDQ +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
 5. V_{IL(min.)}= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
 6. For any pin under test input of 0V ≤ V_{IN} ≤ VDD is acceptable. For all other pins that are not under test V_{IN}=0V.
 7. Output logic high voltage and low voltage is depend on output channel condition.

DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

| Parameter | Symbol | Test Condition | Version | | | Unit | Note |
|---|-------------------|---|---------|-----|-----|------|------|
| | | | -25 | -2A | -33 | | |
| Operating Current (One Bank Active) | I _{CC1} | Burst Length=2 t _{RC} ≥ t _{RC} (min) I _{OL} =0mA, t _{CC} = t _{CC} (min) | 270 | 242 | 238 | mA | |
| Precharge Standby Current in Power-down mode | I _{CC2P} | CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min) | 10 | 10 | 10 | mA | |
| Precharge Standby Current in Non Power-down mode | I _{CC2N} | CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), t _{CC} = t _{CC} (min) | 57 | 52 | 47 | mA | |
| Active Standby Current power-down mode | I _{CC3P} | CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min) | 60 | 55 | 48 | mA | |
| Active Standby Current in Non Power-down mode | I _{CC3N} | CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), t _{CC} = t _{CC} (min) | 201 | 183 | 164 | mA | |
| Operating Current (Burst Mode) | I _{CC4} | I _{OL} =0mA ,t _{CC} = t _{CC} (min), Page Burst, All Banks activated. | 368 | 342 | 314 | mA | |
| Refresh Current | I _{CC5} | t _{RC} ≥ t _{RFC} (min) | 314 | 286 | 274 | mA | 1 |
| Self Refresh Current | I _{CC6} | CKE ≤ 0.2V | 7 | 7 | 7 | mA | |
| Operating Current (4Bank interleaving) | I _{CC7} | Burst Length=4 t _{RC} ≥ t _{RC} (min) I _{OL} =0mA, t _{CC} = t _{CC} (min) | 615 | 533 | 479 | mA | |

Note : 1 Refresh period is 32ms**AC INPUT OPERATING CONDITIONS**Recommended operating conditions(Voltage referenced to V_{SS}=0V, TA=0 to 65°C)

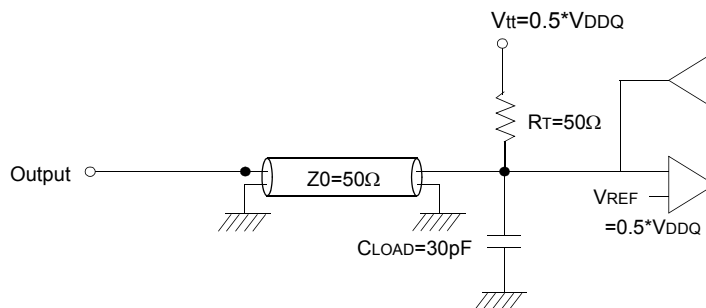
| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-----------------|---------------------------|-----|---------------------------|------|------|
| Input High (Logic 1) Voltage ;DQ | V _{IH} | V _{REF} +0.35 | - | - | V | |
| Input Low (Logic 0) Voltage; DQ | V _{IL} | - | - | V _{REF} -0.35 | V | |
| Clock Input Differential Voltage; CK and \overline{CK} | V _{ID} | 0.7 | - | V _{DDQ} +0.6 | V | 1 |
| Clock Input Crossing Point Voltage; CK and \overline{CK} | V _{IX} | 0.5*V _{DDQ} -0.2 | - | 0.5*V _{DDQ} +0.2 | V | 2 |

Note : 1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same

AC OPERATING TEST CONDITIONS (TA= 0 to 65°C)

| Parameter | Value | Unit | Note |
|--|-------------------|------|------|
| Input reference voltage for CK(for single ended) | 0.50*VDDQ | V | 1 |
| CK and \overline{CK} signal maximum peak swing | 1.5 | V | |
| CK signal minimum slew rate | 1.0 | V/ns | |
| Input Levels(VIH/VIL) | VREF+0.4/VREF-0.4 | V | |
| Input timing measurement reference level | VREF | V | |
| Output timing measurement reference level | Vtt | V | |
| Output load condition | See Fig.1 | | |

Note 1 : In case of differential clocks(CK and \overline{CK}), input reference voltage for clock is a CK and \overline{CK} 's crossing point.



(Fig. 1) Output Load Circuit

CAPACITANCE (TA= 25°C, f=1MHz)

| Parameter | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Input capacitance(CK, \overline{CK}) | CIN1 | 1.0 | 5.0 | pF |
| Input capacitance(A0~A11, BA0~BA1) | CIN2 | 1.0 | 4.0 | pF |
| Input capacitance (CKE, CS, RAS, CAS, WE) | CIN3 | 1.0 | 4.0 | pF |
| Data & DQS input/output capacitance(DQ0~DQ31) | COUT | 1.0 | 6.5 | pF |
| Input capacitance(DM0 ~ DM3) | CIN4 | 1.0 | 6.5 | pF |

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

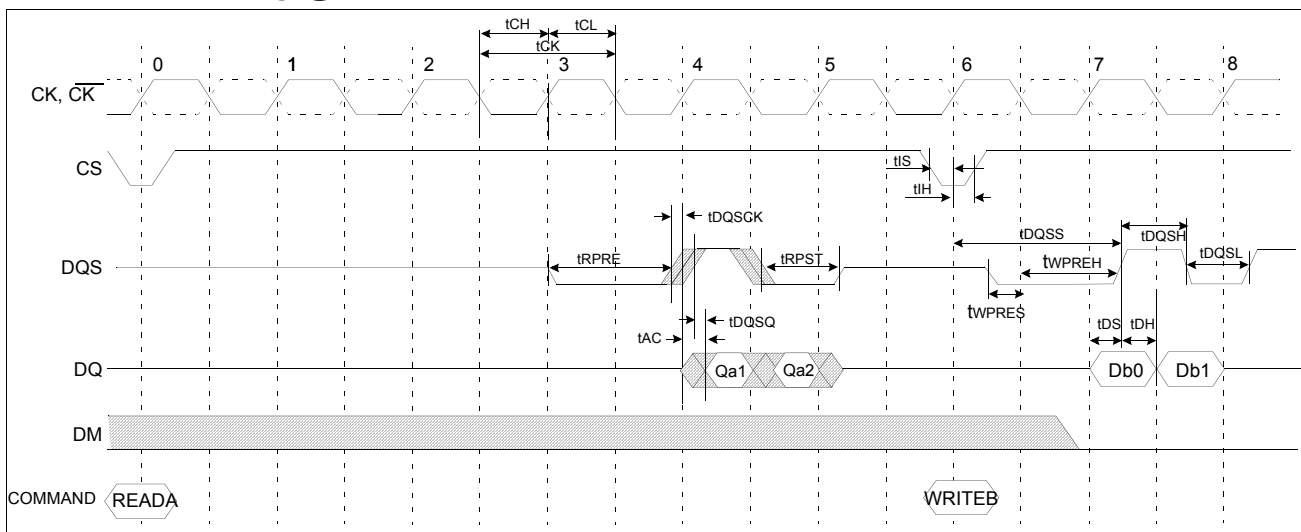
| Parameter | Symbol | Value | Unit |
|--|--------|------------|------|
| Decoupling Capacitance between VDD and Vss | CDC1 | 0.1 + 0.01 | uF |
| Decoupling Capacitance between VDDQ and VSSQ | CDC2 | 0.1 + 0.01 | uF |

Note : 1. VDD and VDDQ pins are separated each other.
 All VDD pins are connected in chip. All VDDQ pins are connected in chip.
 2. Vss and VSSQ pins are separated each other
 All Vss pins are connected in chip. All VSSQ pins are connected in chip.

AC CHARACTERISTICS (I)

| Parameter | Symbol | -25 | | -2A | | -33 | | Unit | Note | |
|---------------------------------|--------|------------------------|------|------------------------|------|------------------------|------|------|------|--|
| | | Min | Max | Min | Max | Min | Max | | | |
| CK cycle time | tCK | CL=3 | - | 10.0 | - | 10.0 | 5 | 10.0 | ns | |
| | | CL=4 | - | | - | | 3.3 | | ns | |
| | | CL=5 | 2.5 | | 2.86 | | - | | ns | |
| | | CL=6 | - | | - | | - | | ns | |
| CK high level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | | |
| CK low level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | | |
| DQS out access time from CK | tDQSCK | -0.45 | 0.45 | -0.55 | 0.55 | -0.55 | 0.55 | ns | | |
| Output access time from CK | tAC | -0.45 | 0.45 | -0.55 | 0.55 | -0.55 | 0.55 | ns | | |
| Data strobe edge to Dout edge | tDQSQ | - | 0.28 | - | 0.35 | - | 0.35 | ns | 1 | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | | |
| CK to valid DQS-in | tDQSS | 0.85 | 1.15 | 0.85 | 1.15 | 0.85 | 1.15 | tCK | | |
| DQS-In setup time | tWPRES | 0 | - | 0 | - | 0 | - | ns | | |
| DQS-in hold time | tWPREH | 0.35 | - | 0.35 | - | 0.35 | - | tCK | | |
| DQS write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | | |
| DQS-In high level width | tDQSH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | | |
| DQS-In low level width | tDQSL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | | |
| Address and Control input setup | tIS | 0.6 | - | 0.8 | - | 0.8 | - | ns | | |
| Address and Control input hold | tIH | 0.6 | - | 0.8 | - | 0.8 | - | ns | | |
| DQ and DM setup time to DQS | tDS | 0.3 | - | 0.35 | - | 0.35 | - | ns | | |
| DQ and DM hold time to DQS | tDH | 0.3 | - | 0.35 | - | 0.35 | - | ns | | |
| Clock half period | tHP | tCLmin or tCHmin | - | tCLmin or tCHmin | - | tCLmin or tCHmin | - | ns | 1 | |
| Data Hold skew factor | tQHS | - | 0.4 | - | 0.4 | - | 0.4 | ns | | |
| Data output hold time from DQS | tQH | tHP- tQHS | - | tHP- tQHS | - | tHP- tQHS | - | ns | 1 | |

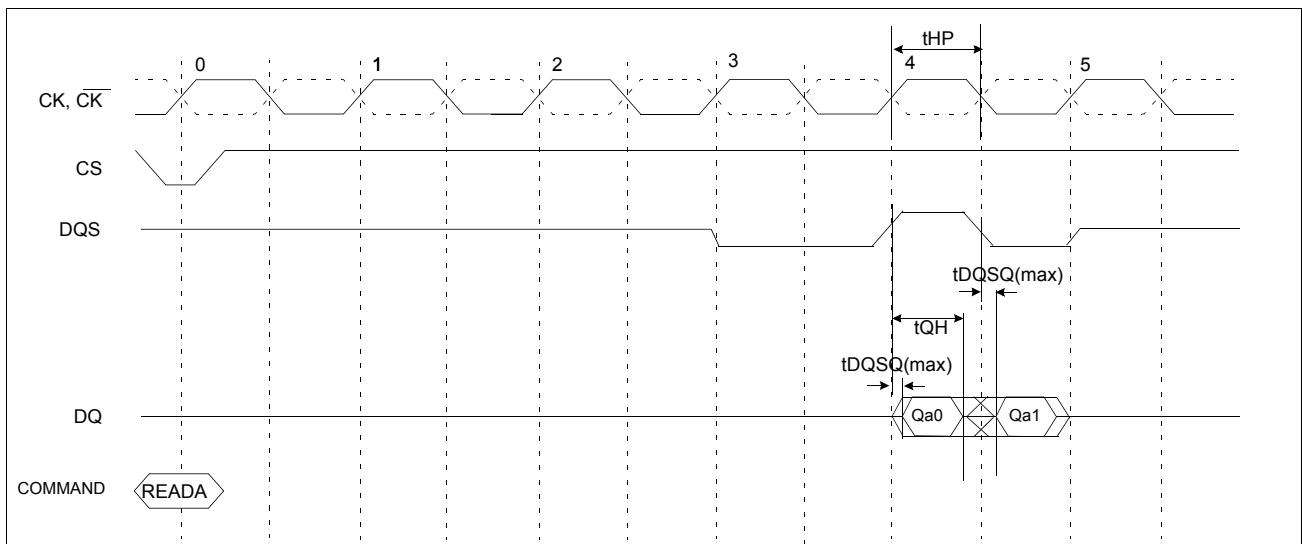
Simplified Timing @ BL=2, CL=4



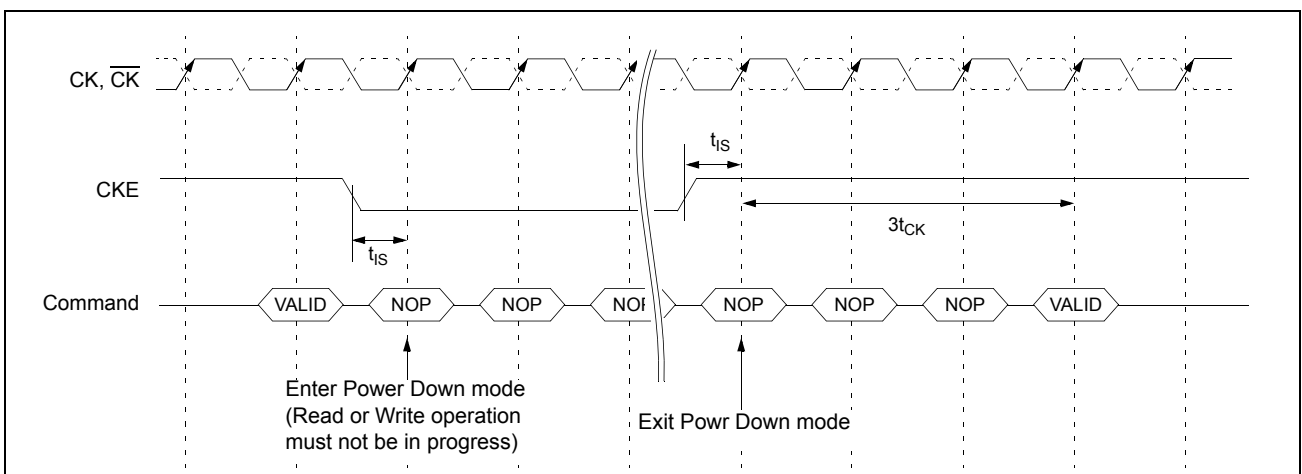
Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(t_{DV}) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of $t_{DV}(=0.35t_{CK})$ artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, t_{QH} which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces t_{DV}
- $t_{QHmin} = t_{HP}-X$ where
 - . t_{HP} =Minimum half clock period for any given cycle and is defined by clock high or clock low time(t_{CH},t_{CL})
 - . X =A frequency dependent timing allowance account for $t_{DQSQmax}$

t_{QH} Timing (CL4, BL2)



Power Down Timing



AC CHARACTERISTICS (II)

| Parameter | Symbol | -25 | | -2A | | -33 | | Unit | Note |
|---|--------|--------------|------|--------------|------|--------------|------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Row cycle time | tRC | 45 | - | 45.8 | - | 49.5 | - | ns | 2,5 |
| Refresh row cycle time | tRFC | 50 | - | 51.5 | - | 56.1 | - | ns | 5 |
| Row active time | tRAS | 28.6 | 100K | 28.6 | 100K | 33 | 100K | ns | 5 |
| RAS to CAS delay for Read | tRCDRD | 15 | - | 16.5 | - | 16.5 | - | ns | 5 |
| RAS to CAS delay for Write | tRCDWR | 10 | - | 11.4 | - | 11.4 | - | ns | 4,5 |
| Row precharge time | tRP | 15 | - | 16.5 | - | 16.5 | - | ns | 5 |
| Last data in to Row precharge @Normal Precharge | tWR | 15 | - | 16.5 | - | 16.5 | - | ns | 1,5 |
| Last data in to Row precharge @Auto Precharge | tWR_A | 6 | - | 6 | - | 5 | - | tCK | 1,3 |
| Auto precharge write recovery + Precharge | tDAL | 30 | - | 33 | - | 33 | - | ns | 3,5 |
| Row active to Row active | tRRD | 4 | - | 4 | - | 3 | - | tCK | |
| Last data in to Read command | tCDLR | 2 | - | 2 | - | 2 | - | tCK | 1 |
| Col. address to Col. address | tCCD | 1 | - | 1 | - | 1 | - | tCK | |
| Mode register set cycle time | tMRD | 4 | - | 3 | - | 3 | - | tCK | |
| Exit self refresh to read command | tXSR | 200 | - | 200 | - | 200 | - | tCK | |
| Power down exit time | tPDEX | 3tCK+ tIS | - | 3tCK+ tIS | - | 3tCK+ tIS | - | ns | |
| Refresh interval time | tREF | 7.8 | - | 7.8 | - | 7.8 | - | us | |

- Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM
 2. The number of clock of tRC is restricted by the number of clock of tRAS and tRP
 3. The number of clock of tWR_A is fixed. It can't be changed by tCK. tWR_A is related with CL. It is equal to CL+1tCK.
 4. tRCDWR is equal to tRCDRD-2tCK and the number of clock can not be lower than 2tCK.
 5. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer unconditionally.

AC CHARACTERISTICS (II)

(Unit : Number of Clock)

K4D553235F-GC25

| Frequency | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 400MHz (2.5ns) | 5 | 18 | 20 | 12 | 6 | 4 | 6 | 4 | 12 | tCK |

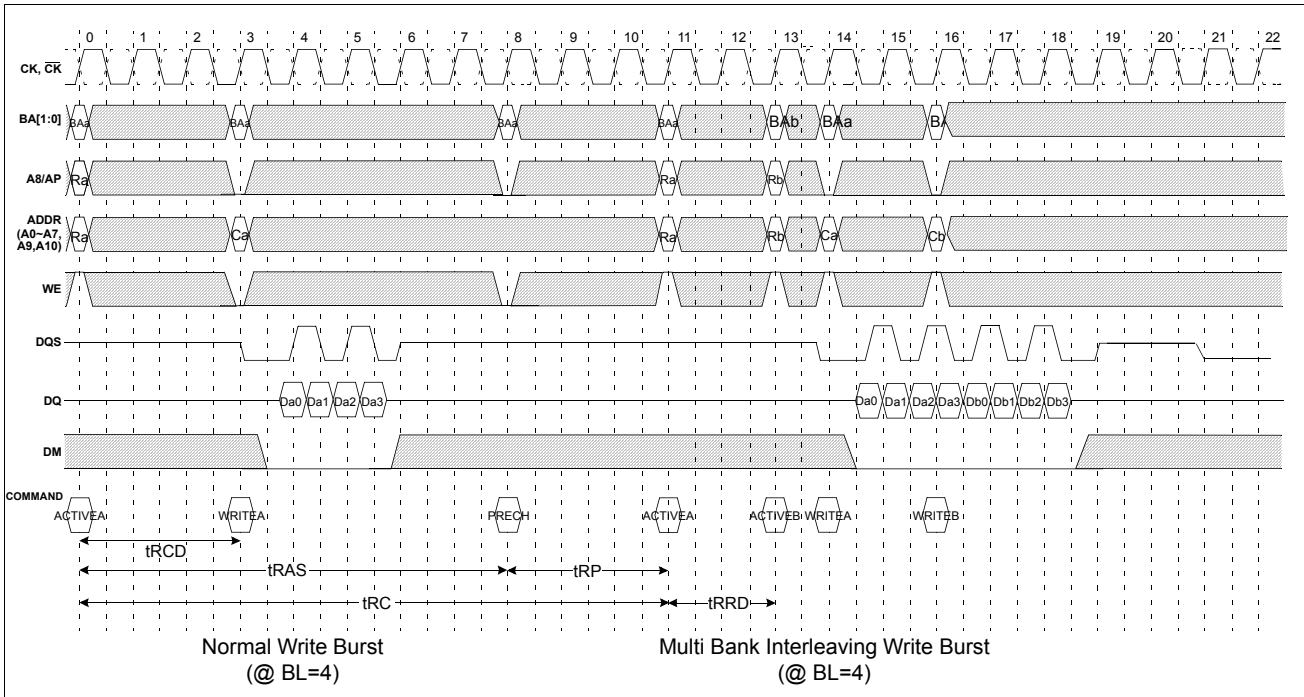
K4D553235F-GC2A

| Frequency | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|-------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 350MHz (2.86ns) | 5 | 16 | 18 | 10 | 6 | 4 | 6 | 4 | 12 | tCK |
| 300MHz (3.3ns) | 4 | 15 | 17 | 10 | 5 | 3 | 5 | 3 | 10 | tCK |

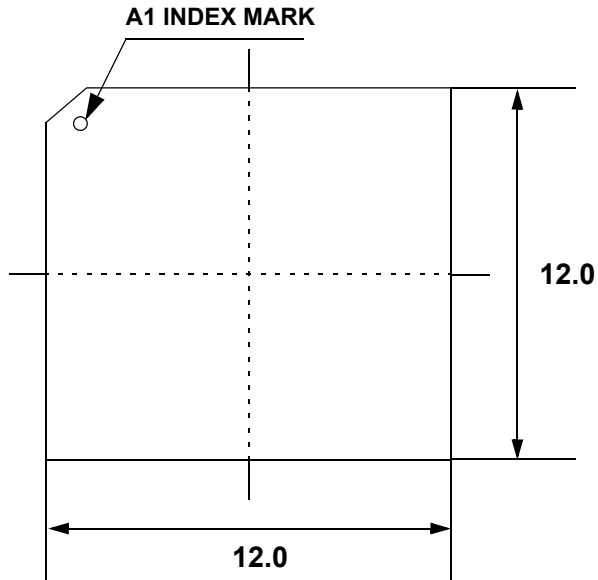
K4D553235F-GC33

| Frequency | Cas Latency | tRC | tRFC | tRAS | tRCDRD | tRCDWR | tRP | tRRD | tDAL | Unit |
|------------------|-------------|-----|------|------|--------|--------|-----|------|------|------|
| 300MHz (3.3ns) | 4 | 15 | 17 | 10 | 5 | 3 | 5 | 3 | 10 | tCK |

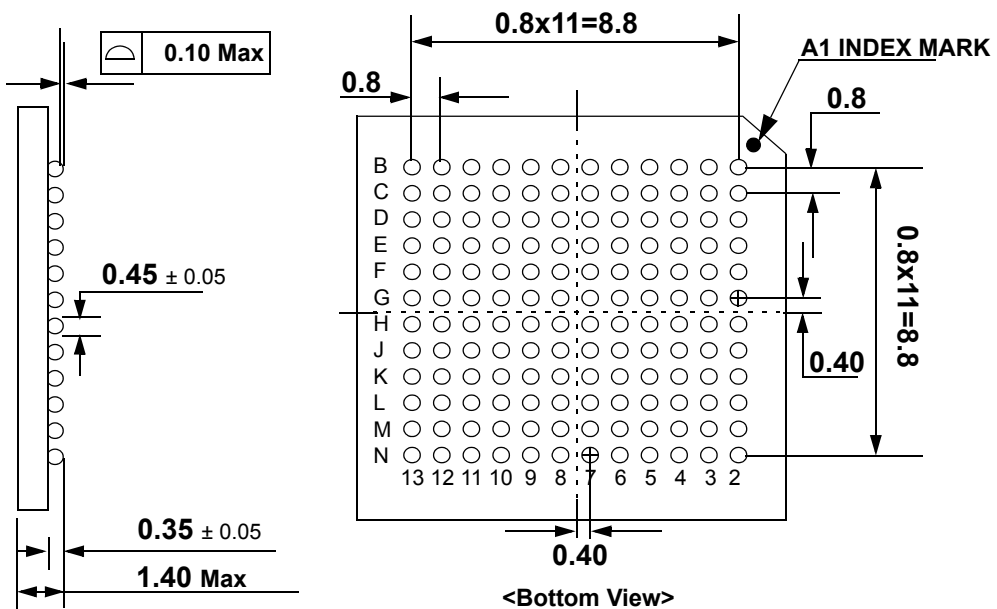
Simplified Timing(2) @ BL=4



PACKAGE DIMENSIONS (144-Ball FBGA)



<Top View>



<Bottom View>

Unit : mm