Preliminary

MHS

MATRA M H S

January 1991

DATA SHEET

M-65864

8,192 x 8 STATIC RAM

FEATURES

- BICMOS FOR OPTIMUM SPEED/POWER
- HIGH SPEED
  – 12 ns
- LOW ACTIVE POWER
  – 600 mW
- LOW STANDBY POWER
  – 200 mW
- TTL-COMPATIBLE INPUTS AND OUTPUTS
- CAPABLE OF WITHSTANDING GREATER THAN 2001V ELECTROSTATIC DISCHARGE

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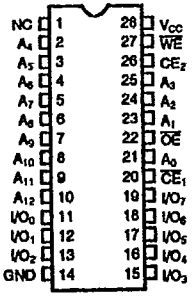
DESCRIPTION

The M-65864 is a high-performance BiCMOS static RAM organized as 8,192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have a power-down feature ($\overline{CE_1}$) that reduces the power consumption by 67 % when deselected. An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE_1}$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

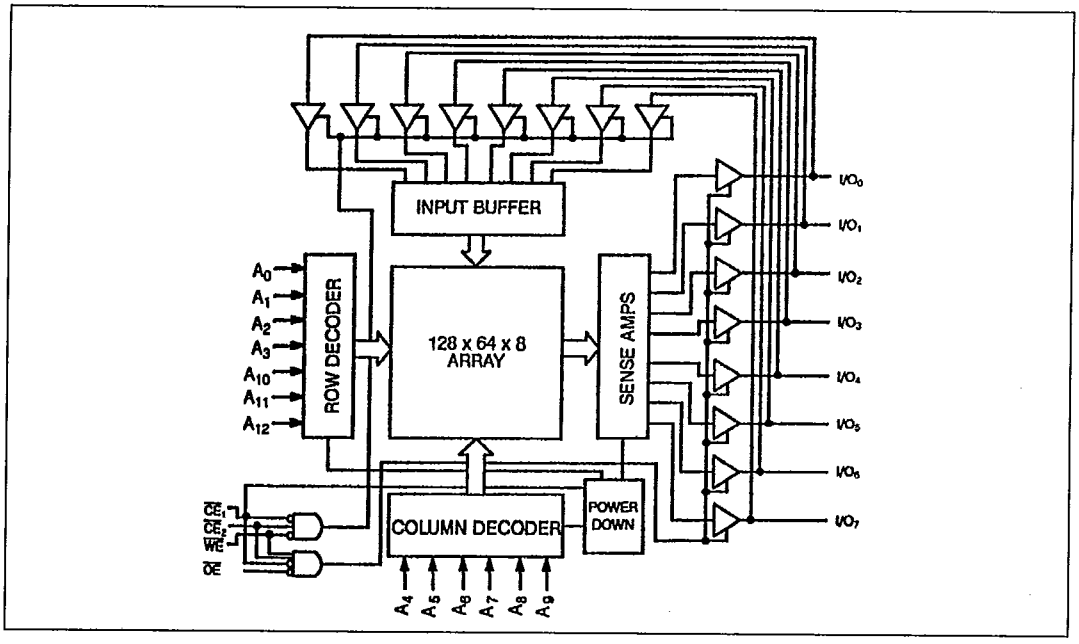
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

PACKAGES

DIP / SOJ
Top view



BLOCK DIAGRAM



SELECTION GUIDE

		M-65864-12	M-65864-15
Maximum Access Time (ns)		12	15
Maximum Operating Current (mA)	Commercial	140	135
	Military		145
Maximun Standby Current (mA)	Commercial	40	40
	Military		50

MAXIMUM RATING

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested)

Storage Temperature ..... – 65°C to + 150°C
Ambient Temperature with Power Applied ..... – 55°C to + 125°C
Supply Voltage to Ground Potential ..... – 0. 5V to + 7. 0V
DC Voltage Applied to Outputs in High Z State ..... – 0.5 V to + 7.0 V
DC Input Voltage[1] ..... – 3.0 V to + 7.0 V
Output Current into Outputs (Low) ... 20 mA
Static Discharge Voltage ..... > 2001 V (per MIL-STD-883, Method 3015)
Latch-up Current ..... > 200 mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5 V ± 10 %
Military [2]	– 55°C to + 125°C	5 V ± 10 %

ELECTRICAL CHARACTERISTICS over the operating range

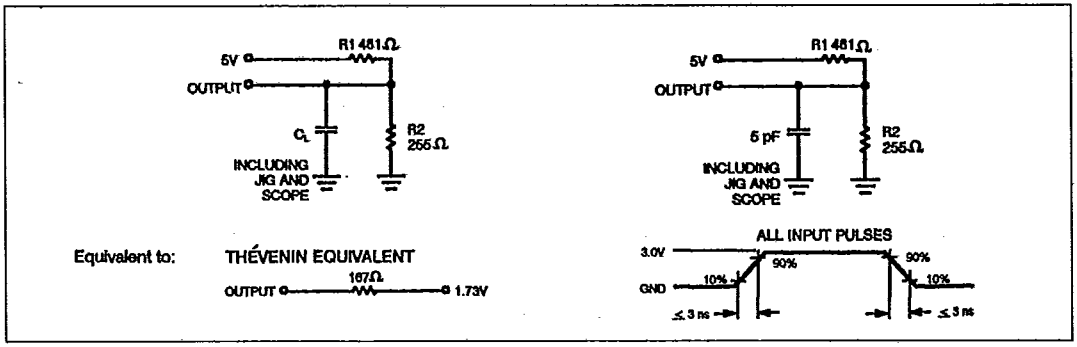
PARAMETERS	DESCRIPTION	TEST CONDITIONS			M-65864-12		M-65864-15		UNITS
					MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = – 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = – 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]				– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			– 10	+ 10	– 10	+ 10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		140		135	mA
				Mil				145	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ V_{IH}		Com'l		40		40	mA
				Mil				50	mA

CAPACITANCE [3]

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX.[4]	UNITS
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0 V	7	pF

Notes : 1. V_{IL}(min) = – 3.0 V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. Tested initially and after any design on process changes that may affect these parameters.
4. For all packages except CERDIP, which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC TEST LOADS AND WAVEFORMS



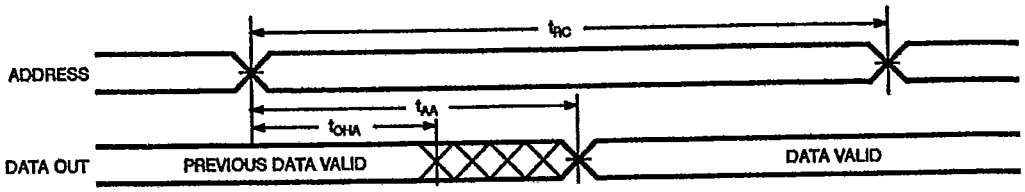
SWITCHING CHARACTERITICS Over the Operating Range [5]

PARAMETERS	DESCRIPTION	M-65864-12		M-65864-15		UNITS
		MIN.	MAX.	MIN.	MAX.	
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		12		15	ns
t_{AE2}	$\overline{CE}_2$ HIGH to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [6]		8		8	ns
t_{LZCE1}	$\overline{CE}_1$ to Low Z [7]	3		3		ns
t_{LZCE2}	$\overline{CE}_2$ HIGH to Low Z [7]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z [5, 6] $\overline{CE}_2$ LOW to High Z		7		8	ns
WRITE CYCLE [8]						
t_{WC}	Write cycle Time	12		15		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		10		ns
t_{SCE2}	$\overline{CE}_2$ HIGH to Write End	8		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold From Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6.5		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5]		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		ns

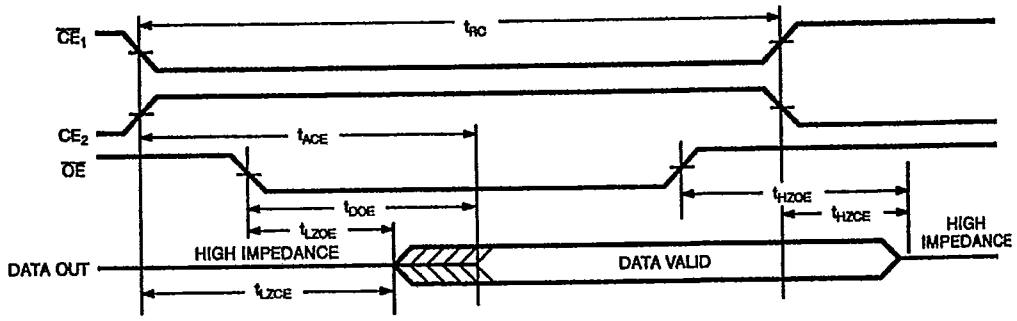
Notes :
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test loads. Transition is measured ± 200 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of CE_1 LOW, CE_2 HIGH, and WE LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

SWITCHING WAVEFORMS

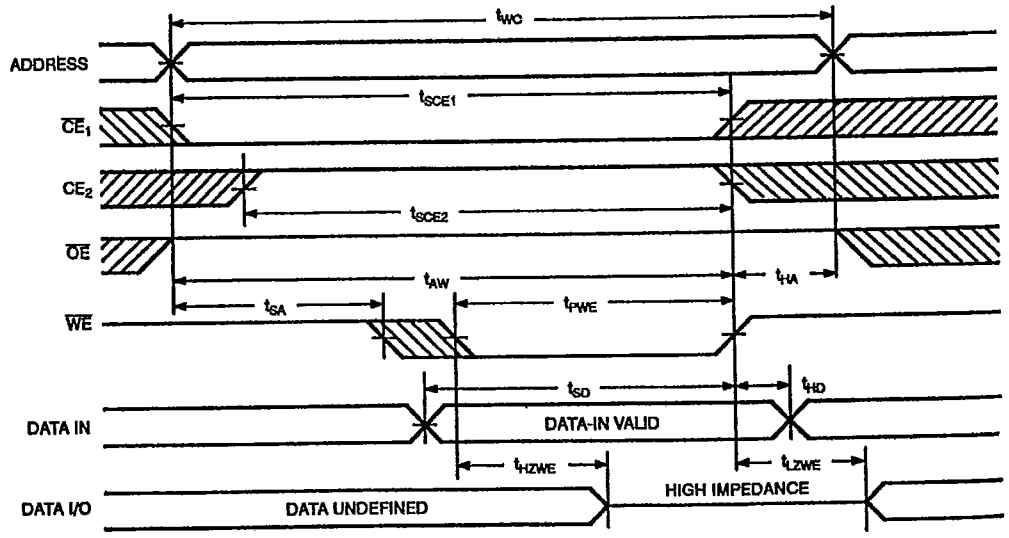
READ CYCLE N°. 1 (9, 10)



READ CYCLE N°. 2 (9, 11)



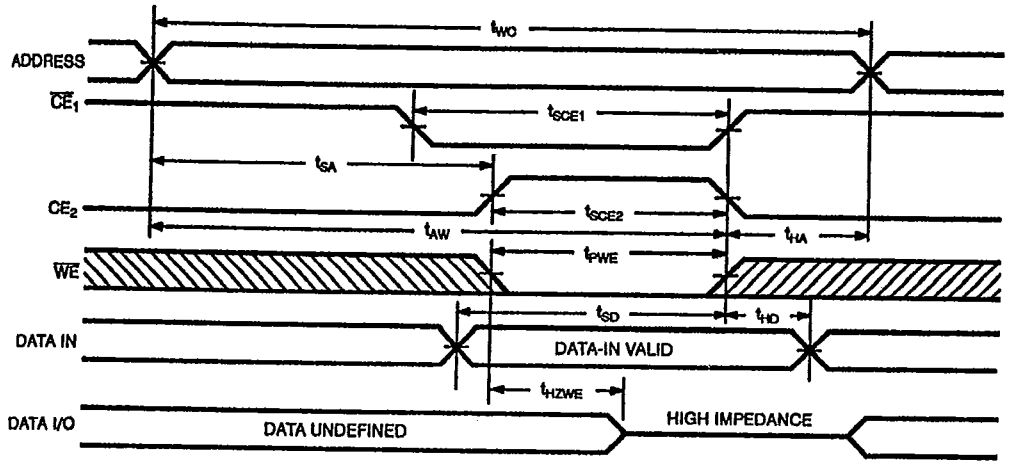
WRITE CYCLE N° 1 (WE Controlled) (7, 12)



Notes :
9. Device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$. $CE_2 = V_{IH}$.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. $\overline{WE}$ is HIGH for read cycle.
12. Data I/O is HIGH impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

SWITCHING WAVEFORMS (continued)

WRITE CYCLE N° 2 ($\overline{CE}$ controlled) (7, 11, 13)



Notes : 9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE} = V_{IL}$ (65889 $\overline{OE} = V_{IL}$ also).
11. Address valid prior to or coincident with $\overline{CE}$ transition low.
12. 65889 only : Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remain in a high-impedance state.

TRUTH TABLE

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	INPUTS/ OUTPUTS	MODE
H	X	X	X	High Z	Deselect/ Power-Down
L	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselec

ORDERING INFORMATION

	M	1	65864	12
	MHS	0 : chip form 1 : ceramic 3 : Plastic Dil U : SOJ	Device Type	Speed 12 : 12 ns 15 : 15 ns

Blank : Commercial
M : Military