S3501/S3501A, S3502/S3502A

SINGLE CHANNEL μ-LAW PCM CODEC/FILTER SET

Features

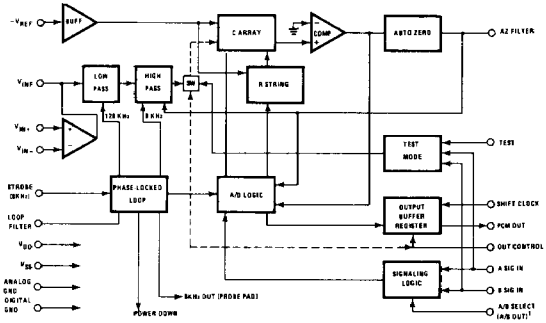
- ☐ CMOS Process for Low Power Dissipation
- ☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
- ☐ Meets or Exceeds AT&T D3 and CCITT G. 711 and G. 733 Specifications
- ☐ On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- ☐ Low Absolute Group and Relative Delay Distortion
- ☐ Single Negative Polarity Voltage Reference Input
- ☐ Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- ☐ Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- ☐ Programmable Gain Input/Output Amplifier Stages
- ☐ CCIS* Compatible A/B Signaling Option—S3501A/S3502A

General Description

The S3501 and S3502 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is typically performed at 1.544Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.

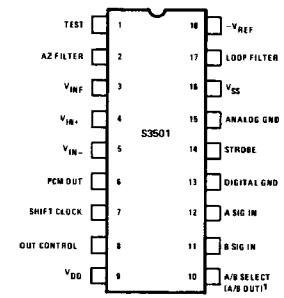
Common Channel Interoffice Signaling

S3501 Block Diagram Encoder with Filter



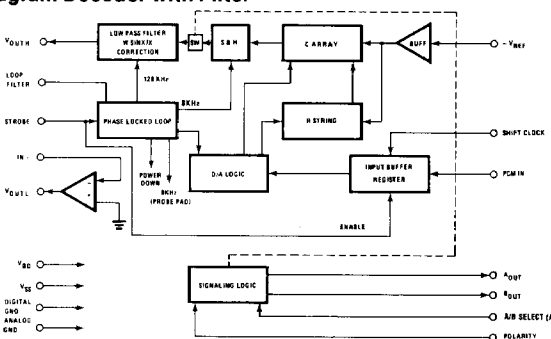
1 CCIS A/B SIGNALING OPTION

Pin Configuration



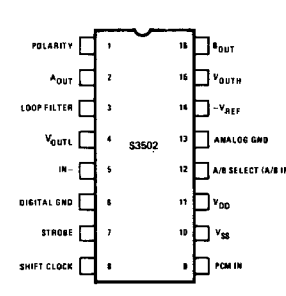
1 CCIS A/B SIGNALING OPTION-S3501A

S3502 Block Diagram Decoder with Filter



CCIS A/B SIGNALING OPTION

Pin Configuration



1 CCIS A/B SIGNALING OPTION-S3502A

S3501 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \le V_{IN} \le V_{DD} + 0.3$
Analog Input	$-V_{REF} \le V_{IN} \le V_{REF}$
$-V_{REF}$	$V_{SS} \le V_{REF} \le 0$

S3501 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 7
V−	Negative Suppply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.10	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3501 AC Characteristics (Refer to Figures 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_d (On)	Shift Clock to PCM Out (On) Delay		140	170	ns	1kΩ, 50pF
t_d (Off)	Shift Clock to PCM Out (Off) Delay		140	170	ns	
t_{rd}	PCM Output Rise Time $C_L = 50pF$		100	125	ns	1kΩ Pull-Up on PCM Out selected for desired rise time
t_{fd}	PCM Output Fall Time $C_L = 50pF$		50	70	ns	
t_{dss}	A/B Select to Strobe Trailing Set Up Time	100			ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P−P Jitter of Strobe Rising Edge			5	μs	

S3501 Encoder DC Characteristics (5V Power Supply, $-V_{REF}=-3.0V$ see Figure 9.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance	10			MΩ	V_{IN-}, V_{IN+} Inputs
C_{IN}	Input Capacitance			10	pF	V_{IN-}, V_{IN+},V_{INF} Inputs
I_{INL}	Logic Input Low Current (Shift Clock, Strobe)			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input High Current			1	μA	$V_{IH}=2.0V$
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.8	V	$I_{OL}=5mA$
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.8	V	$I_{OL}=.1mA$
I_{OH}	PCM Output Off Leakage Current			1	μA	$V_O=0$ to 5V

S3501 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input= (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	39		dB	−25
	35	38		dB	−30
	32	35		dB	−35
	29	32		dB	−40
	25	28		dB	−45
Gain Tracking		0±.02	±0.25	dB	−10
		0±0.02	±0.25	dB	−20
		0±0.03	±0.25	dB	−25
		0±0.03	±0.25	dB	−30
		−.02±0.04	±0.25	dB	−35
		−.02±0.06	±0.50	dB	−40
		−.02±0.09	±0.50	dB	−45
		−.02±0.13	±0.50	dB	−50
Idle Channel Noise		12.5	19	dBrncO	Analog Input to Analog GND
Transmission Level Point		5.4		dBm	

S3502 AC Characteristics (Refer to Figures 1 and 6)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{rd}	PCM Input Rise Time			100	ns	
t_{fd}	PCM Input Fall Time			100	ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P—P Jitter of Strobe Rising Edge			5	μs	
t_s	PCM Input Setup Time	100			ns	
$t_{A/BS}$	A/B Select Set Up Time to Strobe Trailing Edge	100			ns	
t_{AO}, t_{BO}	Strobe Falling Edge to A/B Out Delay			200	ns	

S3502 Decoder DC Characteristics 5V Power Supplies, $-V_{REF} = -3.0V$ (see Figure 11.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_L(V_{OUTL})$	Output Load Resistance	600			Ω	
R_{INA}(IN−)	Analog Input Resistance	10			MΩ	
C_{INA}(IN−)	Analog Input Capacitance			10	pF	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{IL}	Logic Input (Shift Clock, Strobe, PCM In) "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{INL}	Logic Input "Low" Current			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input "High" Current			1	μA	$V_{IH}=2.0V$
V_{OL}	A, B Output "Low" Voltage			0.8	V	Polarity=Dig. Gnd, $I_{OL}=1mA$
V_{OL}	A, B Output "Low" Voltage			$V_{SS}+1.0$	V	Polarity=V_{SS}; $I_{OL}=1mA$

S3502 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input = (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	38.5		dB	−25
	35	39		dB	−30
	32	36.5		dB	−35
	29	33.5		dB	−40
	25	29		dB	−45
Gain Tracking		.02±.02	±0.25	dB	−10
		.04±.02	±0.25	dB	−20
		.04±.03	±0.25	dB	−25
		.03±.03	±0.25	dB	−30
		.04±.04	±0.25	dB	−35
		.04±.05	±0.50	dB	−40
		.1±.05	±0.50	dB	−45
		.15±.07	±0.50	dB	−50
Idle Channel Noise		9	13	dBrncO	PCM Input to Analog GND
0 Transmission Level Point (Digital Milliwatt Response)		4.9		dBm	−3V V_{REF} 600Ω Load

S3501/S3502 System Characteristics Typical Group Delay Characteristic

Device	Abs. Gr. Delay μs f = 1000Hz	Abs. Gr. Delay μs f = 2600Hz	Relative Gr. Delay Distortion (Over Band of 1000 Hz to 2600Hz wrt 1000Hz) μs
Encoder Low Pass	132	220	88
Encoder High Pass	104	22	−82
Encoder Total	236	242	6
Decoder Low Pass	153	250	97
Encoder + Decoder (Total)	389	492	103
End to End Group Delay (Encoder Analog Input to Decoder Analog Output)	639	742	103

Design Considerations

Because the Codec set is required to handle signals with a very large dynamic range, optimal analog performance requires careful attention to the layout of components:

The analog ground, digital ground, V_{DD} and V_{SS} busses should run independently to the power supply, or at least to the edge connector. They should be separate for each chip and should be kept as wide as possible on the printed circuit.

The connections should be as independent as possible. For example (see Figure 7), the 750Ω pull-up resistor to Pin 6 should join the V_{DD} supply at the edge connector and not at the device pin.

Decoupling capacitors should be as close as possible to the power supply pin and analog ground pin.

Digital signal lines should be kept away from analog signals, and separated by an analog ground line where possible for shielding.