1/4-Inch SOC VGA CMOS Active-Pixel Digital Image Sensor

MT9V111I29STC

Features

- DigitalClarity™ CMOS Imaging Technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra low-power, low cost CMOS image sensor
- Superior low-light performance
- Up to 30 fps progressive scan at 27 MHz for high-quality video at VGA resolution
- On-chip Image Flow Processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, 2X fixed zoom
- Image decimation to arbitrary size with smooth, continuous zoom and pan
- Automatic exposure, white balance and black compensation, flicker avoidance, color saturation, and defect identification and correction, auto frame rate, back light compensation
- Xenon and LED-type flash support
- Two-wire serial programming interface
- ITU_R BT.656 (YCbCr), YUV, 565RGB, 555RGB, and 444RGB output data formats

Applications

- Cellular phones
- PDAs
- PC Camera
- Toys and other battery-powered products

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical Format		1/4-inch (4:3)
Active Imager Size		3.58mm(H) x 2.69mm(V) 4.48mm (Diagonal)
Active Pixels		640H x 480V (VGA)
Pixel Size		5.6um x 5.6um
Color Filter Array		RGB Bayer Pattern
Shutter Type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		12—13.5 MPS/24—27 MHz
Frame Rate	VGA (640 x 480)	15 fps at 12 MHz (default), programmable up to 30 fps at 27 MHz
	CIF (352 x 288)	Programmable up to 60 fps
	QVGA (320 x 240)	Programmable up to 90 fps
ADC Resolution		10-bit, on-chip
Responsivity		1.9 V/lux-sec (550nm)
Dynamic Range		60dB
SNR_{MAX}		45dB
Supply Voltage		2.8V $\pm$0.25V
Power Consumption		<80mW at 2.8V, 15 fps at 12MHz
Operating Temperature		-20°C to +60°C
Packaging		44-Ball ICSP, wafer or die

General Description

The Micron® Imaging MT9V111 is a 1/4-inch VGA-format CMOS active-pixel digital image sensor, the result of combining the MT9V011 image sensor core with Micron Imaging's third-generation digital image flow processor technology. The MT9V111 has an active imaging pixel array of 649 x 489, capturing high-quality color images at VGA resolution. The sensor is a complete camera-on-a-chip solution and is designed specifically to meet the demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

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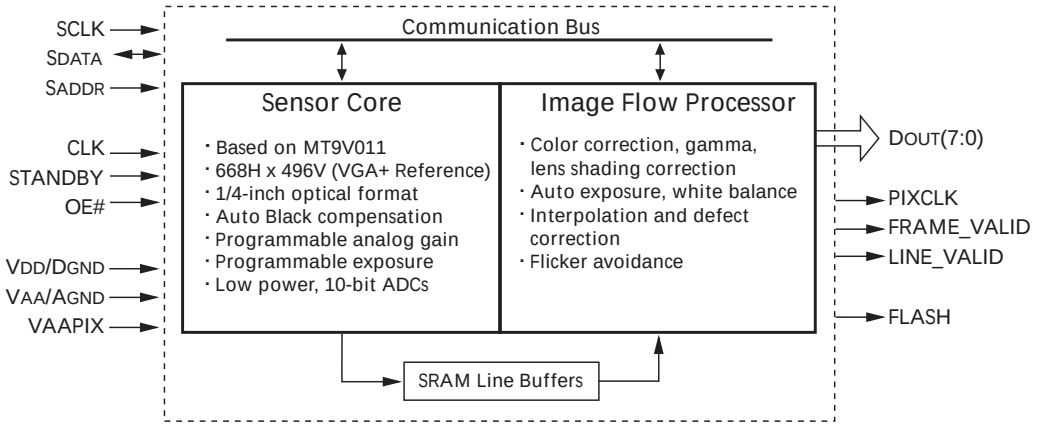
General Description

This SOC VGA CMOS image sensor features DigitalClarity—Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The MT9V111 is a fully-automatic, single-chip camera, requiring only a power supply, lens and clock source for basic operation. Output video is streamed via a parallel eight-bit DOUT port as shown in Figure 1. Output pixel clock is used to latch the data, while FRAME_VALID and LINE_VALID signals indicate the active video. The sensor can be put in an ultra-low power sleep mode by asserting the STANDBY pin. Output pads can also be tri-stated by de-asserting the OE# pin. The MT9V111 internal registers can be configured using a two-wire serial interface.

The MT9V111 can be programmed to output progressive scan images up to 30 fps in an 8-bit ITU_R BT.656 (YCbCr) formerly CCIR656, YUV, 565RGB, 555RGB, or 444RGB formats. The FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Figure 1: Chip Block Diagram

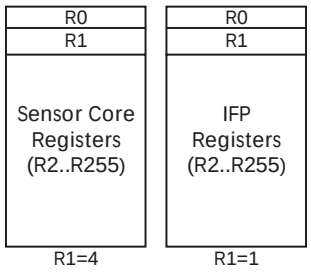


The MT9V111 can accept the input clock of up to 27 MHz, delivering 30 fps. With power-on defaults (see Appendix B for recommended defaults), the camera is configured to deliver 15 fps at 12 MHz and automatically slows down the frame rate in low-light conditions to achieve longer exposures and better image quality.

Internally, the MT9V111 consists of a sensor core and an image flow processor. The sensor core functions to capture raw Bayer-encoded images that are input into the IFP as shown in Figure 1. The IFP processes the incoming stream to create interpolated, color-corrected output and controls the sensor core to maintain the desirable exposure and color balance.

Sensor core and IFP registers are grouped into two separate address spaces, as shown in Figure 2. The internal registers can be accessed via the two-wire serial interface. Selecting the desired address space can be accomplished by programming register R1 which remains present in both register sets.

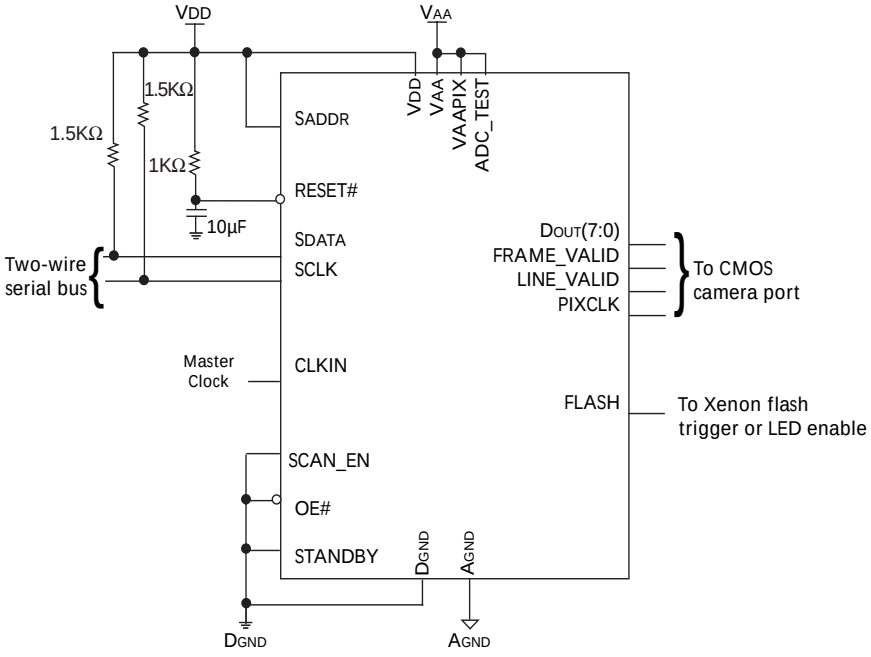
Figure 2: Internal Register Grouping



Note: Program R1 to select the desired space (4 = sensor core registes, 1 = IFP/SOC registers).

Figure 3 shows MT9V111 typical connections. For low-noise operation, the MT9V111 requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

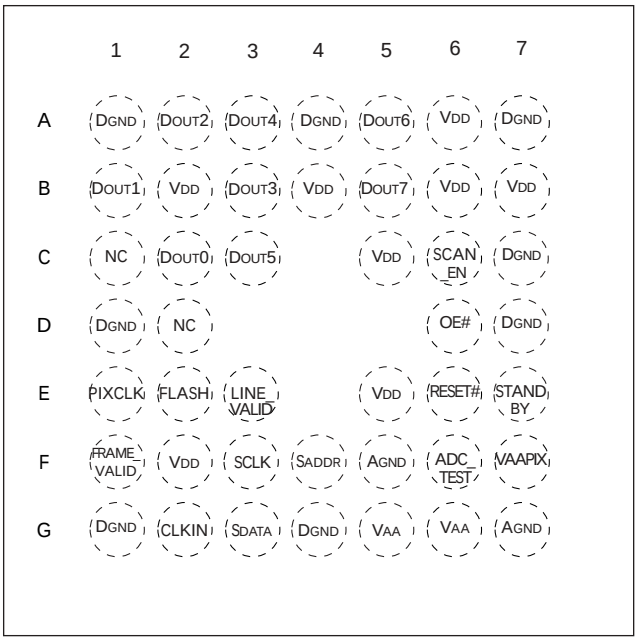
Figure 3: Typical Configuration (Connection)



Note: 1.5KΩ resistor value is recommended, but may be greater for slower two-wire speed.

Ball Assignment

Figure 4: 44-Ball ICSP Package



Top View
(Ball Down)

Table 2: Ball Description

Ball Numbers	Name	Type	Description
G2	CLKIN	Input	Master Clock into sensor. Default is 12 MHz (27 MHz maximum).
F3	SCLK	Input	Serial Clock.
F4	SADDR	Input	Serial Interface address select: Reg0xB8 when HIGH (default). Reg0x90 when LOW.
F6	ADC_TEST	Input	Tie to VAAPIX (factory use only).
E6	RESET#	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
E7	STANDBY	Input	When HIGH puts the imager in ultra-low power standby mode.
D6	OE#	Input	Output_Enable_Bar pin. When HIGH tri-state all outputs except SDATA (tie LOW for normal operation).
C6	SCAN_EN	Input	Tie to Digital ground.
G3	SDATA	I/O	Serial data I/O.
E2	FLASH	Output	Flash Strobe.
E1	PIXCLK	Output	Pixel Clock Out. Pixel data output are valid during rising edge of this clock. IFP Reg0x08 [9] inverts polarity. Frequency = Master Clock.
E3	LINE_VALID	Output	Active HIGH during line of selectable valid pixel data.
F1	FRAME_VALID	Output	Active HIGH during frame of valid pixel data.
B5	DOUT7	Output	ITU_R BT.656/RGB data bit 7 (MSB).

Table 2: Ball Description (Continued)

Ball Numbers	Name	Type	Description
A5	DOUT6	Output	ITU_R BT.656/RGB data bit 6.
C3	DOUT5	Output	ITU_R BT.656/RGB data bit 5.
A3	DOUT4	Output	ITU_R BT.656/RGB data bit 4.
B3	DOUT3	Output	ITU_R BT.656/RGB data bit 3.
A2	DOUT2	Output	ITU_R BT.656/RGB data bit 2.
B1	DOUT1	Output	ITU_R BT.656/RGB data bit 1.
C2	DOUT0	Output	ITU_R BT.656/RGB data bit 0 (LSB).
A6,B2,B4,B6, B7,C5,E5,F2	VDD	Supply	Digital Power (2.8V).
G5,G6	VAA	Supply	Analog Power (2.8V).
F7	VAAPIX	Supply	Pixel Array Power (2.8V).
F5,G7	AGND	Supply	Analog Ground.
A1,D1,A4, A7,C7,D7,G1,G4	DGND	Supply	Digital Ground.
C1,D2	NC	—	No connect.

Image Flow Processor

Overview of Architecture

The image flow processor consists of a color processing pipeline and a measurement and control logic block as shown in Figure 5. The stream of raw data from the sensor enters the pipeline and undergoes a number of transformations. Image stream processing starts from conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel and defective pixels are corrected. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections and is formatted for final output.

The measurement and control logic continuously accumulates statistics about image brightness and color. Indoor 50/60 Hz flicker is detected and automatically updated when possible. Based on these measurements the IFP calculates updated values for exposure time and sensor analog gains, which are sent to the sensor core via the communication bus.

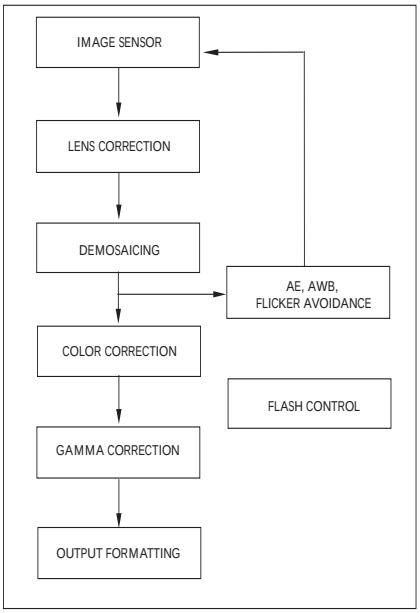
Color correction is achieved through linear transformation of the image with a 3 x 3 color correction matrix. Color saturation can be adjusted in the range from zero (black and white) to 1.25 (125% of full color saturation).

Gamma correction compensates for non-linear dependence of the display device output vs. driving signal (e.g. monitor brightness vs. CRT voltage).

Output and Formatting

Processed video can be output in the form of a standard ITU_R BT.656 or RGB stream. ITU_R BT.656 (default) stream contains 4:2:2 data with optional embedded synchronization codes. This kind of output is typically suitable for subsequent display by standard video equipment. For JPEG/MPEG compression, YUV/ encoding is suitable. RGB functionality is provided to support LCD devices. The MT9V111 can be configured to output 16-bit RGB (RGB565), 15-bit RGB (RGB555) as well as two types of 12-bit RGB (RGB444). The user can configure internal registers to swap odd and even bytes, chrominance channels and luminance and chrominance components to facilitate interface to application processors.

Figure 5: Image Flow Processor Block Diagram



The MT9V111 features smooth, continuous zoom and pan. This functionality is available when the IFP output is downsized in the decimation block. The decimation block can downsize the original VGA image to any integer size, including QVGA, QQVGA, CIF and QCIF with no loss to the field of view. The user can program the desired size of the output image in terms of horizontal and vertical pixel count. In addition the user can program the size of a region for downsizing. Continuous zoom is achieved every time the region of interest is less than the entire VGA image. The maximum zoom factor is equal to the ratio of VGA to the size of the region of interest. For example, an image rendered on a 160x120 display can be zoomed by 640/160=480/120=4 times. Continuous pan is achieved by adjusting the starting coordinates of the region of interest.

Also a fixed 2X up-zoom is implemented by means of windowing down the sensor core. In this mode the IFP receives a QVGA-sized input data and outputs a VGA-size image. The sub-window can be panned both vertically and horizontally by programming sensor core registers.

The MT9V111 supports both LED and Xenon-type flash light sources using a dedicated output pad. For Xenon devices the pad generates a strobe to fire when the imager's shutter is fully open. For LED the pad can be asserted or de-asserted asynchronously. Flash modes are configured and engaged over the two-wire serial interface using IFP Reg0x98.

Output Data Ordering

In YCbCr the first and second bytes can be swapped. Luma/chroma bytes can be swapped as well. R and B channels are bit-wise swapped when chroma swap is enabled. See IFP Reg0x3A for channel swapping configuration.

Table 3: YUV/YCbCr Output Data Ordering

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 4: RGB Output Data Ordering in Default Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB 565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB 555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB 444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGB x444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

A bypass mode is available whereby raw Bayer 10-bits data is output as two bytes. See IFP Reg8[7].

Table 5: Byte Ordering in 8 + 2 Bypass Mode

Byte Ordering									
8+2 Bypass	First	D9	D8	D7	D6	D5	D4	D3	D2
	Second	0	0	0	0	0	0	D1	D0

IFP Register List

Table 6: IFP Register List

Address		Defaults		Description
Dec	Hex	Dec	Hex	
0	00			Reserved
1	01	1	0x0001	Register Address Space Selection
2	02	110	0x006E	Color Correction Register 1
3	03	10531	0x2923	Color Correction Register 2
4	04	1316	0x0524	Color Correction Register 3
5	05	11	0x000B	Aperture Correction (Sharpening)
6	06	28686	0x700E	Operating Mode Control
7	07	0	0x0000	Image Flow Processor Soft Reset
8	08	51200	0xC800	Output Format Control
9	09	146	0x0092	Color Correction Register 4
10	0A	22	0x0016	Color Correction Register 5
11	0B	8	0x0008	Color Correction Register 6
12	0C	171	0x00AB	Color Correction Register 7
13	0D	147	0x0093	Color Correction Register 8
14	0E	88	0x0058	Color Correction Register 9
15	0F	77	0x004D	Color Correction Register 10
16	10	169	0x00A9	Color Correction Register 11
17	11	160	0x00A0	Color Correction Register 12
18	12	R/O		White Balance Register 1
19	13	R/O		White Balance Register 2
20	14	R/O		White Balance Register 3
21	15	373	0x0175	Color Correction Register 13
22	16	22	0x0016	Color Correction Register 14
23	17	67	0x0043	Color Correction Register 15
24	18	12	0x000C	Color Correction Register 16
25	19	0	0x0000	Color Correction Register 17
26	1A	21	0x0015	Color Correction Register 18
27	1B	31	0x001F	Color Correction Register 19
28	1C	22	0x0016	Color Correction Register 20
29	1D	152	0x0098	Color Correction Register 21
30	1E	76	0x004C	Color Correction Register 22
31	1F	160	0x00A0	White Balance Register 4
32	20	51220	0xC814	White Balance Register 5
33	21	0	0x0000	AWB Tint add-on color
34	22	55648	0xD960	White Balance Register 6
35	23	55648	0xD960	White Balance Register 7
36	24	32512	0x7F00	White Balance Register 8
37	25	17684	0x4514	AWB Speed and Color Saturation Control
38	26	65283	0xFF03	Horizontal Boundaries of AE Measurement Window
39	27	65296	0xFF10	Vertical Boundaries of AE Measurement Window
40	28	26624	0x6800	White Balance Register 9
41	29	36211	0x8D73	White Balance Register 10

Table 6: IFP Register List (Continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
42	2A	128	0x0080	White Balance Register 11
43	2B	30760	0x7828	Horizontal Boundaries of AE Measurement Window for Back Light Compensation
44	2C	46140	0xB43C	Vertical Boundaries of AE Measurement Window for Back Light Compensation
45	2D	57504	0xE0A0	Boundaries of AWB Measurement Window
46	2E	4196	0x1064	AE Target and Accuracy Control
47	2F	68	0x0044	AE Speed and Sensitivity Control
48	30	R/O		White Balance Register 12
49	31	R/O		White Balance Register 13
50	32	R/O		White Balance Register 14
51	33	5230	0x146E	Auto Exposure Register 1
52	34	16	0x0010	Luminance Offset Control
53	35	61456	0xF010	Clipping Limits for Output Luminance
54	36	30736	0x7810	Auto Exposure Register 2
55	37	768	0x0300	White Balance Register 15
56	38	1144	0x0478	Auto Exposure Register 3
57	39	680	0x02A8	Auto Exposure Register 4
58	3A	0	0x0000	Output Format Control 2
59	3B	1066	0x042A	Black Level Register 1
60	3C	1024	0x0400	Black Level Register 2
61	3D	4570	0x11DA	Auto Exposure Register 5
62	3E	3327	0x0CFF	White Balance Register 16
63	3F	0	0x0000	Auto Exposure Register 6
64	40	7696	0x1E10	Auto Exposure Register 7
65	41	5143	0x1417	Auto Exposure Register 8
66	42	26128	0x6610	Auto Exposure Register 9
67	43	28010	0x6D6A	Auto Exposure Register 10
68	44	29040	0x7170	Auto Exposure Register 11
69	45	29811	0x7473	Auto Exposure Register 12
70	46	0	0x0000	Auto Exposure Register 13
71	47	24	0x0018	Defect Correction Register 1
72	48	0	0x0000	Test Pattern Generator
74	4A	R/O		Reserved
75	4B	R/O		Reserved
76	4C	R/O		Auto Exposure Register 14
77	4D	R/O		Auto Exposure Register 15
78	4E	16	0x0010	Reserved
79	4F	R/O		Reserved
82	52	R/O		Reserved
83	53	7700	0x1E14	Gamma Correction Register 1
84	54	17966	0x462E	Gamma Correction Register 2
85	55	34666	0x876A	Gamma Correction Register 3
86	56	47008	0xB7A0	Gamma Correction Register 4

Table 6: IFP Register List (Continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
87	57	57548	0xE0CC	Gamma Correction Register 5
88	58	0	0x0000	Gamma Correction Register 6
89	59	248	0x00F8	Auto Exposure Register 16
90	5A	298	0x012A	Auto Exposure Register 17
91	5B	2	0x0002	Flicker Control
92	5C	4366	0x110E	Reserved
93	5D	5137	0x1411	Reserved
94	5E	26684	0x683C	Color Correction Register 23
95	5F	12296	0x3008	Color Correction Register 24
96	60	2	0x0002	Color Correction Register 25
97	61	R/O		Reserved
98	62	4112	0x1010	AE Digital Gains
99	63	R/O		Reserved
100	64	5499	0x157B	Reserved
102	66	R/O		Reserved
103	67	16400	0x4010	AE Digital Gains Limit
104	68	17	0x0011	Reserved
105-125	69-8D	R/O		Reserved
127	7F	N/A		8-bit Serial Interface Helper
128	80	6	0x0006	Lens Shading Correction Register 1
129	81	56588	0xDD0C	Lens Shading Correction Register 2
130	82	1268	0x04F4	Lens Shading Correction Register 3
131	83	15377	0x3C11	Lens Shading Correction Register 4
132	84	57868	0xE20C	Lens Shading Correction Register 5
133	85	758	0x02F6	Lens Shading Correction Register 6
134	86	12817	0x3211	Lens Shading Correction Register 7
135	87	56588	0xDD0C	Lens Shading Correction Register 8
136	88	244	0x00F4	Lens Shading Correction Register 9
137	89	12822	0x3216	Lens Shading Correction Register 10
138	8A	34866	0x8832	Lens Shading Correction Register 11
139	8B	63453	0xF7DD	Lens Shading Correction Register 12
140	8C	15372	0x3C0C	Lens Shading Correction Register 13
141	8D	127	0x007F	Lens Shading Correction Register 14
142	8E	47646	0x6A1E	Lens Shading Correction Register 15
143	8F	63468	0xF7EC	Lens Shading Correction Register 16
144	90	14088	0x3708	Lens Shading Correction Register 17
145	91	100	0x0064	Lens Shading Correction Register 18
146	92	48926	0x6F1E	Lens Shading Correction Register 19
147	93	63470	0xF7EE	Lens Shading Correction Register 20
148	94	12815	0x320F	Lens Shading Correction Register 21
149	95	100	0x0064	Lens Shading Correction Register 22
152	98	1040	0x0410	Flash Control
153	99	R/O		Line Counter
154	9A	R/O		Frame Counter

Table 6: IFP Register List (Continued)

Address		Defaults		Description
Dec	Hex	Dec	Hex	
155	9B	R/O		Reserved
156	9C	8	0x0008	Reserved
157	9D	42158	0xA4AE	Reserved
158	9E	R/O		Reserved
165	A5	0	0x0000	Horizontal Pan In Decimation
166	A6	640	0x0280	Horizontal Zoom In Decimation
167	A7	640	0x0280	Horizontal Output Size In Decimation
168	A8	0	0x0000	Vertical Pan In Decimation
169	A9	480	0x01E0	Vertical Zoom In Decimation
170	AA	480	0x01E0	Vertical Output Size In Decimation

IFP Register Description

Table 7: IFP Register Description

Register	Bits	Default	Name
1 **0x01**	7:0	1	Register address space selection.
	This register controls the address space for the two-wire serial interface communications. Set Reg0x01 = 1 to select IFP address space and Reg0x01 = 4 for sensor space. Reg0x01 is always accessible regardless of the page currently selected.		
5 **0x05**	3:0	11	Aperture correction (sharpening).
	2:0	3	Sharpening factor: ”000” — no sharpening. ”001” — 25% sharpening. ”010” — 50% sharpening. ”011” — 75% sharpening. ”100” — 100% sharpening. ”101” — 125% sharpening. ”110” — 150% sharpening. ”111” — 200% sharpening.
	3	1	Automatically reduces sharpness in low light.
6 **0x06**	15:0	28686	Operating mode control.
	0	0	Reserved.
	1	1	“1” — enables auto white balance. “0” — stops AWB at the current values.
	3:2	3	Back light compensation: ”00” — AE measurement window is specified by Reg0x26 and Reg0x27 (“large window”). “01” — AE measurement window is specified by Reg0x2B and Reg0x2C (“center window”). “10” and “11” — AE measurement window is a weighted sum of “large window” and “center window” with center window given twice the weight.
	4	0	“1” — bypass color correction matrix. “0” — normal color processing.
	5	0	Reserved.
	6	0	Reserved.
	7	0	“1” — ITU_R BT.656 synchronization codes are embedded in the image.
	9:8	0	N/A
	10	0	Reserved.
	11	0	Reserved.
	12	1	Enable aperture correction knee.
	13	1	“1” — enables on-the-fly defect correction.
	14	1	“1” — enable auto exposure.
	15	0	Reserved.
7 **0x07**	0	0	Image flow processor soft reset.
			Asserts reset on all IFP registers. Example: write Reg0x07 = 1 followed by Reg0x07 = 0 to reset IFP.

Table 7: IFP Register Description (Continued)

Register	Bits	Default	Name
8 0x08	15:0	51200	Output format control.
	0	0	Toggles the assumption about Bayer CFA (horizontal shift). “0” — row containing blue comes first. “1” — row with red comes first.
	1	0	Toggles the assumption about Bayer CFA (vertical shift). “0” — green comes first. “1” — red or blue comes first.
	2	0	Disable Cr. Forces output Cr = 128 in YCbCr mode and R = 0 in RGB.
	3	0	Disable Y. Force output Y = 128 in YCbCr mode and G = 0 in RGB.
	4	0	Disable Cb. Force output Cb = 128 in YCbCr mode and B = 0 in RGB.
	5	0	Monochrome. Forces Cr=Cb=128 in YCbCr or R,B = G in RGB mode.
	6	0	N/A
	7	0	Entire image processing is bypassed and raw 8+2 Bayer data output directly.
	8	0	“1” — enables lens shading correction.
	9	0	Inverts output pixel clock.
	10	0	Reserved.
	11	1	Enable automatic flicker avoidance.
	12	0	“1” output mode is RGB. “0” — output mode is YCbCr. See also Reg0x3A[7:6]. This bit is subject to synchronous update, see Reg0xA5.
	13	0	N/A
	14	1	Reserved.
	15	1	Reserved.
33 0x21	15:0	0	AWB tint.
	7:0	0	Blue channel add-on.
	15:8	0	Red channel add-on.
	In the AWB mode, this register specifies gain “add-ons” to the values determined by AWB, allowing to “skew” the overall color of the image.		
37 0x25	14:0	17700	AWB speed and color saturation control.
	2:0	4	AWB reaction delay: “000” — fastest. "111” — slowest.
	6:3	4	AWB speed. “000” — fastest. "111” — slowest.
	10:8	5	Reserved.
	13:11	0	U/V saturation. Specify overall attenuation of the color saturation: ”000” — full color saturation. ”001” — 75% of full saturation. “010” — 50% of full saturation. ”011” — 37.5% of full saturation. ”100” — 25% of full saturation. ”101” — 150% of full saturation. ”110” — black and white.
	14	1	“1” — enables automatic color saturation control in low light. The automatic saturation control acts “in addition” to the saturation specified in Bits13:11.

Table 7: IFP Register Description (Continued)

Register	Bits	Default	Name
38 0x26	15:0	65283	Horizontal boundaries of AE measurement window.
	7:0	3	Left window boundary.
	15:8	255	Right window boundary.
	This register specifies left and right boundaries of the window used by AE measurement engine. The values programmed in the registers are desired boundaries divided by four.		
39 0x27	15:0	65296	Vertical boundaries of AE measurement window.
	7:0	16	Bottom window boundary.
	15:8	255	Top window boundary.
			This register specifies top and bottom boundaries of the window used by AE measurement engine. The values programmed in the registers are desired boundaries divided by two.
43 0x2B	15:0	30760	Horizontal boundaries of AE measurement window for back light compensation.
	7:0	40	Left window boundary.
	15:8	120	Right window boundary.
			This register specifies left and right boundaries of the window used by AE measurement engine in backlight compensation mode, see Reg6[3:2]. The values programmed in the registers are desired boundaries divided by four.
44 0x2C	15:0	46140	Vertical boundaries of AE measurement window for back light compensation.
	7:0	60	Top window boundary.
	15:8	180	Bottom window boundary.
	This register specifies top and bottom boundaries of the window used by AE measurement engine in backlight compensation mode, see Reg6[3-2]. The values programmed in the registers are desired boundaries divided by two.		
45 0x2D	15:0	57504	Boundaries of AWB measurement window.
	3:0	0	Left window boundary.
	7:4	10	Right window boundary.
	11:8	0	Top window boundary.
	15:12	14	Bottom window boundary.
	This register specifies the boundaries of the window used by AWB measurement engine. The values programmed in the registers are desired boundaries divided by 32 for vertical limits and by 64 for horizontal.		
46 0x2E	15:0	4196	Auto exposure target and accuracy control.
	7:0	100	Target luminance.
	15:8	16	Tracking accuracy.
	This register specifies luminance target of the auto exposure algorithm and the size of the margin around the target in which no AE adjustment is made.		
47 0x2F	7:0	68	Auto exposure speed and sensitivity control.
	2:0	4	AE reaction delay: “000” — fastest. "111” — slowest.
	5:3	0	AE speed: “000” — fastest. "111” — slowest.
	7:6	0	AE step size: “00” — medium speed when going down, slow when going up. ”01” — medium speed. ”10” — fast speed. ”11” — fast when going down, medium when going up.

Table 7: IFP Register Description (Continued)

Register	Bits	Default	Name
52 0x34	15:0	16	Luminance offset control. Use this register to adjust LCD brightness.
	7:0	16	Y offset in YCbCr mode.
	15:8	0	Offset in RGB mode.
	This register specifies constant offset added to the luminance or RGB components prior to the output. Use this register to adjust LCD brightness.		
53 0x35	15:0	61456	Clipping limits for output luminance.
	7:0	16	Lowest value of output luminance.
	15:8	240	Highest value of output luminance.
	This register specifies upper and low limits to which the output YCbCr data is clipped.		
58 0x3A	7:0	0	Output format control 2.
	0	0	In YUV output mode swaps Cb and Cr channels. In RGB, swaps R and B. This bit is subject to synchronous update.
	1	0	Swap chrominance byte with luminance byte in YCbCr/YUV output. In RGB, swap odd and even bytes. This bit is subject to synchronous update.
	2	0	Average two nearby chrominance bytes.
	4:3	0	Test ramp output: “00” — off. “01” — by column. “10” — by row. “11” — by frame.
	5	0	Output R,G,B or Cr,Y,Cb values are shifted 3 bits up; use with Reg0x3A[4:3] to test LCDs with low color depth.
	7:6	0	RGB output format: “00” = 16-bit RGB565. ”01” = 15-bit RGB555. “10” = 12-bit RGB444. “11” = 12-bit RGBx444.
72 0x48	7:0	0	Test pattern generator.
	2:0	0	Test pattern selection.
	7	0	“1” — force WB digital gains to 1.0.
	This register enables color bar test-pattern generation at the input of the image processor. Values greater than "0" turn test pattern generation on. The brightness of the flat-color areas depends on the value programmed in this register.		
91 0x5B	2:0	2	Flicker control.
	0	0	“1”— manual mode. “0” — auto flicker detection.
	1	1	If R0x5B [0] = “1” then '“0”- 50Hz AC; “1”- 60Hz AC.
98 0x62	15:0	4112	AE digital gains.
	7:0	16	Current digital gain applied before lens shading correction.
	15:8	16	Current digital gain applied during lens shading correction.
	When R6 [14] = 1, registers are read-only and show current digital gains. When R6 [14] = 0, writing into registers sets current digital gains. LC digital gain, R98 [15:8], is unity if LC is disabled, R8 [8] = 0. The combined gain of R98 [15:8] and LC must be less than 16. See also R103.		
103 0x67	15:0	16400	AE digital gains limits.
	7:0	16	Maximal digital gain applied before lens shading correction.
	15:8	64	Maximal digital gain applied during lens shading correction.
	Value 16 corresponds real digital gain of 1.0. As AE increases gain in dark conditions, pre-LC gain is used first. Post-LC gain is used only after pre-LC gain reaches its maximum allowed limit. See also R98.		

Table 7: IFP Register Description (Continued)

Register	Bits	Default	Name
127 0x7F	7:0	0	Eight-bit, Two-wire serial interface helper.
	Internal MT9V111 registers are up to 16-bit wide. To execute 16-bit reads and writes, eight-bit two-wire serial interface devices need special handling by using Reg0x7F. A 16-bit write is done by writing the upper eight bits to the desired register and then writing the lower eight bits to Reg0x7F. The register is not updated until all 16 bits have been written. It is not possible to just update half a register. To read eight-bytes at a time, read the upper eight bits from the desired register; then read the lower eight bits from Reg0x7F.		
152 0x98	15:0	1040	Flash control.
	7:0	16	Strobe duration, x512 CLK_IN. Value of 255 is special, enabling infinite duration.
	8	0	Invert pin state.
	9	0	“1” = fire every frame continuously. “0” = fire only once per arming.
	10	1	Strobe source select. “1” = end of shutter enable. “0” = end of frame enable.
	12:11	0	Delay; skips programmed number of frames after arming and before firing.
	13	0	Write “1” to arm flash and set it to fire. Flash will fire after delay set in Reg0x98 [12-11].
	14	R/O	“1” = Flash has fired in current frame.
	15	R/O	State of the output flash pin.
	The flash control supports both Xenon and LED light sources using a dedicated output pad. For Xenon flashes the pad generates a strobe to fire when the imager's shutter is fully open. For LED the pad can be asserted or de-asserted asynchronously. To turn LED off and on program Reg0x98 [8]. To fire a Xenon flash, arm the strobe trigger by setting Reg0x98 [13]=1. The strobe will appear when the shutter fully opens. Strobe length is set by Reg0x98 [7-0]. Other available modes include continuous vs. single firing and skipping a programmable number of frames after arming and before firing.		
153 0x99	12:0	R/O	Line counter.
	Use line counter to determine the number of line currently being output.		
154 0x9A	15:0	R/O	Frame counter.
	Use frame counter to determine number of frames output so far.		
165 0xA5	15:0	0	Horizontal pan in decimation.
	9:0	0	Horizontal pan.
	15	W/O	“1” = freeze update of decimation parameters.
	Decimation control registers work to downsize output image to any size. The output image size is specified in Reg0xA7 and Reg0xAA for horizontal and vertical directions respectively. For example, to downsize the VGA output to QQVGA set Reg0xA7 = 160 and Reg0xAA = 20. Whenever output image is downsized, the zoom feature becomes available. To zoom in, program Reg0xA6 and Reg0xA9 with the size of window to be decimated. For example, in QQVGA setting Reg0xA6 = 320 and Reg0xA9 = 240 results in 2X zoom. Here the output image of 160 x 120 is created from a pre-decimation window of 320 x 240 instead of the full VGA 640 x 480. Whenever the output image is zoomed, pan controls become available. To pan a zoomed image program Reg0xA5 and Reg0xA8 to offset the pre-decimation window in to the right and bottom respectively. When implementing a smooth zoom and pan, it is useful to synchronize the update of all decimation registers to avoid jerks in the output video. When writing a batch of decimation settings, set bit 15 of each datum to”1” to freeze the update. Set bit 15 of the last datum in the batch to “0” to enable normal operation. The entire batch of decimation settings will then be synchronously loaded on the next frame start.		
166 0xA6	15:0	640	Horizontal zoom in decimation.
	9:0	640	Horizontal size of window before decimation.
	15	W/O	“1” = freeze update of decimation parameters.
	See R0xA5 for details.		

Table 7: IFP Register Description (Continued)

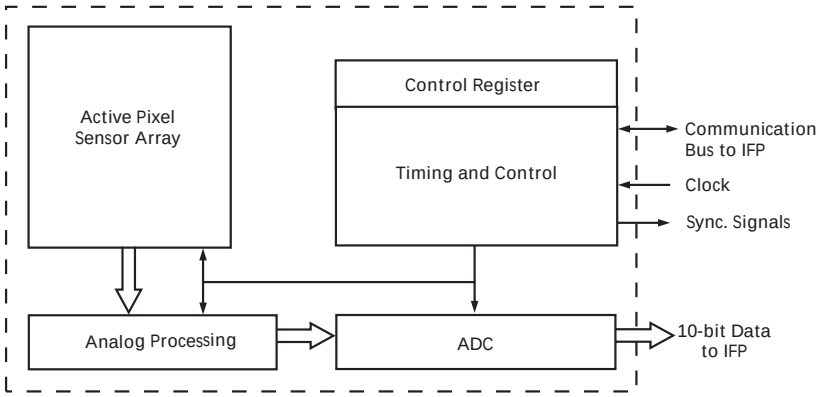
Register	Bits	Default	Name
167 0xA7	15:0	640	Horizontal output size in decimation.
	9:0	640	Horizontal size of output image.
	15	W/O	"1" = freeze update of decimation parameters.
	See R0xA5 for details.		
168 0xA8	15:0	0	Vertical pan in decimation.
	8:0	0	Vertical pan.
	15	W/O	"1" = freeze update of decimation parameters.
	See R0xA5 for details.		
169 0xA9	15:0	480	Vertical zoom in decimation.
	8:0	480	Vertical size of window before decimation.
	15	W/O	"1" = freeze update of decimation parameters.
	See R0xA5 for details.		
170 0xAA	15:0	480	Vertical output size in decimation.
	8:0	480	Vertical size of output image.
	15	W/O	"1" = freeze update of decimation parameters.
	See R0xA5 for details.		

Sensor Core Overview

The sensor consists of a pixel array of 668 x 496 total, analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

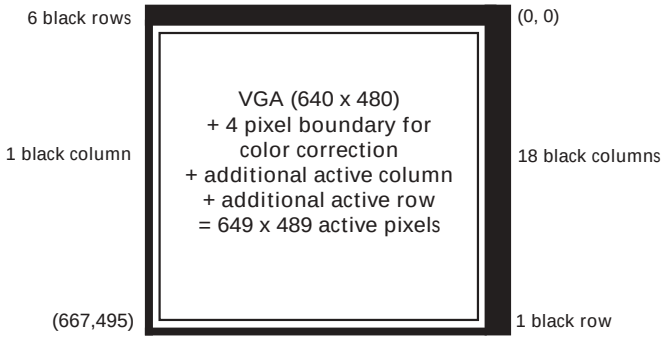
Note: See Sensor Core (MT9V011) data sheet for more details.

Figure 6: Sensor Core Block Diagram



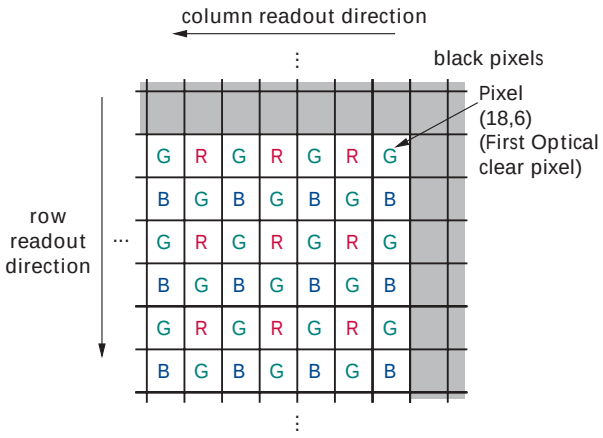
The sensor core's pixel array is configured as 668 columns by 496 rows (shown in Figure 7). The first 18 columns and the first 6 rows of pixels are optically black and can be used to monitor the black level. The last column and the last row of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. There are 649 columns by 489 rows of optically active pixels, which provides a four-pixel boundary around the VGA (640 x 480) image to avoid boundary affects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel, as shown in Figure 7.

Figure 7: Pixel Array Description



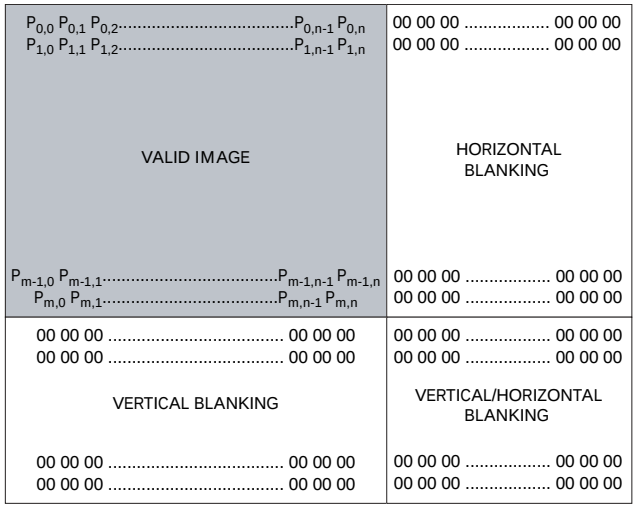
The sensor core uses the RGB Bayer color pattern (shown in Figure 8). Even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

Figure 8: Pixel Color Pattern Detail (Top Right Corner)



The sensor core image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 9. The amount of horizontal and vertical blanking is programmable through the sensor core registers Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Appendix A – Sensor Timing" on page 35 for the description of FRAME_VALID timing.

Figure 9: Spatial Illustration of Image Readout



Sensor Core Registers

Table 8: Sensor Core Register List

Register		Description	Default Value	
Dec	Hex		Dec	Hex
0	0x00	Reserved	-	-
1	0x01	Register Address Select	1	0x01
2	0x02	Column Start[1]	18	0x0012
3	0x03	Window Height[1]	487	0x01E7
4	0x04	Window Width[1]	647	0x0287
5	0x05	Horizontal Blanking	38	0x0026
6	0x06	Vertical Blanking[1]	4	0x0004
7	0x07	Output Control[1]	12306	0x3012
8	0X08	Row Start[1]	6	0x0006
9	0x09	Shutter Width[2]	248	0x00F8
10	0x0A	Reserved	0	0x0000
11	0x0B	Reserved	0	0x0000
12	0x0C	Shutter Delay[2]	0	0x0000
13	0x0D	Reserved	0	0x0000
18	0x12	2X Zoom Col Start	176	0x00B0
19	0x13	2X Zoom Row Start	124	0x007C
30	0x1E	Digital Zoom	0	0x0000
32	0x20	Read Mode	4096	0x1000
33	0x21	Reserved	0	0x0000
34	0x22	Reserved	0	0x0000
39	0x27	Reserved	36	0x0024
40	0x28	Reserved	0	0x0000
43	0x2B	Green1 Gain[2]	32	0x0020
44	0x2C	Blue Gain[2]	32	0x0020
45	0x2D	Red Gain[2]	32	0x0020
46	0x2E	Green2 Gain[2]	32	0x0020
47	0x2F	Reserved	63408	0xF7B0
48	0x30	Reserved	30725	0x7805
49	0x31	Reserved	42	0x002A
50	0x32	Reserved	0	0x0000
51	0x33	Reserved	12303	0x300F
52	0x34	Reserved	256	0x0100
53	0x35	Global Gain[2]	32	0x0020
54	0x36	Chip Version (R/O)	33338	0x823A
55	0x37	Reserved	10	0x000A
59	0x3B	Reserved	N/A	
60	0x3C	Reserved	2080	0x0820
61	0x3D	Reserved	1679	0x068F
62	0x3E	Reserved	N/A	
63	0x3F	Reserved	1696	0x06A0
64	0x40	Reserved	480	0x01E0
65	0x41	Reserved	209	0x00D1
66	0x42	Reserved	2178	0x0882

Table 8: Sensor Core Register List (Continued)

Register		Description	Default Value	
Dec	Hex		Dec	Hex
88	0x58	Reserved	248	0x00F8
89	0x59	Reserved	1859	0x0743
90	0x5A	Reserved	1063	0x0427
91	0x5B	Reserved	R/O	
92	0x5C	Reserved	R/O	
93	0x5D	Reserved	R/O	
94	0x5E	Reserved	R/O	
95	0x5F	Reserved	41757	0xA31D
96	0x60	Reserved	0	0x0000
97	0x61	Reserved	0	0x0000
98	0x62	Reserved	1048	0x0418
99	0x63	Reserved	0	0x0000
100	0x64	Reserved	0	0x0000
101	0x65	Reserved	0	0x0000
241	0xF1	Reserved	1	0x0001
247	0xF7	Reserved	R/O	
248	0xF8	Reserved	R/O	
249	0xF9	Reserved	44	0x002C
250	0xFA	Reserved	R/O	
251	0xFB	Reserved	R/O	
252	0xFC	Reserved	R/O	
253	0xFD	Reserved	R/O	
255	0xFF	Chip Version (R/O)	33338	0x823A

Notes: 1. Do not change these registers. Contact Micron support for settings different from defaults.
2. IFP controls these registers when AE, AWE, or flicker avoidance are enabled.

Table 9: Sensor Core Register Description

Register (Dec) (Hex)	Bit	Description
Register Address Selector		
1 0X01	0	Selects the IFP/SOC registers (0–170). 001= Select IFP registers—default = 0x01.
	2	Selects the core registers (0–255). 100 = Select core registers.
Window Control These registers control the size of the window. Register values are one less than actual height and width.		
2 0x02	9:0	First column to be read out—default = 0x0012 (18). See Reg0x08 for row adjustment.
3 0x03	8:0	Window height (number of rows - 1)—default = 0x01E7 (487).
4 0x04	9:0	Window width (number of columns - 1)—default = 0x0287 (647). Minimum value for Reg0x04 = 0x0009.
Blanking Control These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. Register values are one less than actual height and width.		
5 0x05	9:0	Horizontal blanking (number of columns)—default = 0x0026 (38 pixel clocks). Minimum value for Reg0x05 = 0x009.
6 0x06	11:0	Vertical Blanking (number of rows -1)—default = 0x0004 (4 rows). Minimum recommended value for Reg0x06 = 0x0003.
Output Control This register controls various features of the output format for the sensor.		
7 0x07	1:0	Reserved.
	4	Controls internal sampling time. This must be “0” when CLK_IN frequency is greater than 13.5 MHz.
	15:5	Reserved.
Row Start		
8 0x08	8:0	First row to be read out—default = 0x0006 (6). Minimum value for Reg0x08 = 0x0004.

Table 9: Sensor Core Register Description (Continued)

Register (Dec) (Hex)	Bit	Description
Pixel Integration Control These registers (along with the window sizing and blanking registers) control the integration time for the pixels. Reg0x09: number of rows of integration Reg0x0C: reset delay, default = 0x0000 (0). This is the number of master clocks that the timing and control logic waits before asserting the reset for a given row. The actual total integration time, t_{INT}, is: t_{INT} = Reg0x09 x Row Time - Overhead Time - Reset Delay, where: Row Time = (Reg0x04 + 1 + 113 + Reg0x05) x 2 master clock periods Overhead Time = K x 57 master clock periods Reset Delay = K x Reg0x0C master clock periods If the value in Reg0x0C exceeds (row time - 444)/K master clock cycles, the row time will be extended by (K x Reg0x0C - (row time - 444)) clock cycles where K = 4 when Reg0x07[4] = 0 and K = 2 when Reg0x07[4] = 1 In this expression the row time term corresponds to the number of rows integrated. The overhead time is the time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay. Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9V111 will add additional blanking rows as needed.		
9 0x09	11:0	Number of rows of integration—default = 0x00F8 (248).
Shutter Delay		
12 0x0C	9:0	Default = 0x0000 (0). This is the number of master clocks x K that the timing and control logic waits before asserting the reset for a given row.
Reset (Soft)		
13 0x0D	0	This register is used to reset the sensor to its default, power-up state. To reset, first write a “1” into bit 0 of this register to put the MT9V111 in reset mode, then write a "0" into bit 0 to resume operation.
2X Zoom		
18 0x12	9:0	Address of starting column in 2X zoom mode. Bit 0 of Reg0x1E must be set.
19 0x13	8:0	Address of starting row in 2X zoom mode. Bit 0 of Reg0x1E must be set.
30 0x1E	0	Zoom by 2X. This bit must be set when using Reg0x12 and Reg0x13.

Table 9: Sensor Core Register Description (Continued)

Register (Dec) (Hex)	Bit	Description
Read Mode This register is used to control many aspects of the readout of the sensor.		
32 0x20	To preserve a right-reading image and the correct color order, all four of these bits should be set to "1" to invert the image.	
	5	1 = readout starting 1 column later. 0 = normal readout.
	7	1 = readout starting 1 row later. 0 = normal readout.
	14	1 = read out from right to left (mirrored). 0 = normal readout.
	15	1 = read out from bottom to top (upside down). 0 = normal readout.
Gain Settings The gain is individually controllable for each color in the Bayer pattern as shown in the register chart. Formula for gain setting: Gain = (Bit [8] + 1) x (Bit [7] + 1) x (Bit [6–0] x 0.03125) Since Bit [7] and Bit [8] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings: Gain — Increments — Recommended Settings 1.000 to 1.969 — 0.03125 — 0x020 to 0x03F 2.000 to 7.938 — 0.0625 — 0x0A0 to 0x0FF 8.000 to 15.875 — 0.125 — 0x1C0 to 0x1FF		
43 0x2B		Green1 gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
44 0x2C		Blue Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
45 0x2D		Red Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain.)
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
46 0x2E		Green2 Gain—default = 0x0020 (32) = 1x gain.
	6:0	Initial Gain = bits (6:0) x 0.03125.
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain each bit gives 2x gain).
	9,10	Total gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
Global Gain		
53 0x35		Global Gain—default = 0x0020 (32) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.

Table 9: Sensor Core Register Description (Continued)

Register (Dec) (Hex)	Bit	Description
	6:0	Initial Gain = bits (6:0) x 0.03125
	7, 8	Analog Gain = (bit 8 + 1) x (bit 7 + 1) x initial gain (each bit gives 2x gain).
	9,10	Total Gain = (bit 9 + 1) x (bit 10 + 1) x analog gain (each bit gives 2x gain).
Chip Version		
54 0x36	15:0	This read-only register contains the chip identification number. Reg0xFF (255) is a repeat of this register.
255 0xFF	15:0	Mirrors the chip identification in Reg0x36.

Electrical Specifications

The recommended die operating temperature ranges from -20°C to +40°C. The sensor image quality may degrade above +40°C.

Table 10: DC Electrical Characteristics

$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
V_{IH}	Input High Voltage		V_{DD} - 0.25		V_{DD} + 0.25	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; $V_{IN} = V_{DD}$ or DGND	-5		5.0	µA
V_{OH}	Output High Voltage		V_{DD} - 0.2			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output High Current				15.0	mA
I_{OL}	Output Low Current				20.0	mA
I_{OZ}	Tri-state Output Leakage Current				5.0	µA
I_{AA}	Analog Operating Supply Current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 10.0 10.0	 20.0 20.0	 25.0 25.0	mA
I_{DD}	Digital Operating Supply Current	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 5.0 10.0	 8.0 15.0	 20.0 20.0	mA
I_{AA} Standby	Analog Standby Supply Current	STDBY = V_{DD}	0.0	2.5	5.0	µA
I_{DD} Standby	Digital Standby Supply Current	STDBY = V_{DD}	0.0	2.5	5.0	µA

Notes: 1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 11: AC Electrical Characteristics

$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
f_{CLKIN}	Input Clock Frequency			12	27	MHz
	Clock Duty Cycle		45	50	55	%
t_R	Input Clock Rise Time			2.0		ns
t_F	Input Clock Fall Time			2.0		ns
t_{PLHP} t_{PHLP}	CLKIN to PIXCLK propagation delay: LOW-to-HIGH HIGH-to-LOW	C_{LOAD} = 10pF		 12 10		ns
t_{DSETUP} t_{DHOLD}	PIXCLK to D_{OUT}(7:0) at 27 MHz Setup Time Hold Time	C_{LOAD} = 10pF		 13.0 13.0		ns
t_{DSETUP} t_{DHOLD}	PIXCLK to D_{OUT}(7:0) at 12 MHz Setup Time Hold Time	C_{LOAD} = 10pF		 25.0 25.0		ns
t_{OH}	Data Hold Time from PIXCLK falling edge			9.0		ns
$t_{PLHF,L}$ $t_{PHLF,L}$	CLKIN to FRAME_VALID and LINE_VALID propagation delay: LOW-to-HIGH HIGH-to-LOW	C_{LOAD} = 10pF		 9.0 7.5		ns
t_{OUTR}	Output Rise Time	C_{LOAD} = 10pF		7.0		ns
t_{OUTF}	Output Fall Time	C_{LOAD} = 10pF		9.0		ns

Notes: 1. For 30 fps operation with a 27 MHz clock, it is very important to have a precise duty cycle equal to 50%. With a slower frame rate and a slower clock the clock duty cycle can be relaxed.

Propagation Delays

Propagation Delays for PIXCLK and Data Out Signals

The typical output delay, relative to the master clock edge, is 7.5 ns. Note that the data outputs change on the falling edge of the master clock, with the pixel clock rising on the subsequent rising edge of the master clock.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same falling master clock edge as the data output. The LINE_VALID goes HIGH on the same falling master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock falling edge as the end of the output of the last valid pixel's data.

As shown in Figure 12, Data Output Timing Diagram, on page 33, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to 6 pixel clocks after the last LINE_VALID goes LOW.

Figure 10: Propagation Delays for PIXCLK and Data Out Signals

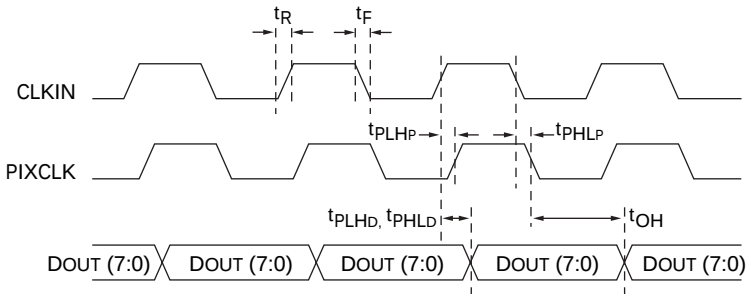


Figure 11: Propagation Delays for FRAME_VALID and LINE_VALID Signals

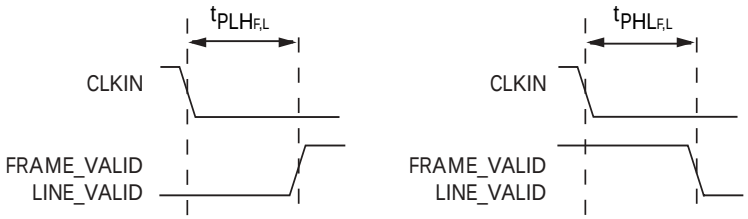
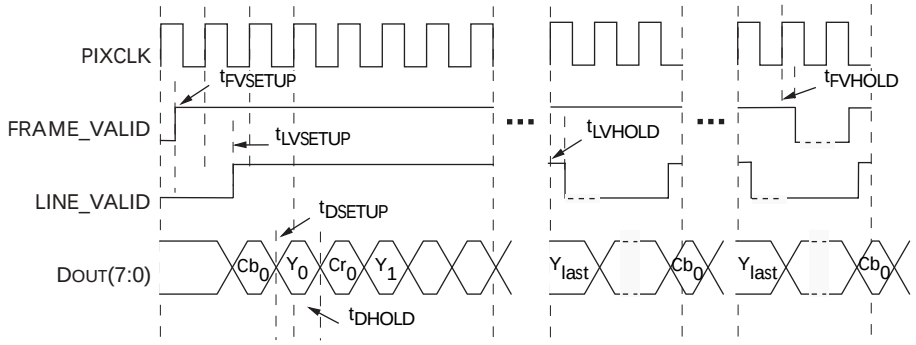


Figure 12: Data Output Timing Diagram



Note: PIXCLK = MAX 27 MHz
^{t}FVSETUP = / setup time for FRAME_VALID before rising edge of PIXCLK / = 18ns
^{t}FVHOLD = / hold time for FRAME_VALID after rising edge of PIXCLK / = 18ns
^{t}LVSETUP = / setup time for LINE_VALID before rising edge of PIXCLK / = 18ns
^{t}LVHOLD = / hold time for LINE_VALID after rising edge of PIXCLK / = 18ns
^{t}DSETUP = / setup time for DOUT before rising edge of PIXCLK / = 13ns
^{t}DHOLD = / hold time for DOUT after rising edge of PIXCLK / = 13ns
Frame start: FF00 00A0
Line start: FF00 0080
Line end: FF00 0090
Frame end: FF00 00B0

Figure 13: Spectral Response

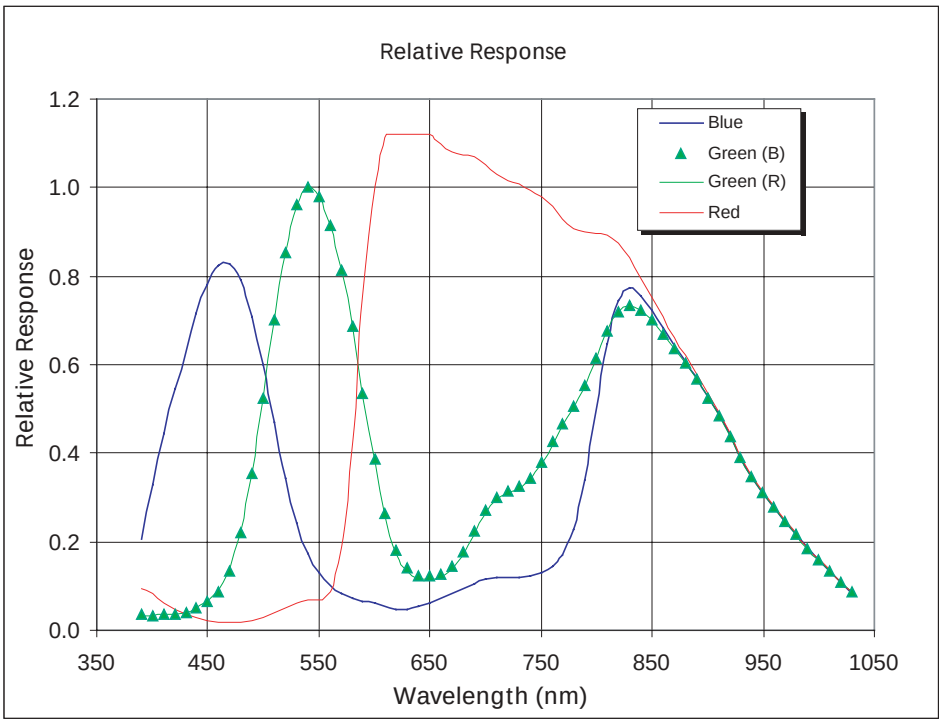
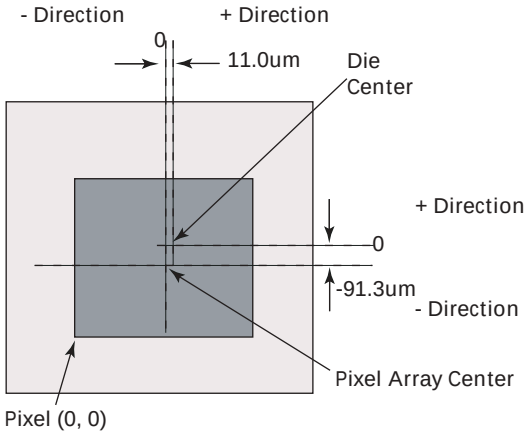


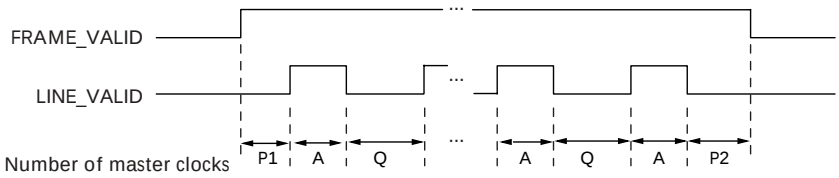
Figure 14: Die Center - Image CenterOffset



Note: Not to scale.

Appendix A – Sensor Timing

Figure 15: Row Timing and FRAME_VALID/LINE_VALID Signals



Note: The signals in Figure 15 are defined in Table 12.

Table 12: Frame Time

Parameter	Name	Equation (Master Clocks)	Default Timing At 12 MHz
A	Active Data Time	(Reg0x04 - 7) x 2	= 1,280 pixel clocks = 1,280 master clocks = 106.7us
P1	Frame Start Blanking	(Reg0x05 + 112) x 2	= 300 pixel clocks = 300 master clocks = 25.0us
P2	Frame End Blanking	14 CLKS	= 14 pixel clocks = 14 master clocks = 1.17us
Q	Horizontal Blanking	(Reg0x05 + 121) x 2 (MIN Reg0x05 value = 9)	= 318 pixel clocks = 318 master clocks = 26.5us
A + Q	Row Time	(Reg0x04 + Reg0x05 +114) x 2	= 1,598 pixel clocks = 1,598 master clocks = 133.2us
V	Vertical Blanking	(Reg0x06 + 9) x (A + Q) + (Q - P1 - P2)	= 20, 778 pixel clocks = 20,778 master clocks = 1.73ms
Nrows x (A + Q)	Frame Valid Time	(Reg0x03 - 7) x (A + Q) - (Q - P1 - P2)	= 767,036 pixel clocks = 767,036 master clocks = 63.92ms
F	Total Frame Time	(Reg0x03 + Reg0x06 + 2) x (A + Q)	= 787,814 pixel clocks = 787,814 master clocks = 65.65ms

Note: In order to avoid flicker, frame time is 65.65ms.

Sensor timing is shown above in terms of master clock cycle. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of Reg0x09) is less than the number of active row plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 13.

Table 13: Frame Time—Larger than One Frame

Parameter	Name	Equation (Master Clocks)	Default Timing
V'	Vertical Blanking (long integration time)	(Reg0x09 - Reg0x03) x (A + Q)	–
F'	Total Frame Time (long integration time)	(Reg0x09 + 1) x (A + Q)	–

Serial Bus Description

Registers are written to and read from the MT9V111 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9V111 through the serial data (SDATA) line. The SDATA line is pulled up to 2.8V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16 bits wide and can be accessed through 16-bit or eight-bit two-wire serial bus sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address. SADDR is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xB8.
- a(n) (no) acknowledge bit
- an eight-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V111 uses 16-bit data for its internal registers, thus requiring two eight-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and eight-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

The MT9V111 allows for eight-bit data transfers through the two-wire serial interface by writing (or reading) the most significant eight bits to the register and then writing (or reading) the least significant eight bits to Reg0x7F (127).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" in the least significant bit (LSB) of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xB8, while the read address is 0xB9; this only applies when SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

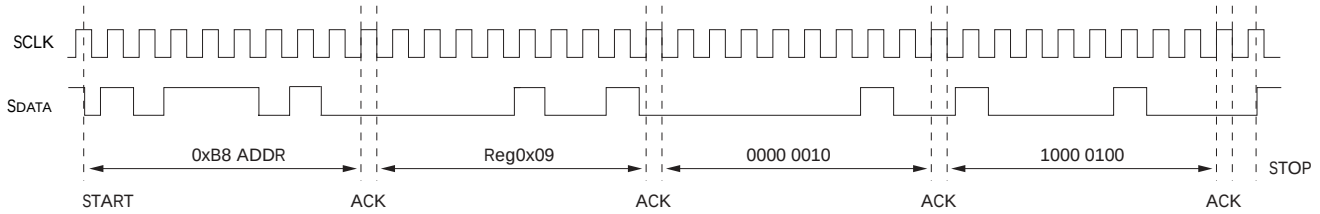
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-wire Serial Interface Sample Write and Read Sequences (with SADDR = 1)

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 16. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

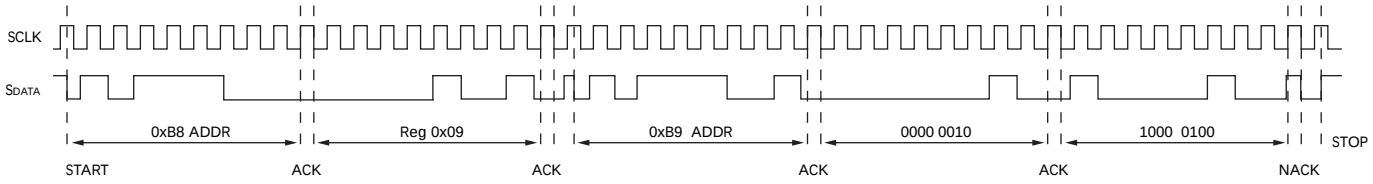
Figure 16: Timing Diagram Showing a Write to Reg0x09 with Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure . First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 17: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284

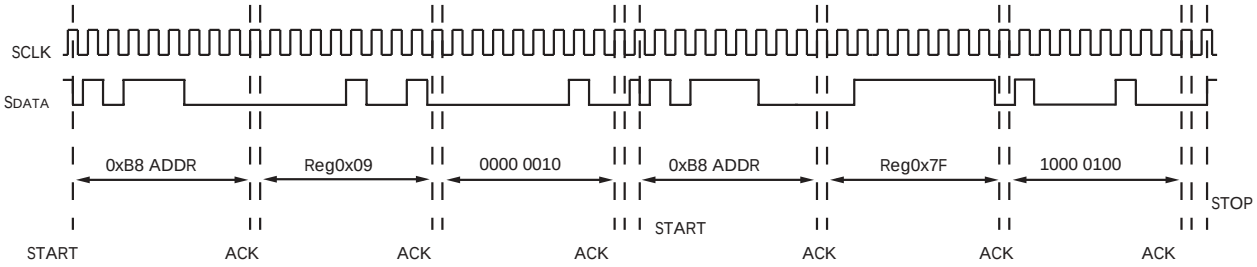


Eight-Bit Write Sequence

All registers in the camera are treated and accessed as 16-bit, even when some registers do not have all 16-bits used. However, certain hosts only support 8-bit serial communication access. The camera provides a special accommodation for these hosts.

To be able to write one byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (Reg0x7F). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 18, a typical sequence for 8-bit writing is shown. The second byte is written to the special register (Reg0x7F).

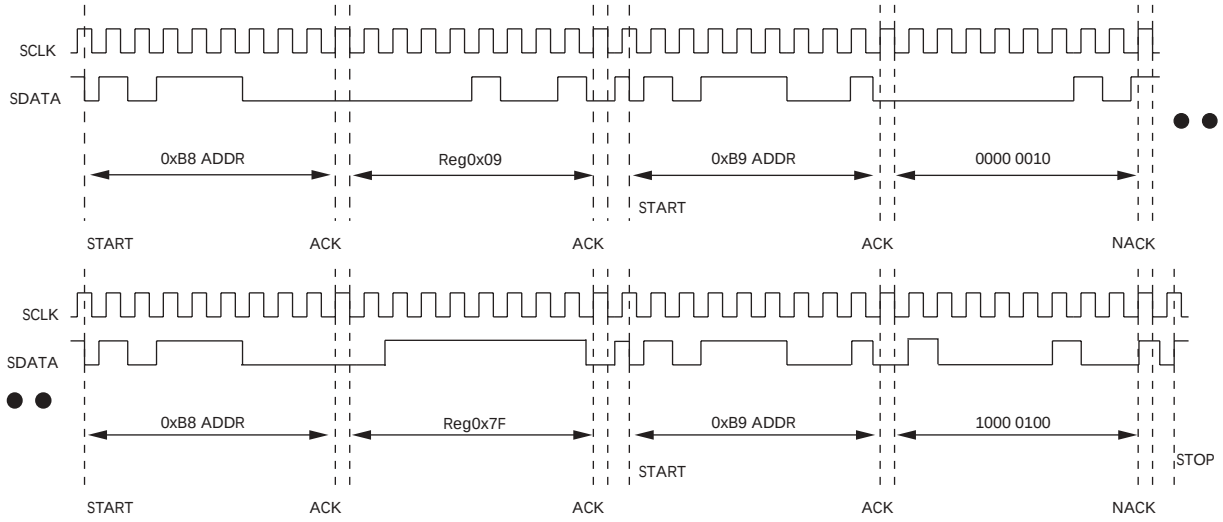
Figure 18: Timing Diagram Showing a Bytewise Write to Reg0x09 with Value 0x0284



Eight-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (Reg0x7F) the lower 8 bits are accessed, as shown in Figure 19 The master sets the no-acknowledge bits.

Figure 19: Timing Diagram Showing a Bytewise Read from Reg0x09; Returned Value 0x0284



Two-wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified below in master clock cycles.

Figure 20: Serial Host Interface Start Condition Timing

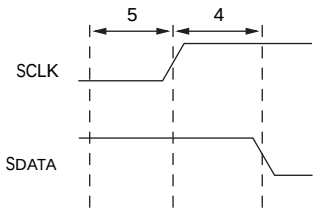
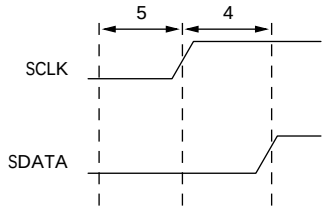
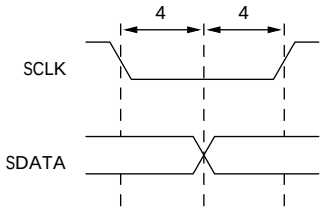


Figure 21: Serial Host Interface Stop Condition Timing



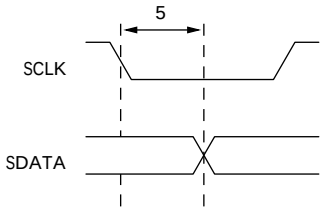
Note: All timing are in units of master clock cycle.

Figure 22: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 23: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 24: Acknowledge Signal Timing After an 8-bit Write to the Sensor

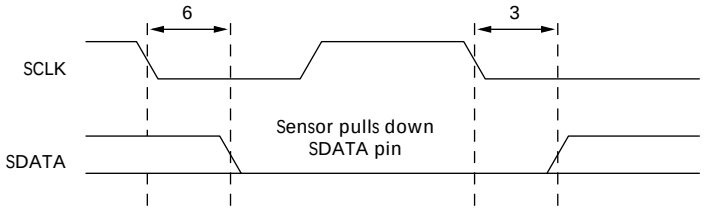
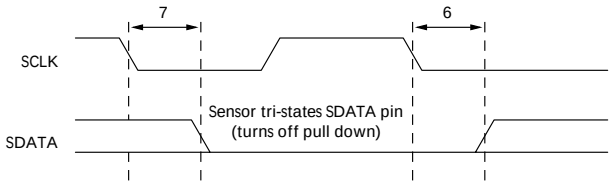


Figure 25: Acknowledge Signal Timing After an 8-bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Appendix B – Overview Of Programming

Default Sensor Configuration

In its default configuration, the sensor outputs up to 15 fps at 12 MHz master clock frequency. Auto exposure, automatic white balance, 60Hz flicker avoidance, defect correction, and automatic noise suppression in low light conditions are enabled. The frame rate is controlled by AE and can be slowed down to 5 fps in low light. Lens shading correction is disabled. Gamma correction uses gamma = 0.6. Image data are output in YCbCr ITU_R.BT.656 VGA format, with Y, Cb, and Cr values ranging from 16 to 240.

The use of the non-default register settings shown in Table 14 are recommended to optimize sensor performance in the above configuration.

Table 14: Non-Default Register Settings Optimizing 15 fps at 12 MHz Operation

Core:	R5 = 46, R7[4] = 0, R33 = 58369, R47 = 63414
IFP:	R51= 5137, R56 = 2168, R57= 290, R59 = 1068, R62 = 4095, R64 = 7696, R65 = 5143, R66 = 4627, R67 = 4370, R68 = 28944, R69 = 29811

Note: Non-default register settings required for an optimal 30 fps, 27 MHz operation are shown in Table 15

Table 15: Non-Default Register Settings Optimizing 30 fps at 27 MHz Operation

Core:	R5 = 132, R6 = 10, R7[4] = 0, R33 = 58369
IFP:	R51 = 5137, R57 = 290, R59 = 1068, R62 = 4095, R89 = 504, R90 = 605, R92 = 8222, R93 = 10021, R100 = 4477

Note: To obtain register settings for other frame rates and clock speeds, please contact a Micron FAE.

Auto Exposure

Target image brightness and accuracy of AE are set by IFP R46[7:0] and R46[15:8], respectively. For example, to overexpose images, set IFP R46[7:0] = 120. To change image brightness on LCD in RGB preview mode, use IFP R52[15:8]. AE logic can be programmed to keep the frame rate constant or vary it within certain range, by writing to IFP R55[9:5] one of the values tabulated in Table 16.

Table 16: Relation Between IFP R55[9:5] Setting and Frame Rate Range

Minimum Frame Rate	Maximum Frame Rate = 15 fps	Maximum Frame Rate = 30 fps
30 fps	N/A	4
15 fps	8	8
7.5 fps	16	16
5 fps	24	24

The speed of AE is set using IFP R47. The speed should be high in preview modes and lower for video output to avoid sudden changes in brightness between frames.

Auto exposure is disabled by setting IFP R6[14] = 0. When AE, AWB, and flicker avoidance are all disabled (IFP R6[14] = 0, IFP R6[1] = 0, and IFP R8[11] = 0), exposure and analog gains can be adjusted manually (see core registers R9, R12, and R43 through R46).

Automatic White Balance

AWB can be disabled by setting IFP R6[1]=0. Use IFP R37[2:0] and R37[6:3] to speed up AWB response. Please note that speeding AWB up may result in color oscillation. If necessary, AWB range can be restricted by changing the upper limit in IFP R36[14:8] and lower limit in IFP R36[6:0].

Flicker Avoidance

Use IFP R91 to choose automatic/manual, 50Hz/60Hz flicker avoidance and IFP R8[11] = 0 to disable this feature.

Flash

For flash programming, see IFP R152 description.

Decimation, Zoom, and Pan

For output decimation programming, see IFP R165 description. Table 17 provides a few examples.

Table 17: Decimation, Zoom, and Pan

Ifp Registers	CIF Output (Correct Aspect Ratio)	QVGA Output 2:1 Zoom	QVGA Output 1:1 Zoom
R165	26	160	0
R166	586	320	640
R167	352	320	320
R168	0	120	0
R169	480	240	480
R170	288	240	240

Note: For fixed 2x upsize zoom, set core R30[0] = 1.

Interpolation

Use IFP R5[2:0] to adjust image sharpness. By default, sharpness is automatically reduced in low-light conditions (see IFP R5[3]). For RGB565 16-bit capture, set IFP R6[12] = 0 and IFP R5[3] = 0 to avoid contouring.

Special Effects

To switch from color to gray scale output, set IFP R8[5] = 1. Contact a Micron FAE for register settings producing other special effects (e.g. sepia output).

Image Mirroring

To mirror images horizontally, set core R32[14] = 1 and IFP R8[0] = 1. To flip images vertically, set core R32[15] = 1 and IFP R8[1] = 1.

Test Pattern

See IFP R72 and IFP Reg58[5:3] description.

Gamma Correction

See Table 18 and Table for register settings required to setup non-default gamma correction. Please note that these settings determine output signal range. Use YCbCr settings with ITU_R BTU-compatible devices. Use YUV settings for JPEG capture and RGB preview; switching to YUV mode requires setting IFP R52 = 0 and IFP R53 = 65281.

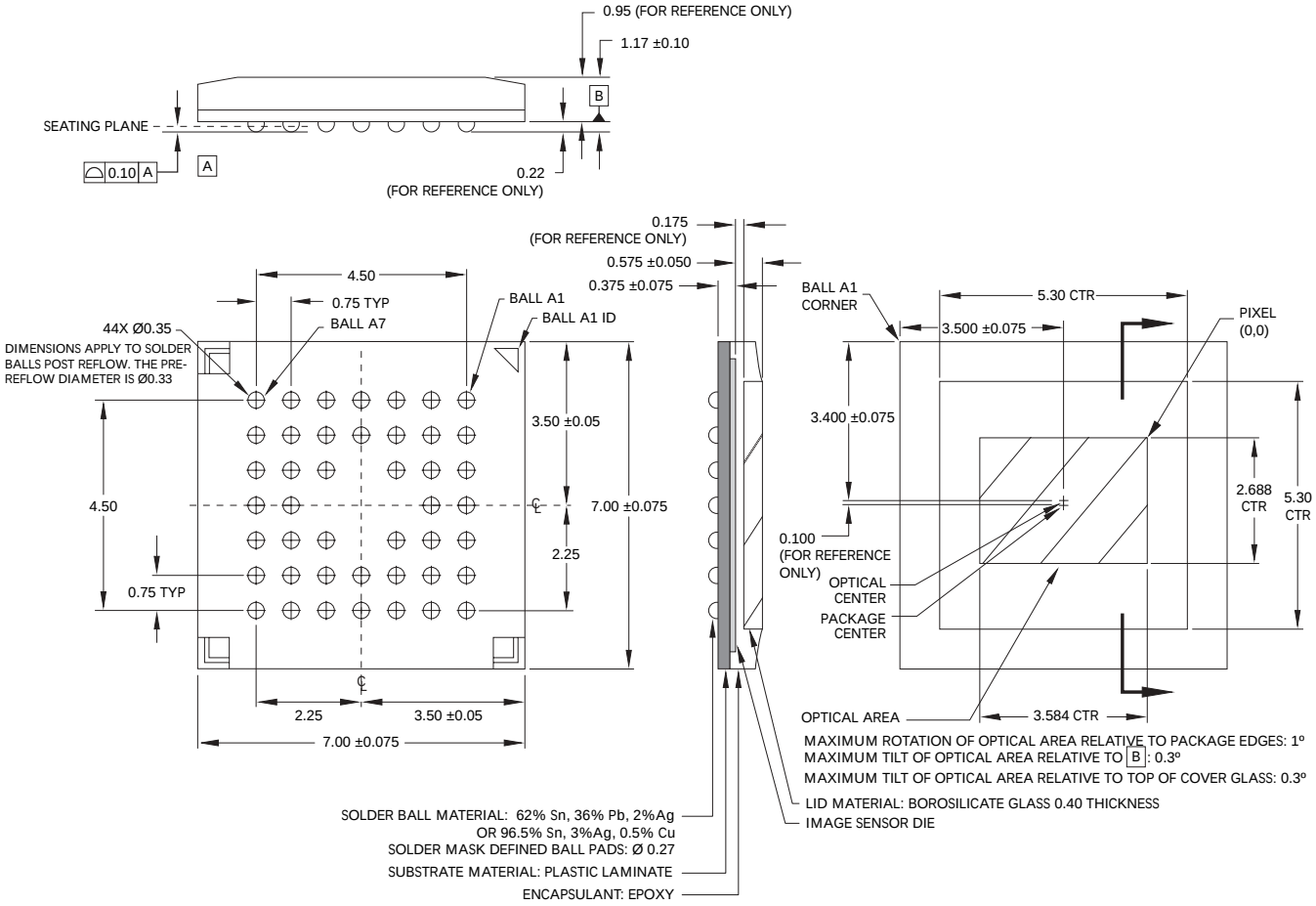
Table 18: YCbCr Settings

Gamma	0.45	0.5	0.55	0.6 (Default)	0.7	1.0
IFP R83	12836	10781	8984	7700	5389	2052
IFP R84	23876	21563	19508	17709	14627	8208
IFP R85	39039	37495	35952	34409	31581	24640
IFP R86	49326	48553	47780	47008	45207	41088
IFP R87	57552	57551	57549	57548	57545	57536

Table 19: YUV Settings

Gamma	0.45	0.5	0.55	0.6	0.7	1.0
IFP R83	14377	12321	10267	8726	6159	2308
IFP R84	26957	24643	22331	20276	16680	9234
IFP R85	44432	42631	40831	39031	35945	27720
IFP R86	56005	54976	54202	53173	51371	46481
IFP R87	65260	65259	65257	65255	65252	65241

Figure 26: 44-Ball ICSP Package Outline Drawing



Notes: 1. All dimensions in millimeters.
2. ICSP package information is preliminary.

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Revision History

Rev. G, Production 1/05

- Modified ^{t}OH definition in Table 11, AC Electrical Characteristics, on page 31
- Updated Figure 10, Propagation Delays for PIXCLK and Data Out Signals, on page 32

Rev. F, Production 8/04

- Updated 44-Ball ICSP Package Outline Drawing

Rev. E 7/04

- Replaced 28-Pin PLCC package information with the 44-Ball ICSP
- Updated Table 12 (Frame Time)
- Updated Electrical Specifications

Rev. D, Preliminary 3/04

- Modify for external web posting - streamlined register descriptions
- Add Appendix B

Rev. C, Preliminary 2/04

- Added Key Performance Parameter Table, Update Register Tables, Update Electrical Specification Table, Added Figures (Image Center Offset, Die Placement, 28-Pin PLCC Package Outline Drawing and Spectral Response)

Rev. B, Preliminary, Draft 1/04

- Format edits on 1/15/04

Rev. A, Preliminary, Draft 12/03

- Initial Release of document