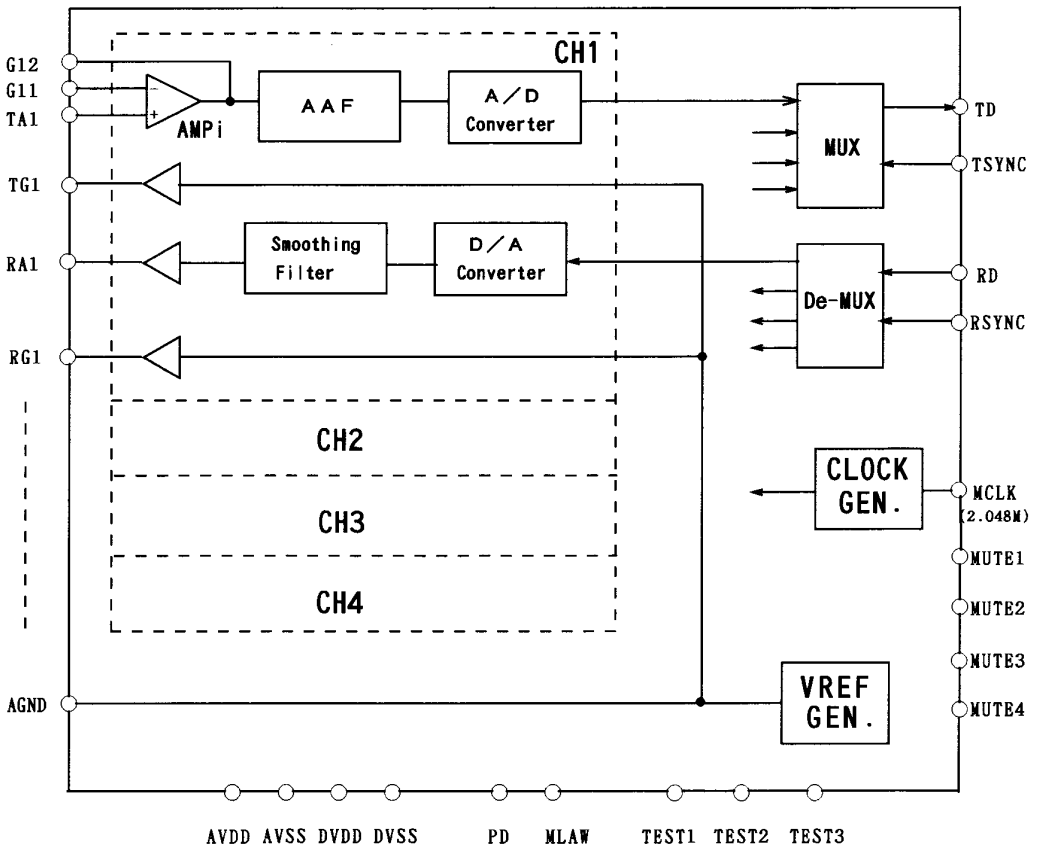
AK2304A

QUAD PCM CODEC/FILTER COMBO LSI

Features

- ☐ Compliant to AT&T and ITU recommendations
- ☐ Monolithic 4-channel CODEC/Filter
- ☐ Suitable for PBX/KTS applications
- ☐ A-law/μ-law pin selectable
- ☐ Integrated op-amps for input gain adjustment
- ☐ Integrated anti-alias filter
- ☐ 2.048Mb/s PCM data output
- ☐ Individual channel mute function
- ☐ Power down mode
- ☐ Single 5 volt operation
- ☐ 44 pin QFP package

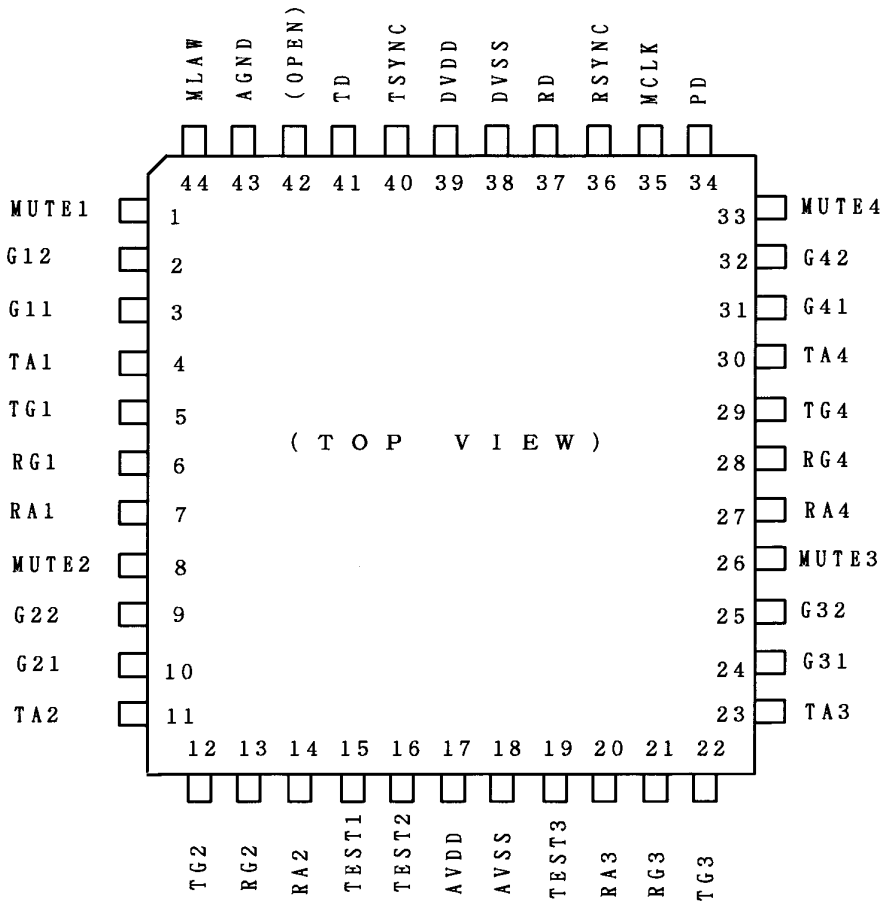
Block Diagram



General Description

The AK2304A is an integrated monolithic quad PCM CODEC for PBX/KTS applications, which integrates band limiting filters, ADCs, DACs and A-law/μ-law compressor/expander.
The device can be set to either A-law or μ-law companding by pin selection.

■ Pin assignment



■ Ordering information

AK2304A	-40～+85℃	44pin QFP
AKD2304	Evaluation board	

Circuit Description

Block	Function
AMP1～4	Op-amps for input gain adjustment. AK2304A has an op-amp at each analog input (CH1～CH4). Normally, this op-amp is used as an inverting amplifier. Adjusting the gain up to +12dB with external resistors. The resistor larger than 50kΩ is recommended for the feedback resistor. This op-amp can be also used as a differential amplifier, but it cannot be used as a non-inverting amplifier. As for the recommended value of external resistors and capacitors, see section "Application circuit example".
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voiceband. AAF is a 2nd order low-pass filter and it provides typically -40dB gain at the sampling frequency.
A/D Converter	Converts analog signal to 8 bit PCM data according to the companding schemes of CCITT recommendation G.711; A-Law or μ-Law. The band limiting filter is also integrated. The selection of companding schemes is set by MLAW pin as follows: "H"[1]: μ-Law "L"[1]: A-Law
MUX	8 bit PCM data from CH1 to CH4 (8bit * 4CH = 32 bit) is muxed into serial data of 2.048Mb/s on the rising edges of MCLK and comes out from TD. The start bit of transmit PCM data is defined by TSYNC. This 3-state output remains in the high impedance state except during the assigned transmit time slot. As for the transmit data timing, see section "Transmit Timing Diagrams".
De-MUX	Received serial PCM data (8bit * 4CH) from RD at the rate of 2.048Mb/s on the falling edges of MCLK is de-muxed into 4CH serial data. The start bit of receive PCM data is defined by RSYNC. The received data is divided into 8bit blocks and sent to CH1 to CH4 sequentially. As for the receive data timing, see section "Receive Timing Diagrams".
D/A Converter	Expands 8bit PCM data according to A-Law or μ-Law and reconstructs a staircase form of analog signal. The selection of companding schemes is set by MLAW pin as follows: "H": μ-Law "L": A-Law
Smoothing Filter	The filter for attenuating the harmonic components from D/A output and extracts the desired inband signal. It also corrects the sinx/x effect of D/A output.
VREF GEN.	Provides the stable analog ground voltage (2.4V) using an on-chip band-gap reference circuit which is temperature compensated.

Note-1: "H" refers to high level digital signal.
"L" refers to low level digital signal.

Pin / Function

Pin #	Name	I/O	Function	Remarks
1	MUTE1	I	Mute for CH1. When set "H", CH1 goes into mute mode. CH1 output from TD goes to high impedance and RA1 output goes to analog ground level.	
2	G12	O	Output of AMP1.	Note-1
3	G11	I	Inverting input of AMP1.	Note-1
4	TA1	I	Non-inverting input of AMP1.	Note-1
5	TG1	O	Analog ground for CH1 analog output. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
6	RG1	O	Analog ground for CH1 analog input. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
7	RA1	O	CH1 analog output. This output can drive 10kΩ or larger, and 50pF or smaller.	
8	MUTE2	I	Mute for CH2. When set "H", CH2 goes into mute mode. CH2 output from TD goes to high impedance and RA2 output goes to analog ground level.	
9	G22	O	Output of AMP2.	Note-1
10	G21	I	Inverting input of AMP2.	Note-1
11	TA2	I	Non-inverting input of AMP2.	Note-1
12	TG2	O	Analog ground for CH2 analog output. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
13	RG2	O	Analog ground for CH2 analog input. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
14	RA2	O	CH2 analog output. This output can drive 10kΩ or larger, and 50pF or smaller.	
15	TEST1	I	Test pin reserved for factory use. When "H", this device goes into test mode. Tie to DVSS for normal operation.	
16	TEST2	I	Test pin reserved for factory use. When "H", this device goes into test mode. Tie to DVSS for normal operation.	
17	AVDD	-	Power supply for analog section.	
18	AVSS	-	Ground for analog section.	
19	TEST3	I	Test pin reserved for factory use. When "H", this device goes into test mode. Tie to DVSS for normal operation.	
20	RA3	O	CH3 analog output. This output can drive 10kΩ or larger, and 50pF or smaller.	

Pin #	Name	I/O	Function	Remarks
21	RG3	O	Analog ground for CH3 analog input. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
22	TG3	O	Analog ground for CH3 analog output. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
23	TA3	I	Non-inverting input of AMP3.	Note-1
24	G31	I	Inverting input of AMP3.	Note-1
25	G32	O	Output of AMP3.	Note-1
26	MUTE3	I	Mute for CH3. When set "H", CH3 goes into mute mode. CH3 output from TD goes to high impedance and RA3 output goes to analog ground level.	
27	RA4	O	CH4 analog output. This output can drive 10kΩ or larger, and 50pF or smaller.	
28	RG4	O	Analog ground for CH4 analog input. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
29	TG4	O	Analog ground for CH4 analog output. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
30	TA4	I	Non-inverting input of AMP4.	Note-1
31	G41	I	Inverting input of AMP4.	Note-1
32	G42	O	Output of AMP4.	Note-1
33	MUTE4	I	Mute for CH4. When set "H", CH4 goes into mute mode. CH4 output from TD goes to high impedance and RA4 output goes to analog ground level.	
34	PD	I	Power down. When "H", this device goes into power down mode. TD output and RA1 to RA4 output go to high impedance.	
35	MCLK	I	Master clock 2.048MHz input.	
36	RSYNC	I	Receive frame sync input. Input 8kHz clock to define the start bit of the receive time slot.	
37	RD	I	2.048Mb/s PCM data input. The 32bit (8bit * 4CH) received PCM data is shifted in on the falling edges of MCLK. The start bit of received PCM data is defined by RSYNC.	
38	DVSS	-	Ground for digital section.	
39	DVDD	-	+5V ± 5% Power supply for digital section.	
40	TSYNC	I	Transmit frame sync input. Input 8kHz clock to define the start bit of the transmit time slot.	

Pin #	Name	I/O	Function	Remarks
41	TD	O	PCM data output at 2.048Mb/s. The 32bit (4CH * 8bit) serial transmit PCM data is shifted out on the rising edges of MCLK. The start bit of transmit PCM data is defined by TSYNC. This 3-state output remains in the high impedance state except during the assigned transmit time slot.	
42	NC	-	No connection (Left open).	Note-2
43	AGND	O	Analog ground output. To stabilize the analog ground, connect to AVSS with 4.7μF or larger.	
44	MLAW	I	Companding schemes selection. "H": μ-Law "L": A-Law	

Note-1: Normally, form the inverting amplifier with external resistors for gain adjustment. For more information, see section "Circuit Description" and "Application Circuit Examples".
Note-2: This pin is used as the digital output during test mode.

Absolute Maximum Ratings

Parameter	Symbol	min	max	units
Power Supply Voltages (Note-1, 2)				
Digital Power Supply	DVDD	-0.3	6.5	V
Analog Power Supply	AVDD	-0.3	6.5	V
Digital Input Voltage (Note-1)	VIND	-0.3	AVDD+0.3	V
Analog Input Voltage (Note-1)	VINA	-0.3	AVDD+0.3	V
Storage Temperature	Tstg	-55	125	℃

Note-1: AVSS=DVSS=0V, all voltages with respect to ground.
Note-2: When DVDD exceeds AVDD, permanent damage may be caused to the device.

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	units
Power Supply Voltage (Note-1)					
Digital Power Supply	DVDD	4.75	5.0	5.25	V
Analog Power Supply	AVDD	4.75	5.0	5.25	V
Ambient Operating Temperature	Ta	-40		85	℃

Note-1: AVSS=DVSS=0V, all voltages with respect to ground.

Electrical Characteristics

Unless otherwise noted, guaranteed for AVDD = DVDD = +5V±5%, Ta = -40～+85℃.

■ DC characteristics

Parameter	Symbol	conditions	min	typ	max	units
Power Consumption	IDD	Normal operation supplying MCLK No load at all output pins		15	20	mA
		Power down mode. No load at all output pins (Note-1)		1	10	μA
Input Leak	Ii				±10	μA
"H" Output Level	VOH	IOH=-2mA	DVDD-1			V
"L" Output Level	VOL	IOL=2mA			0.4	V
"H" Input Level	VIH	(Note-2)	2.0			V
"L" Input Level	VIL	(Note-2)			0.8	V

Note-1: Connect PD pin to DVDD and connect the others digital input to DVSS
Note-2: Except test pins

■ Analog Characteristics

Parameter	Conditions		min	typ	max	units
Signal to Total Distortion (A → A)	1020Hz Sinusoidal test with C-message	-45dBm0	23	–	–	dB
		-40dBm0	28	–	–	
		0, -30dBm0	34	–	–	
Gain Tracking (A → A)	Reference Level -10dBm0@1020Hz Sinusoidal test	-55dBm0	-1.0	–	1.0	dB
		-50dBm0	-0.5	–	0.5	
		3, -40dBm0	-0.3	–	0.3	
Analog Input Level	Input: 0dBm0 @ 1020Hz			0.849		Vrms
Analog Output Level	Input: 0dBm0 @ 1020Hz Code			0.849		Vrms
TX Gain, Absolute	0dBm0@1020Hz		-0.6	–	0.6	dB
RX Gain, Absolute			-0.6	–	0.6	dB
Idle Channel Noise A → D (Note-1)	μ-law, with C-message		–	5	10	dBrnC0
	A-law, with P-message		–	-85	-80	dBm0p
Idle Channel Noise D → A (Note-2)	μ-law, with C-message		–	5	10	dBrnC0
	A-law, with P-message		–	-85	-80	dBm0p
Crosstalk between Channels (Note-3)	A to A, Input: 0dBm0@1020Hz		–	-90	-82	dB
Frequency Response (A → D)	Input: 0 dBm0 Relative to 0dBm0@1020Hz	0.06kHz	24	–	–	dB
		0.2kHz	0	–	2.5	
		0.3～3.0kHz	-0.15	–	0.15	
		3.4kHz	0	–	0.8	
		3.78kHz	6.5	–	–	
Frequency Response (D → A)	Input: 0 dBm0 Relative to 0dBm0@1020Hz	0～3.0kHz	-0.15	–	0.15	dB
		3.4kHz	0	–	0.8	
		3.78kHz	6.5	–	–	
Spurious Out-of-Band Signals (Note-4)	Input: 0 dBm0, 300Hz～3400Hz PCM Code	4.6k～7.6kHz			-30	dB
		7.6k～8.4kHz			-40	
		8.4k～50kHz			-30	
PSRR (A → A)	AVDD=DVDD= 5.0V ± 100mVop f=300Hz～100kHz		–	45	–	dB
Delay, Absolute (Note-4)	A→D, f=1300Hz		–	290	300	μs
	D→A, f=1300Hz		–	180	230	

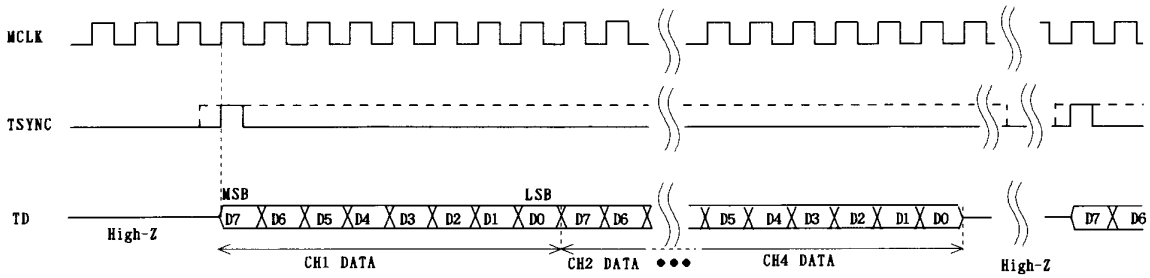
Note-1: Analog input = Analog ground
Note-2: Digital input (RD) = +0 Code
Note-3: Measured with 4.7μF capacitor between AGND, TGi, RGi, and AVSS respectively.
Note-4: Not tested in production test.
Parameters guaranteed by design and characterization.

■ Switching Characteristics (Refer to Timing Diagrams)

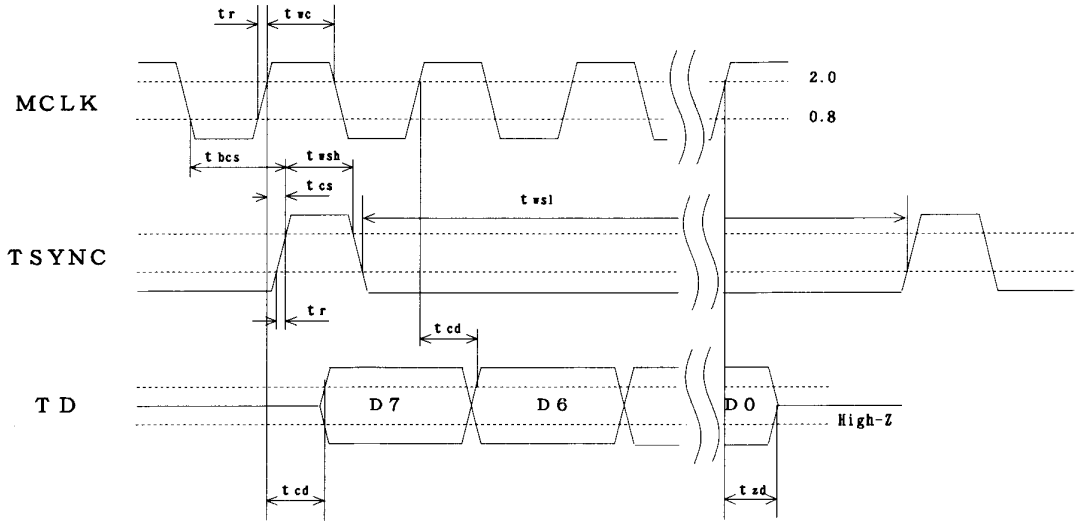
Parameter	Symbol	min	typ	max	units
Master Clock Frequency	MCLK		2.048		MHz
Rise Time of Digital Input(Note-3)	tr	5.0	–	50	ns
Fall Time of Digital Input(Note-3)	tf	5.0	–	50	ns
Clock Pulse Width	twc	195	244	293	ns
Transmitter Side Timing					
TSYNC High Period	twsh	200	–	–	ns
TSYNC Low Period	twsl	8	–	–	μs
Hold Time from MCLK rising edge to TSYNC	tcs	–	–	100	ns
Hold Time from MCLK falling edge to TSYNC	tbcs	0	–	–	ns
Delay Time from MCLK rising edge to Data Valid (Note-1)	tcd	–	–	180	ns
Delay Time from MCLK rising edge to High-Z (Note-2,3)	tzd	–	–	30	ns
Receiver Side Timing					
RSYNC High Period	twsh	200	–	–	ns
RSYNC Low Period	twsl	8	–	–	μs
Hold Time from MCLK rising edge to RSYNC	tcs	–	–	100	ns
Hold Time from MCLK falling edge to RSYNC	tbcs	0	–	–	ns
Set-up Time from RD Valid to MCLK falling edge	tsu	65	–	–	ns
Hold Time from MCLK falling edge to RD Invalid	thd	120	–	–	ns

Note-1: Measured with 50pF.
Note-2: With no load capacitance.
Note-3: Not tested in production test.
Parameters guaranteed by design and characterization.

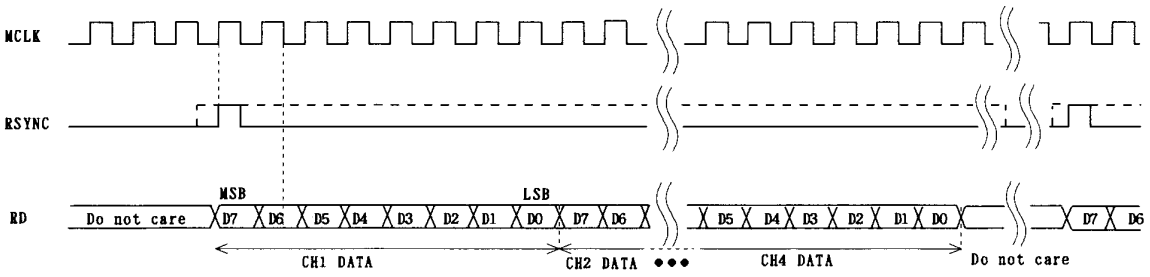
Transmit Timing Diagrams



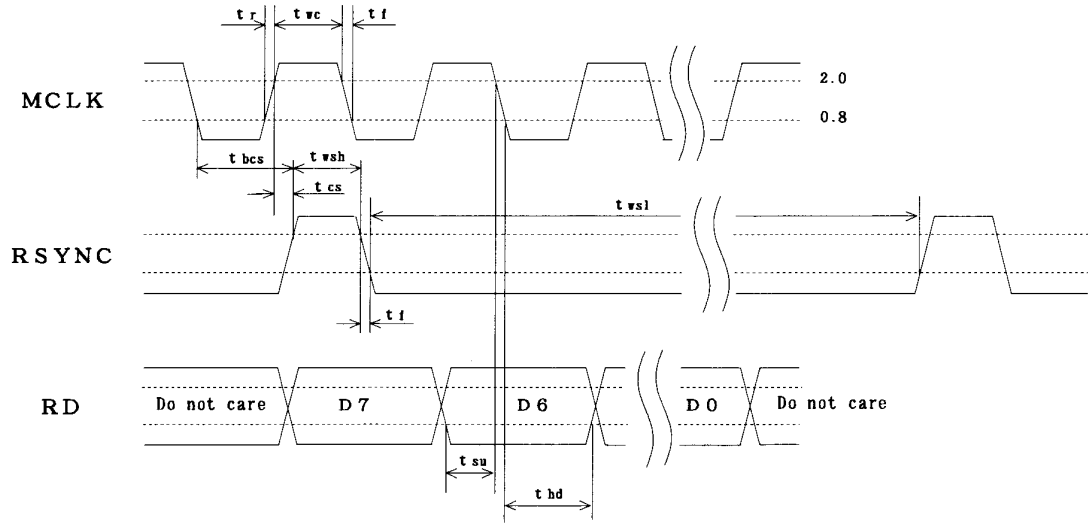
Note: As for TSYNC timing, refer to t_{bcs}, t_{cs} and t_{wsl} of Timing Diagrams below.



Receive Timing Diagrams



Note: As for RSYNC timing, refer to t_{bcs}, t_{cs} and t_{wsl} of Timing Diagrams below.



Application Circuit Examples

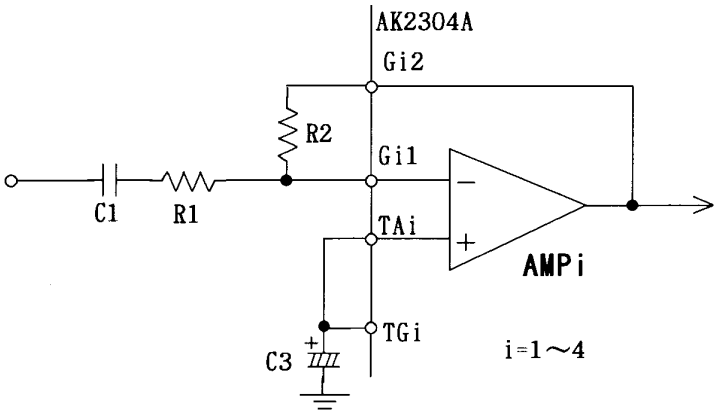
1. Analog input circuit (AMP1～AMP4)

AK2304A has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment.

Op-amp can be used as an inverting amplifier or a differential amplifier, but not as a non-inverting amplifier.

Where, Gain: 12dB or smaller, Feedback resistor: 50kΩ or larger

(Circuit example as inverting amplifier)

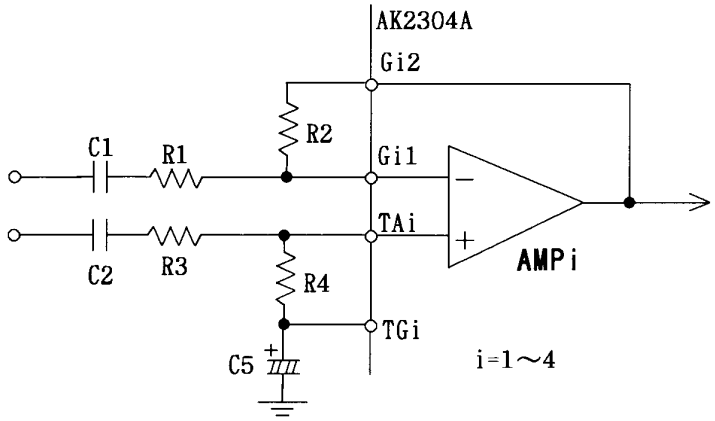


Components values for 0dB gain

C1=0.47μF, C2=56pF, C3=4.7μF, Cn=1500pF

R1=R2=56kΩ

(Circuit Example as differential amplifier)



Components values for 0dB gain

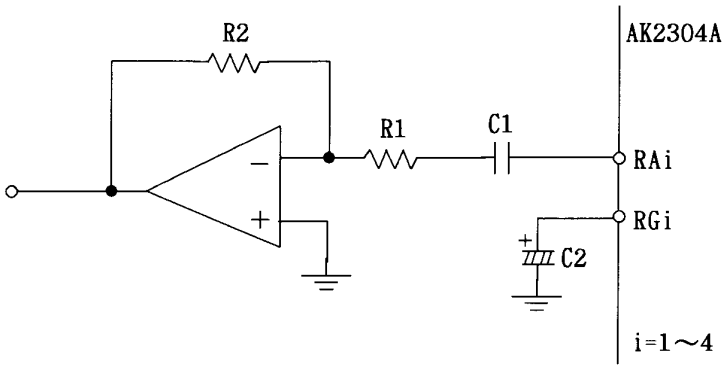
C1=C2=0.47μF, C3=C4=56pF, C5=4.7μF, Cn=1500pF

R1=R2=R3=R4=56kΩ

2. Analog output circuit

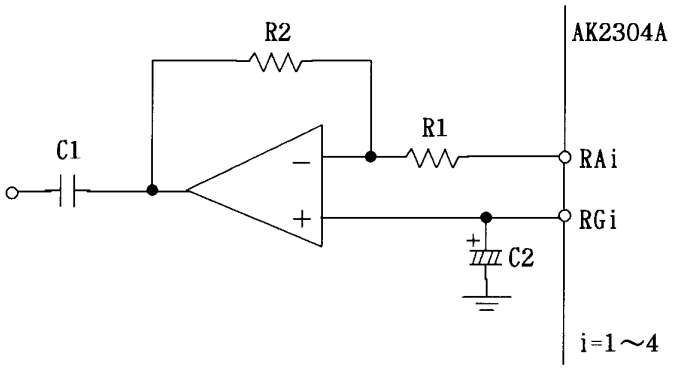
Each AK2304A analog output can drive 10kΩ or larger, and 50pF or smaller. To drive 10kΩ or smaller loads, use external op-amps. Since AK2304A analog output is biased, form a high pass filter if necessary.

(Circuit example used inverting amplifier)



Components values for 0dB gain
C1=0.47μF, C2=4.7μF
R1=R2=33kΩ

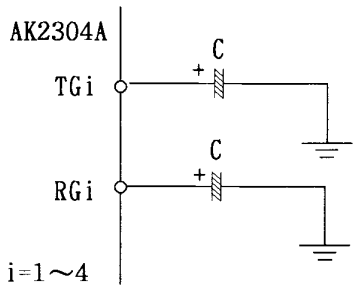
(Circuit example used single power supply op-amp)



Components values for 0dB gain
C1=0.47μF, C2=4.7μF
R1=R2=33kΩ

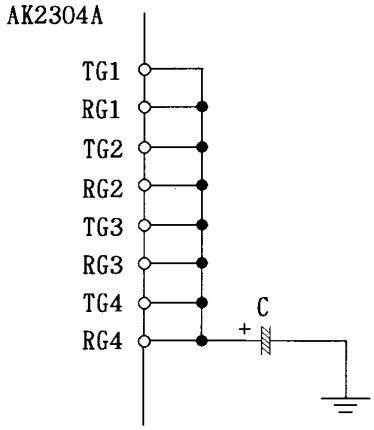
3. Analog ground stabilization capacitor

To stabilize each analog ground (TGi and RGi, i=1～4), connect to AVSS through 4.7μF or larger capacitor.



C=4.7μF

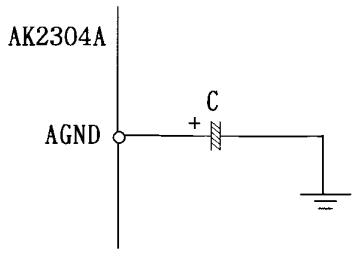
When connecting all analog ground to AVSS through only one capacitor, connect to AVSS through 47μF or larger capacitor, as shown below. This method could result in higher cross-talk than in above circuit.



C=47μF

4. Analog reference voltage stabilization capacitor

To stabilize the reference voltage (analog ground), connect 4.7μF or larger capacitor between AGND and AVSS.

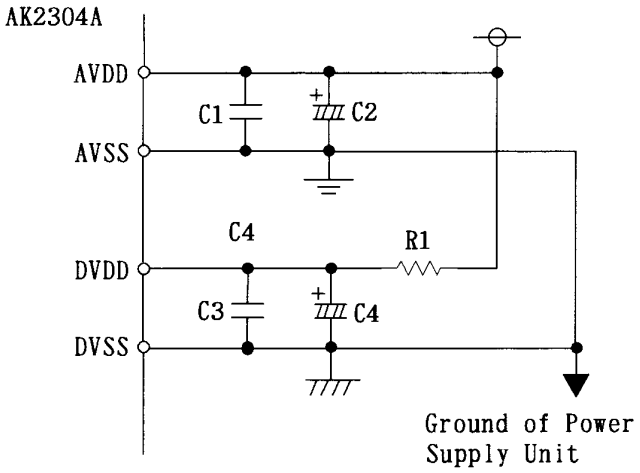


C=4.7μF

5. Power Supply

To use the same supply for both digital and analog power supply (DVDD and AVDD), insert 10Ω resistor between AVDD and DVDD, and separate analog VSS and digital VSS and connect them at power supply unit.

To attenuate the power supply noise, connect capacitors between AVDD and AVSS, and DVDD and DVSS, as shown below.



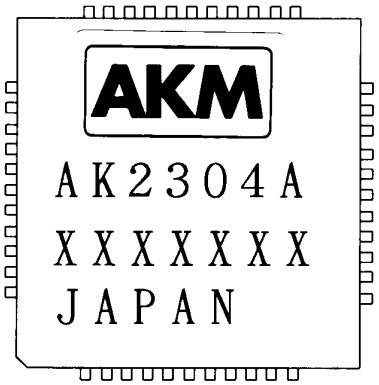
C1=C3=0.1μF
C2=C4=100μF
R1=10Ω

Packaging Information

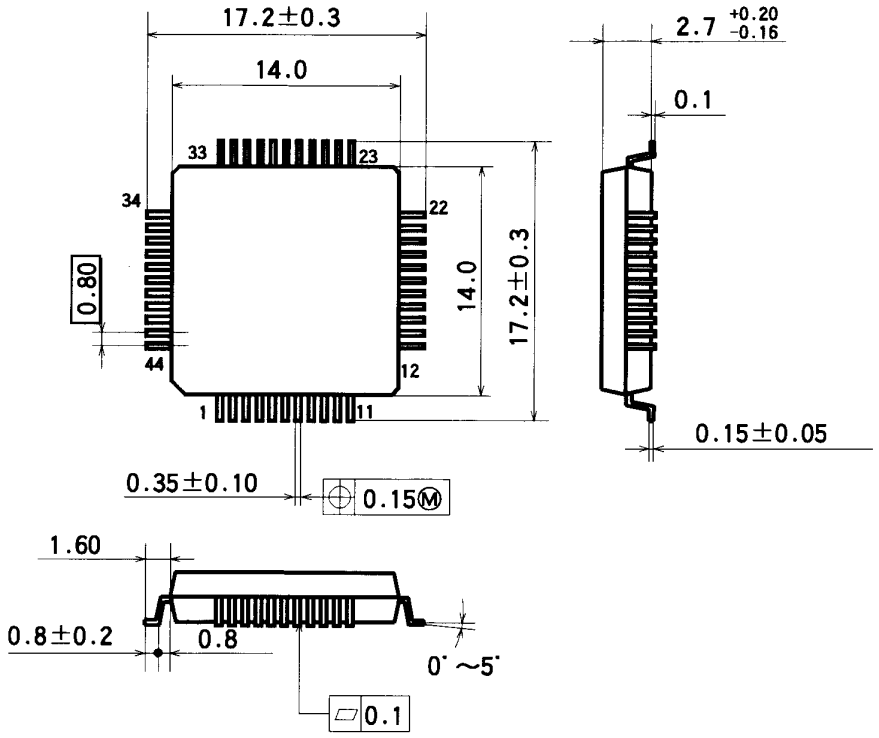
☐ 44 Pin QFP

■ Marking

(1) Pin # 1 indication
(2) Date Code: 7 Digits XXXXXXX
(3) Marketing Code: AK2304A
(4) Country of Origin: JAPAN
(5) Asahi Kasei Logo



■ Outline Dimensions



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