### 1.1 Scope.

This specification covers the detail requirements for a hybrid, buffered, digital-to-analog converter with voltage output.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

| Device | Part Number |
|---|---|
| −1 | AD3860SD/883B |

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-24B.

### 1.3 Absolute Maximum Ratings. ($T_A$ = +25°C unless otherwise noted)

Single Voltage $+V_S$ ..... +18 V max
$-V_S$ ..... −18 V max
$+V_{LOGIC}$ ..... +7 V max
$V_{IN}$ Digital $V_{INL}$ ..... 0 to $+V_{LOGIC}$
Short Circuit Protection to GND ..... Continuous
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

### 1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC}$ = 8°C/W
$\theta_{JA}$ = 25°C/W

# AD3860 – SPECIFICATIONS

| Test | Symbol | Device | Design Limit @ +25°C (−55°C to +125°C) | Sub Group 1 | Sub Group 2, 3 | Sub Group 4 | Test Condition[1] | Units |
|---|---|---|---|---|---|---|---|---|
| Digital Input High Voltage | $V_{IH}$ | −1 | 2.0 (2.0) | | | | | V min |
| Digital Input Low Voltage | $V_{IL}$ | −1 | 0.8 (0.8) | | | | | V max |
| Digital Input High Current | $I_{IH}$ | −1 | 30 (30)<br>60 (60) | | | 30 | Data Inputs @ 2.0 V<br>Register Input @ 2.0 V | μA max |
| Digital Input Low Current | $I_{IL}$ | −1 | 600 (600)<br>1200 (1200) | | | 600 | Data Inputs @ 0.8 V<br>Register Enable @ 0.8 V | μA max |
| Gain Error | $A_E$ | −1 | 0.1 | 0.1 | | | $V_O$ = +FS, ±10 V Range | ±% FSR max |
| Gain Error Temperature Coefficient | $TCA_E$ | −1 | (0.3) | | 0.3 | | $V_O$ = +FS, ±10 V Range | ±% FSR max |
| Unipolar Gain Error | $V_{UGE}$ | −1 | 0.1 | 0.1 | | | $V_O$ = +FS<br>0 to 10 V Range | ±% FSR max |
| Unipolar Gain Drift | $V_{UGD}$ | −1 | (0.3) | | 0.3 | | $V_O$ = +FS<br>0 to 10 V Range | ±% FSR max |
| Unipolar Offset Error | $V_{OS}$ | −1 | 0.05 | 0.05 | | | $V_O$ = 0 V, +10 V Range | ±% FSR max |
| Unipolar Offset Error Temperature Coefficient | $TCV_{OS}$ | −1 | (0.1) | | 0.1 | | Over Operating Temperature | ±% FSR max |
| Bipolar Gain Error | $V_{BGE}$ | −1 | 0.1 | 0.1 | | | $V_O$ = +FS, ±10 V Range | ±% FSR max |
| Bipolar Gain Drift | $V_{BGD}$ | −1 | (0.3) | | 0.3 | | $V_O$ = +FS, ±10 V Range | ±% FSR max |
| Bipolar Offset Error | $B_{POS}$ | −1 | 0.05 | 0.05 | | | $V_O$ = −FS, ±10 V Range | ±% FSR max |
| Bipolar Offset Error Temperature Coefficient | $TCB_{POS}$ | −1 | (0.1) | | 0.1 | | $V_O$ = −FS, ±10 V Range | ±% FSR max |
| Bipolar Zero Error | $B_{PZ}$ | −1 | 0.1 | | | | $V_O$ = 0 V, ±10 V Range | ±% FSR max |
| Bipolar Zero Error Temperature Coefficient | $TCP_{PZ}$ | −1 | (0.3) | | | | $V_O$ = 0 V, ±10 V Range | ±% FSR max |
| Integral Nonlinearity | $L_E$ | −1 | 1/2 (1/2) | 1/2 | 1/2 | | Linearity ±10 V Range | ±LSB max |
| Differential Nonlinearity Error | $D_{LE}$ | −1 | 1 (1) | 1 | 1 | | Monotonic Over Temperature | ±LSB max |
| Output Voltage Range, Ideal | $V_{OUT}$ | −1 | +9.9952<br>(9.9952)<br>−10.000<br>(−10.000) | | | | ±10 V Range | V Ideal |
| Output Current | $I_{OUT}$ | −1 | 5.0 (5.0) | | | 5.0 | ±10 V Range<br>$C_L$ = 250 pF, $R_L$ = 2 kΩ | mA min |
| Input Resistance | $R_{IN}$ | −1 | N/A | | | | | |
| Reference Output Voltage Error | $V_{REFER}$ | −1 | 126<br>126 | 126<br>126 | | | Error @ No Load<br>Error @ 2.5 mA Load | ±mV max |
| Reference Output Voltage[2] Temperature Coefficient | $TCV_{REF}$ | −1 | (126)<br>(126) | | 126<br>126 | | Error @ No Load<br>Error @ 2.5 mA Load | ±mV max |
| Reference Output Current | $I_{REF}$ | −1 | 2.5 | | | | For External Use | mA min |
| Slew Rate | $V_{SL}$ | −1 | 10 (10) | | | | ±10 V Range | V/μs min |
| Output Voltage Settling Time | $t_{SL}$ | −1 | 7 (7)<br>5 (5) | | | | ±10 V Range, 20 V Step<br>±5 V Range, 10 V Step | μs max |
| DC Feedthrough Error | FTE | −1 | 1 | 1 | | | Latch @ +FS then Change to Offset | ±mV max |
| DC Feedthrough Error Over Temperature | TCFTE | −1 | (1) | | 1 | | Latch @ +FS then Change to Offset | ±mV max |

*Table 1. (Continued on next page)*

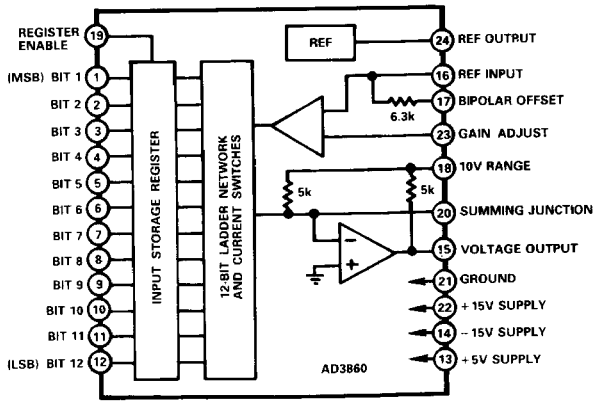
REV. C

| Test | Symbol | Device | Design Limit @ +25°C (−55°C to +125°C) | Sub Group 1 | Sub Group 2, 3 | Sub Group 4 | Test Condition[1] | Units |
|---|---|---|---|---|---|---|---|---|
| Output Short Circuit Current | $I_{SC}$ | −1 | 25 (25) | | | | | mA max |
| Power Supply Rejection Ratio | PSRR | −1 | 0.01<br>0.004 | 0.01<br>0.004 | 0.01<br>0.004 | | +15 V, ±0.5 V<br>−15 V, ±0.5 V | ±% FSR/% $V_S$ max |
| Power Supply Current | $I_{CC}$<br>$I_{EE}$<br>$I_{DD}$ | −1 | +20 (+20)<br>−30 (−30)<br>+50 (+50) | +20<br>−30<br>+50 | +20<br>−30<br>+50 | | +15 $V_{CC}$<br>−15 $V_{EE}$<br>+5 $V_{LOGIC}$ | mA max |
| Power Dissipation | $P_D$ | −1 | 1000 (1000) | | | | | mW max |
| Write Pulse Width | $t_{NEPW}$ | −1 | 60 | | | | | ns min |
| Data Setup Time | $t_{SDE}$ | −1 | 40 | | | | | ns min |
| Data Hold Time | $t_{DH}$ | −1 | 10 | | | | | ns min |

NOTES
[1]Specified and tested at +25°C, ±15 V, +5 V, ±10 V range, no load conditions, internal reference unless noted otherwise in the table.
[2]$V_{REF}$ = +6.300 V.

*Table 1.*

### 3.2.1 Functional Block Diagram and Terminal Assignments.

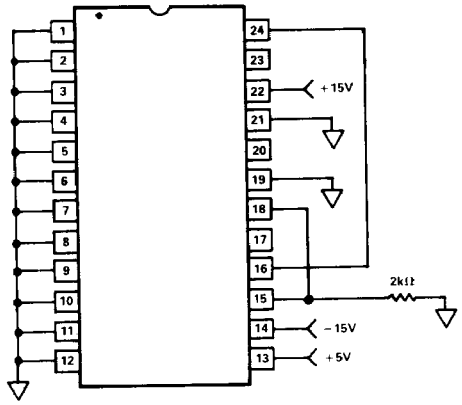



### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



### 6.0 Output Range.

The analog input range is as specified in Table 2 when externally connected as shown in Table 3 below. The output range must be limited to ±5 V full scale when operated with ±12 V supplies.

**OUTPUT VOLTAGE RANGE SELECTION**

| Output Range | 0 to +10 V | ±5 V | ±10 V |
|---|---|---|---|
| Pin Connection | | | |
| Connect Pin 24 to | 16 | 16 | 16 |
| Connect Pin 17 to | 21 | 20 | 20 |
| Connect Pin 15 to | 18 | 18 | NC |
| Connect Pin 20 to | NC | 17 | 17 |

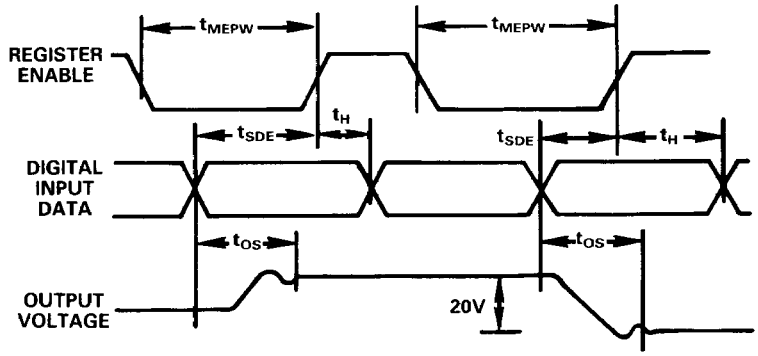
*Table 2.*

**INPUT LOGIC CODING**

| Digital Input MSB LSB | Analog Output 0 to +10 V | ±5 V | ±10 V |
|---|---|---|---|
| 0000 0000 0000 | +9.9976 V | +4.9976 V | +9.9951 V |
| 0000 0000 0001 | +9.9951 V | +4.9951 V | +9.9902 V |
| 0111 1111 1111 | +5.0000 V | 0.0000 V | 0.0000 V |
| 1000 0000 0000 | +4.9976 V | −0.0024 V | −0.0049 V |
| 1111 1111 1110 | +0.0024 V | −4.9976 V | −9.9951 V |
| 1111 1111 1111 | 0.0000 V | −5.0000 V | −10.0000 V |

**CODING NOTES:**
1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR = 20 V, 1 LSB = 4.88 mV.
4. For FSR = 10 V, 1 LSB = 2.44 mV.

*Table 3.*




**TIMING NOTES:**

$t_{MEPW}$ MINIMUM ENABLE PULSE WIDTH IS 60 ns.
$t_{SDE}$ MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40 ns.
$t_H$ HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA AND IS 10 ns.
$t_{OS}$ OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO ±1/2LSB IS 7µs MAX.

*Figure 1. Input Register Timing Diagram*