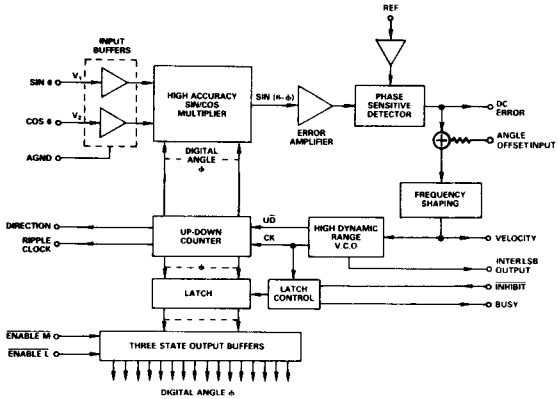
Tachogenerator Output, Hybrid Resolver-to-Digital Converters

1S14/1S24/1S44/1S64

FEATURES
40-Pin Hybrid
Tachogenerator Velocity Output
DC Error Output
Sub LSB Output
Angle Offset Input
Reference Frequency of 2kHz to 10kHz
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Feed Forward Velocity Stabilizing Loops
Robotics
Closed Loop Motor Drives
Brushless Tachometry
Single Board Controllers

1S14/1S24/1S44/1S64 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1SN4* are hybrid devices that convert standard resolver inputs to digital position and analog velocity outputs. All the essential features for multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically the input signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1SN4 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the users chosen volts/rpm relationship.

Repeatability is 1LSB under constant temperature conditions.

Four resolutions are available all operating over a frequency range of 2kHz to 10kHz.

1S14 is 10-bit up to 40,800 revolutions per minute.
1S24 is 12-bit up to 10,200 revolutions per minute.
1S44 is 14-bit up to 2,550 revolutions per minute.
1S64 is 16-bit up to 630 revolutions per minute.

*N is 1, 2, 4 or 6 depending upon resolution of model.

APPLICATIONS

The 1SN4 has been specifically designed for motor position control for the numerically controlled machine and robot industry, using the type 2 servo loop tracking principle that ideally suits these converters to the electrically noisy environment found in these industrial applications.

USER BENEFITS

Allows both velocity and position measurement from a single, low cost, standard, brushless resolver.

80dB dynamic range of velocity output.

0.5% ripple on velocity signal.

0.1% linearity of velocity signal.

Cost effective tachogenerator replacement.

Tracks at 5 to 10 times the rate of equivalent resolution encoders.

Analog output for interpolation between digital codes.

Direction and Ripple Clock (Datum) outputs facilitate revolution counting.

Hybrid construction offering small size and MTBF of >200 years at 50°C GB.

SPECIFICATIONS (typical for both commercial (5Y0) and extended (4Y0) temperature range options @ 25°C and ±15V or ±12V power supplies, unless otherwise noted)

Models / Parameters		1S14	1S24	1S44	1S64	Units
RESOLVER INPUTS						
Signal Voltage		2.0 ± 5%	*	*	*	V rms
Reference Voltage		2.0 + 50%/ − 20%	*	*	*	V rms
Signal & Reference Frequency		2k–10k	*	*	*	Hz
Signal Input Impedance		10(min)	*	*	*	MΩ
Reference Input Impedance		125	*	*	*	kΩ
Allowable Phase Shift (Signal to Reference)		± 10	*	*	*	Degrees
POSITION OUTPUT						
Resolution		10	12	14	16	Bits
1LSB		0.35	0.088	0.022	0.0055	Degrees
Accuracy (max error over temp. range)	5Y0	± 25.0 (0.42)	± 8.5 (0.14)	± 5.3 (0.09)	± 4.0 (0.07)	Arc-mins (degrees)
		± 0.12	± 0.04	± 0.025	± 0.019	% F.S.
	4Y0	± 25.0 (0.42)	± 8.5 (0.14)	± 5.3 (0.09)	± 2.6 (0.04)	Arc-mins (degrees)
		± 0.012	± 0.04	± 0.025	± 0.012	% F.S.
Digital Position Output Format		Parallel natural binary	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Monotonicity		Guaranteed	*	*	*	
Repeatability		1	*	*	*	LSB
DATA TRANSFER						
Busy Output		Logic "Hi" when Busy	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Busy Width		380 (min) 530 (max)	*	*	*	ns
$\overline{\text{ENABLE}}$ Inputs		Logic "Lo" to Enable	*	*	*	
Load		1	*	*	*	LSTTL
Enable & Disable Times		250 (max)	*	*	*	ns
$\overline{\text{INHIBIT}}$ Input		Logic "Lo" to Inhibit	*	*	*	
Load		1	*	*	*	LSTTL
Direction Output (DIR)		Logic "Hi" when counting up, Logic "Lo" when counting down.	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Ripple Clock (RC)		Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Width		1μ(max) 850n(min)	*	*	*	Secs
DYNAMIC CHARACTERISTICS						
Tracking Rate (min)						
with ± 15V supplies		40,800	10,200	2,550	630	rpm
with ± 12V supplies		34,680	8,670	2,168	536	rpm
Acceleration Constant Ka		220,000	*	*	*	Sec^{-2}
Settling time (179° step input)		25 (max)	35 (max)	60 (max)	120 (max)	ms
Bandwidth		230	*	*	*	Hz
VELOCITY OUTPUT						
Polarity		Positive for increasing angle	*	*	*	
Tachogenerator Voltage Scaling		0.25	1	4	16	V/K rpm
Scale Factor Accuracy		± 1 (max)	*	*	*	% of output
Scale Factor Tempco		200 (max)	*	*	*	ppm/°C
Reversion Error		± 0.2 (max)	*	*	*	%
Reversion Error Tempco		50 (max)	*	*	*	ppm/°C
Linearity		0.1	*	*	*	% of output
Over full temp range		0.25 (max)	*	*	*	% of output
Ripple and Noise						
Steady State @10kHz (200Hz b/w)		100	150	300	1300	μV rms
Dynamic Ripple (av-pk)		0.5 (max)	*	*	*	% of output
Zero Offset		± 500	*	*	*	μV
Zero Offset Tempco		50 (max)	*	*	*	μV/°C
Output Load		5 (min)	*	*	*	kΩ

Models Parameters	1S14	1S24	1S44	1S64	Units
SPECIAL FUNCTIONS					
DC Error Output Voltage	450	*	*	*	mV/degree
Inter LSB Output	±1 (±20%)	*	*	*	V/LSB
Load	1 (min)	*	*	*	kΩ
Angle Offset Input (over operating temperature range)	320 (±10%)	*	*	*	nA/LSB
Maximum Input	32	*	*	*	LSB
POWER REQUIREMENTS					
Power Supplies					
$\pm V_S$	±15 (±5%) or ±12 (±5%)	*	*	*	V dc
+5V	+4.75 to +5.25	*	*	*	V dc
Power Supply Consumption					
$\pm V_S$	30 (max)	*	*	*	mA
+5V	125 (max)	*	*	*	mA
Power Dissipation	1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating 5Y0 option	0 to +70	*	*	*	°C
4Y0 option	−55 to +125	*	*	*	°C
Storage 5Y0 option	−55 to +125	*	*	*	°C
4Y0 option	−60 to +150	*	*	*	°C
DIMENSIONS					
5Y0 option	2.1" × 1.1" × 0.195(5.3 × 28 × 4.95)	*	*	*	Inches (mm)
4Y0 option	2.14" × 1.14" × 0.18(54.4 × 29 × 4.6)	*	*	*	Inches (mm)
WEIGHT	1 (28)	*	*	*	oz. (grms)

NOTES
*Specifications same as 1S14.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +17V dc
$-V_S$[1] . . . . . 0V to −17V dc
+5V[2] . . . . . 0V to +6.0V dc
Reference . . . . . ±17V dc
Sine . . . . . ±17V dc
Cosine . . . . . ±17V dc
Any Logical Input . . . . . −0.4V to +5.5V dc

CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

OPERATION OF THE CONVERTER

The 1SN4 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the resolution option. No convert command is necessary as the conversion is initiated by each LSB increment for the input. Each LSB increment of the converter initiates a BUSY pulse.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

The static angular accuracy quoted for each converter type is the worst case error that can occur over the full operating temperature range with the following input conditions:

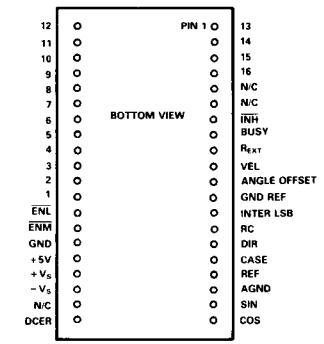
a) Signal input amplitudes within 5% of the nominal values.
b) Signal and reference frequency within the specified operating range.
c) Phase shift between signal and reference less than 10 degrees.
d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice the converters can be used well outside these operating conditions providing the following points are observed:

Signal Amplitude (Sine and Cosine Inputs)
The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the analog outputs and inputs of the converter such as velocity, inter LSB position and angle offset.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the factor Ka is proportional to signal level.

PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" WHEN NO SCALING REQUIRED
2. CASE PIN CONNECTED ON 460 OPTION ONLY.

Signal and Reference Frequency
Any frequency within the specified range of the converter may be used. It should be noted that the same frequency must be used on both inputs.

Reference Voltage Level
The amplitude of the reference signal applied to the converter's input is very uncritical, however it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

Harmonic Distortion
The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square and triangle waveforms can be used but the input levels should be adjusted so that the average value after rectification is 1.9 volts. (For example – a square wave should be 1.9V peak).

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Phase Shift (Between Signal and Reference)
See Section on "Dynamic Accuracy vs. Resolver Phase Shift".

DATA TRANSFER

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:
The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Note: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

$\overline{\text{ENABLE}}$ Inputs:
Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the most significant 8-bits and $\overline{\text{ENABLE L}}$ for the least significant remainder. These $\overline{\text{ENABLES}}$ determine the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins. The operation of these $\overline{\text{ENABLES}}$ has no effect on the conversion process.

Two methods are available for transferring data, by using the inputs and outputs described.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

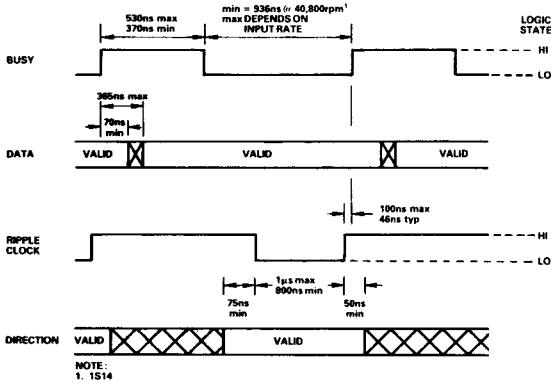


Figure 1. Timing Diagram

RIPPLE CLOCK (RC) and DIRECTION (DIR) Outputs: As the digital output of the converter passes through the major carry, i.e. all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The DIRECTION (DIR) logic output indicates the direction of input rotation and this data is always valid in advance of the

RIPPLE CLOCK pulse, and stays valid until the direction changes (see Timing Diagram – Figure 1).

These two logic outputs are provided so that the user can count the input revolutions or pitches. An external extension counter is required. Figure 7 shows the application circuit which should be used to perform this counting function.

Note: CMOS external counters can be used (see Figure 2) but it is not advisable as great care must be taken to keep stray capacitances low because of the high tracking rate of the converter.

VELOCITY OUTPUT

The tracking conversion technique produces an internal signal at the input to the voltage controlled oscillator (VCO) that is proportional to the rate of the input angle. In the 1SN4 series additional circuitry is included to linearize this signal, which is closely characterized, producing a high quality tachogenerator velocity output at the VELOCITY (VEL) pin.

This analog tachogenerator velocity output is resistively scaled internally to give a full scale output of ± 10V dc at the specified tracking rate for the converter.

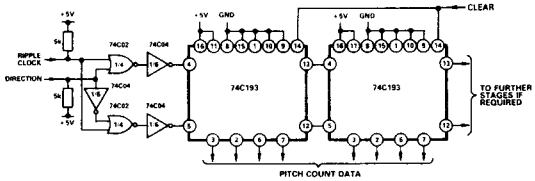


Figure 2. CMOS External Counter

However, a full scale output of ± 10V dc can be obtained for lower speeds by changing the gain of the internal scaling amplifier using only one external resistor. The external resistor, R_{EXT}, should be connected between "R_{EXT}" pin and the GND REF pin, and calculated using the following equation.

$$R_{EXT} = \frac{10 \times A}{B - A}\ k\Omega$$

Where A = required rps to be represented by ± 10V FS

and B = specified rps for the converter.

Note: A cannot be greater than B and for unity gain "VEL" and "R_{EXT}" pins should be linked (no external resistor required).

When the external resistor facility is used to provide large magnifications there is an additional velocity output offset generated due to the inevitable common ground impedance inherent with a single ground connection point. While these offsets will still be in spec, they can be code dependent. They can be minimized by taking the external scaling resistor from "R_{EXT}" to GND REF instead of "GND". This means that the velocity output will be unaffected by the varying current drawn from the +5V supply as the digital output changes.

Ripple and noise on the velocity signal consists of two components – steady state noise and dynamic noise.

Steady state noise – this is internally generated noise produced by the converter's circuitry and is the only noise signal present under static input conditions.

Dynamic noise – this is the noise produced, in addition to steady state noise, under dynamic operating conditions.

The two main components of the dynamic noise signal are due to the "non-zero" angular error of the resolver/converter combination. The figures given in the specification are typical for a size 11, 7 arc-minutes, brushless resolver.

It should be noted that when operating at low tracking rates it is critical to maintain the signal input voltage at its nominal value in order to keep the noise level on the velocity signal to an absolute minimum. The effect of variation in signal voltage at low tracking rates is to produce low energy spikes on the velocity output on the rising edge of the BUSY pulse. The amplitude of these spikes will be in the region of 30µV per percent variation in signal input voltage level.

Note: The velocity signal output and max tracking rate derates by 15% (max) for operation with ± 12 volt power supplies.

SPECIAL FUNCTIONS

DC Error: The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converters are a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason. It is therefore an indication that the input has exceeded the maximum tracking rate of the converter, or, due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

INTER LSB Output: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

The output is therefore proportional to the inter LSB resolved position with a maximum output representing 1LSB.

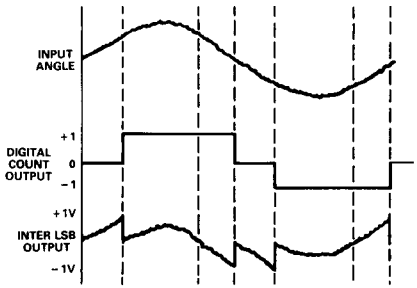


Figure 3

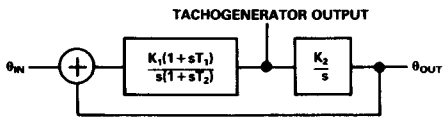
Figure 3 illustrates how the INTER LSB output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and INTER LSB output equals the actual input angle.

ANGLE OFFSET Input: A unique feature of the 1SN4 series of converter is their angle offset input which allows the user to electrically "rotate" the input shaft of the resolver.

Injecting a current of 320nA into the angle offset input pin will offset the digital output of the converter by 1LSB relative to the angle defined by the resolver inputs. It is recommended that an offset equivalent to no greater than 30LSB's be applied to this input.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Positional Transfer Function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1K_2}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2} \text{ Open Loop}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_1K_2} + \frac{s^3T_2}{K_1K_2}} \text{ Closed Loop}$$

where $K_1K_2 = K_a$

Tachogenerator Transfer Function:

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{K_1(1 + sT_1)}{s(1 + sT_2)} \text{ Open Loop}$$

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{s(1 + sT_1)}{K_2(1 + sT_1) + \frac{s^2}{K_1} + \frac{s^3T_2}{K_1}}$$

Closed Loop

Where: $K_1 = 3.23$
$K_2 = 68.2 \times 10^3$
$K_a = 220 \times 10^3$
$T_1 = 4.46\text{ms}$
$T_2 = 0.21\text{ms}$

Refer: Figures 4 and 5

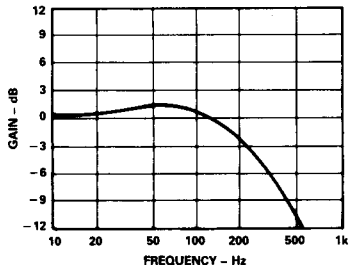


Figure 4. Gain Plot

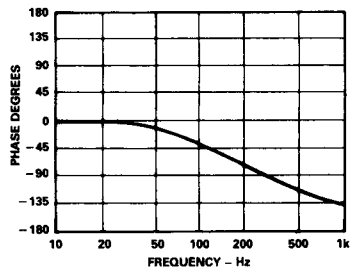


Figure 5. Phase Plot

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Under static operating conditions phase shift between signal and reference lines theoretically does not effect the converter's static accuracy.

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

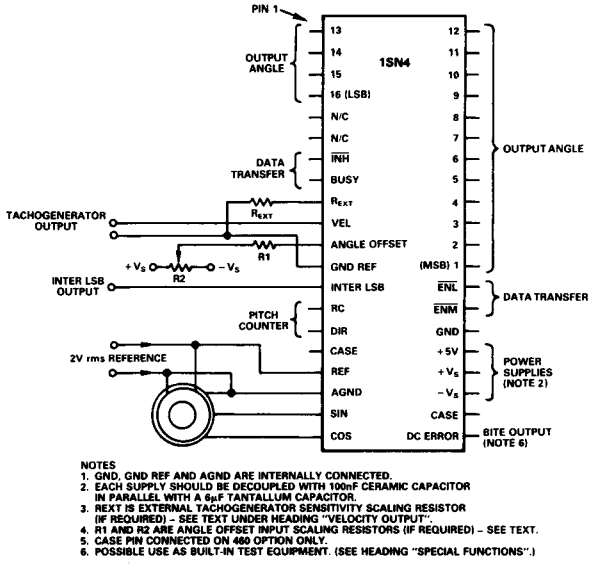
$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.



NOTES
1. GND, GND REF AND AGND ARE INTERNALLY CONNECTED.
2. EACH SUPPLY SHOULD BE DECOUPLED WITH 100nF CERAMIC CAPACITOR IN PARALLEL WITH A 6μF TANTALLUM CAPACITOR.
3. REXT IS EXTERNAL TACHOGENERATOR SENSITIVITY SCALING RESISTOR (IF REQUIRED) – SEE TEXT UNDER HEADING "VELOCITY OUTPUT".
4. R1 AND R2 ARE ANGLE OFFSET INPUT SCALING RESISTORS (IF REQUIRED) – SEE TEXT.
5. CASE PIN CONNECTED ON 460 OPTION ONLY.
6. POSSIBLE USE AS BUILT-IN TEST EQUIPMENT. (SEE HEADING "SPECIAL FUNCTIONS".)

Figure 6. Electrical Connections

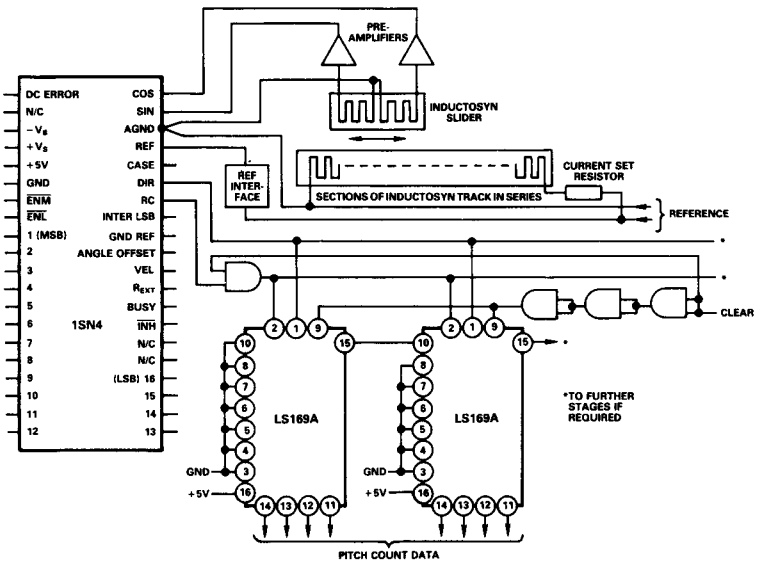


Figure 7. Connections for Use with Inductosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be ±12V to ±15V but must not be reversed. The +5V supply connects to the +5V pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors are connected in parallel between the power lines ($+V_S$, $-V_S$ and +5V) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 6).

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

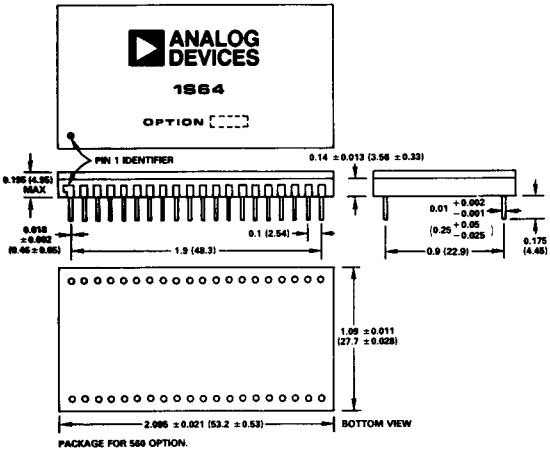
HIGH REL PROCESSING

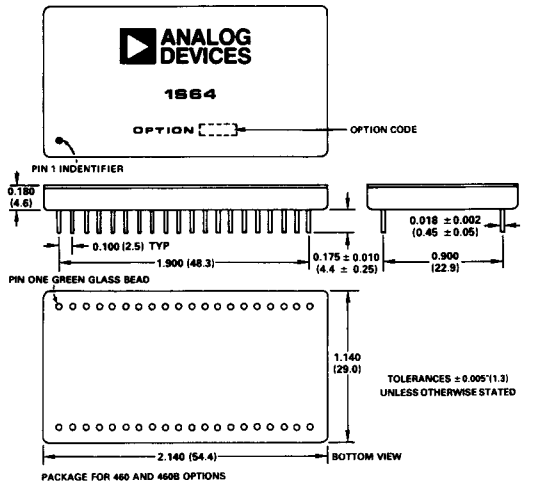
All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 5000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{MIN} and T_{MAX}
7. Seal test, fine and gross
8. External visual inspection

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).





ORDERING INFORMATION