Advance **8Mb (256Kx36 & 512Kx18) and 4Mb (128Kx36 & 256Kx18) SRAM**

Features

- 8Mb: 256K x 36 or 512K x 18 Organizations
- 4Mb: 128K x 36 or 256K x 18 Organizations
- CMOS Technology
- Double Data Rate and Single Data Rate Synchronous Modes of Operation
- Pipeline Mode of Operation
- Self-Timed Late Write with Full Data Coherency
- Single Differential HSTL Clock
- +2.5V Power Supply, Ground, 1.6V V_{DDQ}, and 0.95V V_{REF}
- HSTL Input and Output levels
- Registered Addresses, Controls, and Data Ins.
- Burst Mode of operation
- Common I/O
- Asynchronous Output Enable
- Boundary Scan using limited set of JTAG 1149.1 functions
- 9 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

Description

The IBM0436A4CXLBB, IBM0418A4CXLBB, IBM0418A8CXLBB, and IBM0436A8CXLBB SRAMs are Synchronous Pipeline Mode, high-performance CMOS Static Random Access Memories that are versatile, have wide I/O, and achieve 4ns cycle times. Differential CK clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the CK clock, all Addresses, Controls, and Data Ins are registered internally. Data Outs are updated from output registers off the next rising and falling edge of the K clock, hence the Double Data Rate. Internal Write buffers allow write data to follow one cycle after addresses and controls. The chip is operated with a single +2.5V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	DQ	DQ	SA	VSS	B1(LD)	VSS	SA	DQ	DQ
C	VSS	VDDQ	SA	SA	$\overline{G}$	SA	SA	VDDQ	VSS
D	DQ	DQ	NC	VSS	VDD	VSS	SA(8M)	DQ	DQ
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	DQ	CQ	DQ	VDD	VDD	VDD	DQ	CQ	DQ
G	VSS	VDDQ	VSS	VSS	CK	VSS	VSS	VDDQ	VSS
H	DQ	DQ	DQ	VDD	$\overline{CK}$	VDD	DQ	DQ	DQ
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	DQ	DQ	DQ	VSS	B2(WE)	VSS	DQ	DQ	DQ
L	VSS	VDDQ	VSS	$\overline{LBO}$	B3(DDR)	NC	VSS	VDDQ	VSS
M	DQ	$\overline{CQ}$	DQ	VDD	VDD	VDD	DQ	$\overline{CQ}$	DQ
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	DQ	DQ	NC	VSS	VDD	VSS	SA	DQ	DQ
R	VSS	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	VSS
T	DQ	DQ	SA	VSS	SA0	VSS	SA	DQ	DQ
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	VSS

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	NC	DQ	SA	VSS	B1(LD)	VSS	SA	NC	DQ
C	VSS	VDDQ	SA	SA	$\overline{G}$	SA	SA	VDDQ	VSS
D	DQ	NC	NC	VSS	VDD	VSS	SA(8M)	DQ	NC
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	NC	CQ	NC	VDD	VDD	VDD	DQ	NC	DQ
G	VSS	VDDQ	VSS	VSS	CK	VSS	VSS	VDDQ	VSS
H	DQ	NC	DQ	VDD	$\overline{CK}$	VDD	NC	DQ	NC
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	NC	DQ	NC	VSS	B2(WE)	VSS	DQ	NC	DQ
L	VSS	VDDQ	VSS	$\overline{LBO}$	B3(DDR)	NC	VSS	VDDQ	VSS
M	DQ	NC	DQ	VDD	VDD	VDD	NC	$\overline{CQ}$	NC
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	NC	DQ	SA	VSS	VDD	VSS	SA	NC	DQ
R	VSS	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	VSS
T	DQ	NC	SA	VSS	SA0	VSS	SA	DQ	NC
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	VSS

Pin Description

SA0-SA18	Address Inputs SA0-SA1 Burst control starting addresses SA0-SA18 for 512Kx18 SA0-SA17 for 256Kx36 SA0-SA17 for 256Kx18 SA0-SA16 for 128Kx36	TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTL levels)
DQ0-DQ35	Data I/O DQ0-DQ17 for 512Kx18 DQ0-DQ35 for 256Kx36	TDO	IEEE 1149.1 Test Output (LVTTL level)
CQ, $\overline{CQ}$	Output Differential Echo Clocks	V_{REF}(2)	HSTL Input Reference Voltage
CK, $\overline{CK}$	Differential Input Register Clocks	V_{DD}	Power Supply (+2.5V)
B1	Synchronous Function Control Input. B1 = 0 Loads a new Address	V_{SS}	Ground
B2	Synchronous Function Control Input (WE). B2 = 0 starts Write & B2 = 1 starts Read.	V_{DDQ}	Output Power Supply
B3	Synchronous Function Control Input. B3 = 0 starts a DDR (Burst) operation. B3 = 1 starts a SDR (Single Data Rate)	ZQ	Input pin for Output Driver Impedance Control.
$\overline{LBO}$	Linear Burst Order, ($\overline{LBO}$ =1 interleave mode, $\overline{LBO}$ = 0 linear mode)	NC	No Connect
$\overline{G}$	Asynchronous Output Enable		

Ordering Information

Part Number	Organization	Speed	Leads
IBM0418A4CXLBB-3	512K x 18	2.0ns Access / 3.5ns Cycle	9 x 17 BGA
IBM0418A4CXLBB-4		2.0ns Access / 4.0ns Cycle	
IBM0418A4CXLBB-5		2.5ns Access / 5.0ns Cycle	
IBM0436A4CXLBB-3	256K x 36	2.0ns Access / 3.5ns Cycle	
IBM0436A4CXLBB-4		2.0ns Access / 4.0ns Cycle	
IBM0436A4CXLBB-5		2.5ns Access / 5.0ns Cycle	
IBM0418A8CXLBB-3	512K x 18	2.0ns Access / 3.5ns Cycle	
IBM0418A8CXLBB-4		2.0ns Access / 4.0ns Cycle	
IBM0418A8CXLBB-5		2.5ns Access / 5.0ns Cycle	
IBM0436A8CXLBB-3	256K x 36	2.0ns Access / 3.5ns Cycle	
IBM0436A8CXLBB-4		2.0ns Access / 4.0ns Cycle	
IBM0436A8CXLBB-5		2.5ns Access / 5.0ns Cycle	

Revision Log

Date	Contents of Modification
8/99	Initial release.

For a complete datasheet, please contact your IBM sales representative.

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.