Features

- 256K x 16 Multiport Video RAM
- Performance:

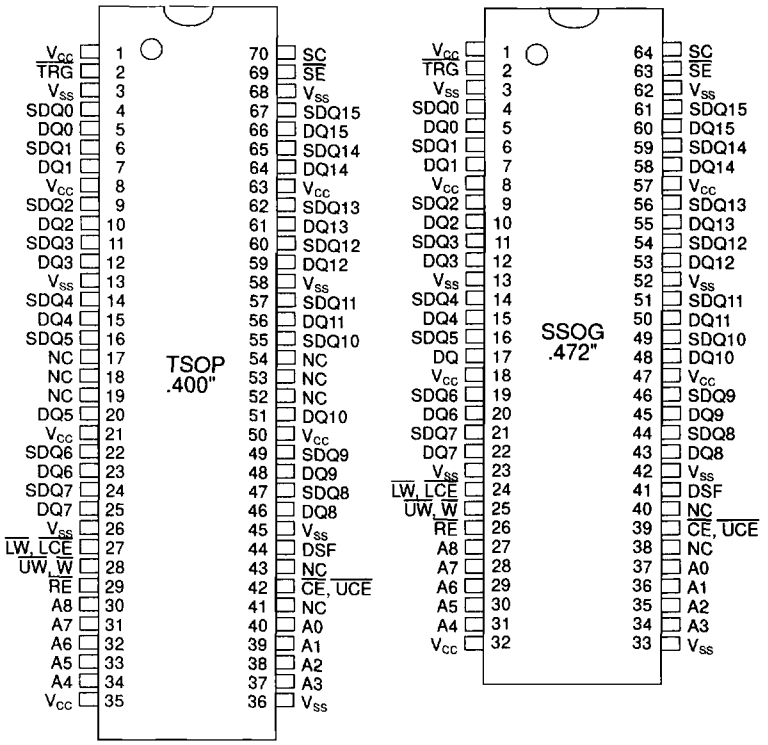
Parameter	-60	-70
t_{RP} - $\overline{RE}$ Precharge	25ns	30ns
t_{SCA} - Serial Access Time	15ns	17ns
t_{CAC} - Access Time from $\overline{CE}$	15ns	17ns
t_{AA} - Column Address Access Time	30ns	35ns
t_{SCC} - Serial Clock Cycle Time	18ns	20ns
t_{RC} - Read or Write Cycle Time	95ns	110ns
t_{PC} - Fast Page Mode Cycle Time	35ns	40ns
t_{HPC} - Extended Data Out Cycle Time	25ns	30ns

- Compatible to Full Depth SAM in SRS mode
- 8 x 16 bits Block Write with masking and individual byte control
- Fast Page Mode with Extended Data Out
- Flash Write with WPBM- 512 x 16 bits
- Persistent & Non-Persistent WPBM mode
- Split Serial Register with Width Control
- 256 Location Start (Start Address) Pointer
- Masked Write Transfer
- Masked Split Write Transfer
- Power Supply: 5.0V±10% and 3.3V±10%
- High Performance, CMOS .6µm process
- TSOP-70 and SSOG-64 JEDEC Std.
- TTL compatible

Description

The 4Mb dual port Video RAM (VRAM) consists of a Dynamic Random Access Memory (DRAM) organized as 256K x 16 interfaced to a Serial Register / Serial Access Memory (SAM) consisting of 256 x 16. The VRAM supports three basic operations: bidirectional random access to the DRAM, bidirectional serial access to the SAM, and bidirectional data transfer between any DRAM row and the SAM. Full compatibility is provided between half depth (256 x 16) SAM and full depth (512 x 16) by setting the VRAM in Serial Register Stop (SRS) mode with a stop address of 128 bit (or less) and performing a split transfer operation every 128 bits (or less) with a tile depth of 2 or more. Unique features have been added to these basic VRAM operations to enhance update capability and to provide maximum system design flexibility. Greater update rates can be achieved with either flash write or block write modes. Two $\overline{W}$ or two $\overline{CE}$ inputs are provided for individual byte control for both normal write and block write. For individual bit control, a Write-Per-Bit Mask (WPBM) can be supplied on the data pins at $\overline{RE}$ time for use during masked write transfers or masked write cycles. A permanent mask can be loaded during the Load Mask Register (LMR) cycle.

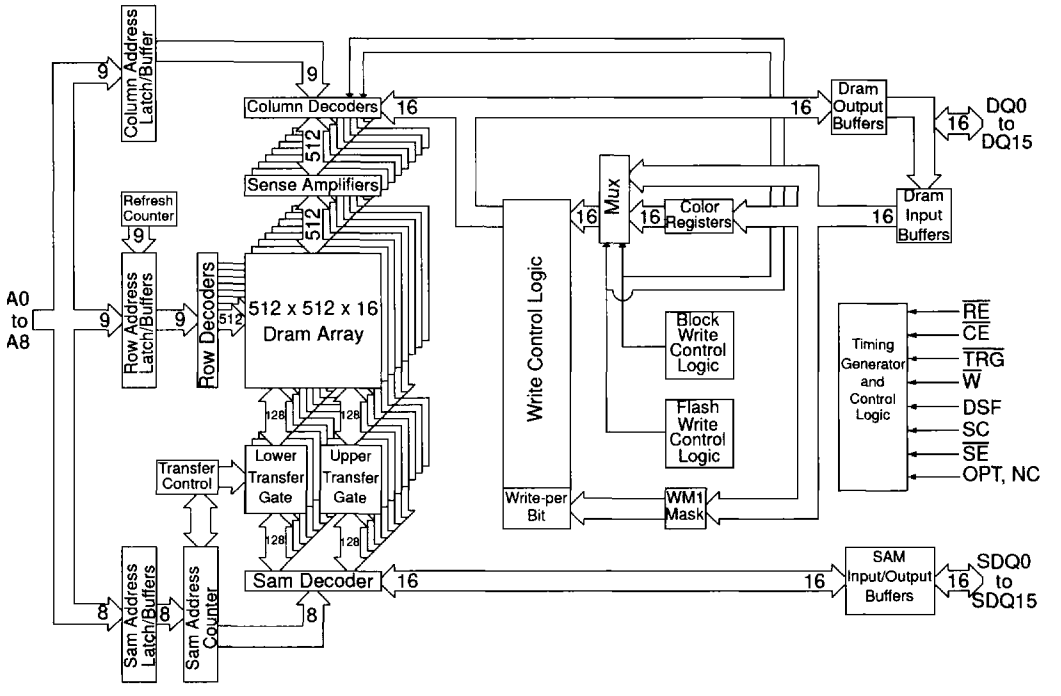
Pin Assignments



Pin Description

$\overline{RE}$	Row Enable. Latches the row addresses and the state of $\overline{CE}$, $\overline{TRG}$, $\overline{W}$, and DSF to invoke the various DRAM port and serial port functions.
$\overline{CE}$	Column Enable Latches the column addresses and state of DSF to invoke various DRAM port and serial port functions. $\overline{CE}$ also acts as an output enable for the DRAM port output pins.
$\overline{UCE}$, $\overline{LCE}$	Upper & Lower Column Enable (Only In Dual $\overline{CE}$ Parts) Latches the column address and state of DSF to invoke various DRAM port and serial port functions. $\overline{LCE}$ and $\overline{UCE}$ control $byte_L$ and $byte_U$ for the DRAM port read and write operations.
$\overline{W}$	Write (Only In Dual $\overline{CE}$ PARTS) Enables the DRAM port write circuitry. It is also used as a control input pin to define the various operations at $\overline{RE}$ time.
$\overline{UW}$, $\overline{LW}$	Upper & Lower Write (Only In Dual $\overline{W}$ Parts) Enable the DRAM port write circuitry for $byte_L$ and $byte_U$, respectively. It is also used as a control input pin to define the various operations at $\overline{RE}$ time. Either $\overline{W}$ being low is considered low for purposes of determining whether a cycle is a read or write.
$\overline{TRG}$	Data Transfer & Output Enable. A multifunctional input which in conjunction with other control pins either enables the DRAM data outputs or enables transfer operations to take place between the serial and primary port. $\overline{TRG}$ is also used as a control input pin to define the various operating modes at $\overline{RE}$ time.
DSF	Designated Special Function A control pin which is used in conjunction with other control pins to define the various operating modes at $\overline{RE}$ and $\overline{CE}$ time.
A8-A0	Address Inputs Defines the cell(s) location within the DRAM and for defining the start pointer for the SAM. The address pins are multiplexed as row and column address inputs.
DQ_{15} - DQ_0	Random Port Input/Output The DRAM port outputs in read mode and the DRAM port inputs in write mode. These ports also serve as input for the mask load cycles, the color register load cycles, the DQ mask and column mask for block write.
SDQ_{15} - SDQ_0	Serial Port Input/Output The serial port outputs in read mode and the serial port inputs in write mode. The output remains valid until next SC.
SC	Serial Clock The input is used to synchronize the SAM read and write operation. The rising edge of the SC signal is used to initiate a read or write.
$\overline{SE}$	Serial Enable. Enable or disable the serial access circuitry.
V_{CC}	Voltage (5.0V±10% & 3.3V±10%). All voltages are referenced to the nearest V_{SS} pin.
V_{SS}	Ground. V_{SS}=0V
NC	No Connect

Block Diagram



Ordering Information.

Part Number		Organization 256K X 16	Speed	Voltage
.472" SSOG	.400" TSOP			
IBM025160LG5B-60		Dual $\overline{CE}$, Fast Page, 5.0V	60 ns	5.0V
IBM025160LG5B-70			70ns	
IBM025170LG5B-60		Dual $\overline{W}$, Fast Page, 5.0V	60 ns	
IBM025170LG5B-70			70ns	
IBM025161LG5B-60		Dual $\overline{CE}$, Extended Data, 5.0V	60 ns	
IBM025161LG5B-70			70ns	
IBM025171LG5B-60		Dual $\overline{W}$, Extended Data, 5.0V	60 ns	
IBM025171LG5B-70			70ns	
IBM025160NG5B-60	IBM025160NT3B-60	Dual $\overline{CE}$, Fast Page, 3.3V	60 ns	3.3V
IBM025160NG5B-70	IBM025160NT3B-70		70ns	
IBM025170NG5B-60	IBM025170NT3B-60	Dual $\overline{W}$, Fast Page, 3.3V	60 ns	
IBM025170NG5B-70	IBM025170NT3B-70		70ns	
IBM025161NG5B-60	IBM025161NT3B-60	Dual $\overline{CE}$, Extended Data, 3.3V	60 ns	
IBM025161NG5B-70	IBM025161NT3B-70		70ns	
IBM025171NG5B-60	IBM025171NT3B-60	Dual $\overline{W}$, Extended Data, 3.3V	60 ns	
IBM025171NG5B-70	IBM025171NT3B-70		70ns	

Truth Table

Menu Code	$\overline{RE}$				$\overline{CE}$	Address		DQ_i			FUNCTION
	$\overline{CE}$	$\overline{TRG}$	$\overline{W}$	DSF	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{RE}$	$\overline{CE}$	$\overline{CE}$, $\overline{W}$	
CBR	0(5)	X	1(4)	0	-	X	-	X	-	-	$\overline{CE}$ before $\overline{RE}$ Refresh
CBRS	0(5)	X	0(3)	1	-	Stop	-	X	-	-	$\overline{CE}$ Before $\overline{RE}$ Refresh and mode set (2)
CBRN	0(5)	X	1(4)	1	-	X	-	X	-	-	$\overline{CE}$ Before $\overline{RE}$ Refresh without mode reset
ROR	1	1	1	X	-	Row(1)	-	X	-	-	$\overline{RE}$ Only Refresh
LCR	1	1	1(4)	1	1	Row(1)	X	X	X	Color	Load Color Register
LMR	1	1	1(4)	1	0	Row(1)	X	X	X	Mask	Load Mask Register
RT	1	0	1(4)	0	X	Row	TAP	X	X	X	Read Transfer
MWT	1	0	0(3)	0	X	Row	TAP	WPBM	X	0	Write Transfer (Masked)
SRT	1	0	1(4)	1	X	Row	TAP	X	X	X	Split Read Transfer
MSWT	1	0	0(3)	1	X	Row	TAP	WPBM	X	X	Split Write Transfer (Masked)
RW	1	1	1(4)	0	0	Row	COL	X	X	Data Input	Read Write Cycle (No Mask)
RWM	1	1	0(3)	0	0	Row	COL	WPBM	X	Data Input	Read Write Cycle (Masked)
BW	1	1	1(4)	0	1	Row	COL A3-A8	X	-	ADDR mask	Block Write Cycle (No Mask)
BWM	1	1	0(3)	0	1	Row	COL A3-A8	WPBM	X	ADDR mask	Block Write Cycle (Masked)
FWM	1	1	0(3)	1	X	Row	X	WPBM	X	X	Flash Write Cycle (Masked)

Notes:

1. Row address needed only for refresh operation to the selected row. Otherwise this is a don't care.
2. This cycle is used to put the chip into special modes. The A_i at $\overline{RE}$ fall select the desired mode.
3. Either $\overline{W}$ is 0.
4. Both $\overline{W}$ are 1.
5. Either $\overline{CE}$ is 0 on Dual CE parts.

Absolute Maximum Ratings (Notes: 1)

Symbol	Item	Rating		
		5.0V	3.3V	
V_{CC}	Power Supply Voltage	-1.0 to +6.0	-0.5 to +4.1	V
T_A	Operating Temperature	0 to +70	0 to +70	°C
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C
P_D	Power Dissipation	1.3	1.3	W
I_{OUT}	Short Circuit Output Current	50	20	mA

1.Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to +70°C) (Notes: 1)

Symbol	Parameter	5.0 Volt			3.3 Volt			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5	5.0	5.5	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.4		V_{CC}+0.5	2.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.5		0.8	-0.3		0.8	V

1.All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f= 1.0 MHz) (Note: 1)

Symbol	Parameter	Min.	Max.	Units
C_{I1}	Input Capacitance (Addresses)	—	5	pF
C_{I2}	$\overline{RE}$, $\overline{CE}$, $\overline{W}$, $\overline{TRG}$, DSF, SC, $\overline{SE}$	—	7	pF
C_O	Output Capacitance (DQ_i, SDQ_i)	—	7	pF

1.Data-in set-up and hold is measured from the later of the two timings - $\overline{CE}$ / $\overline{UCE}$ / $\overline{LCE}$ or $\overline{W}$ / $\overline{UW}$ / $\overline{LW}$.

Output Drivers

Driver	Impedance	Output Voltage, Low	Output Voltage, High
Serial Port	60±15 Ω	I_{OUT}=2.0 mA, V=0.4	I_{OUT}=-1 mA, V=2.4
Parallel Port	45±15 Ω	I_{OUT}=2.0 mA, V=0.4	I_{OUT}=-1 mA, V=2.4

AC Measurement Condition

Port	Detect	Load
Parallel Port Output Detect Level	2.0V / 0.8V	—
Serial Port Output Detect Level	2.0V / 0.8V	—
Parallel Port Output Load	—	1 TTL + 50 PF
Serial Port Output Load	—	1 TTL + 30 PF

Device Electrical Characteristics (T_A= 0 to +70°C, V_{CC}=5.0V/3.3V±10%)

Symbol	Parameter		5.0V		3.3V		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current (Random) Average Power Supply Operating Current ($\overline{RE}$ and $\overline{CE}$ Cycling, t_{RC}=120ns -60, t_{RC}=130ns -70, SC=0)	-60	—	135	—	135	mA	1,2,3,6
		-70	—	130	—	130		
I_{CC2}	Operating Current (Serial) Average Power Supply Current (t_{SCC}=20ns -60, t_{SCC}=23ns -70)	-60	—	40	—	40	mA	1,2,7
		-70	—	35	—	35		
I_{CC3}	Operating Current (Both Port) Average Power Supply Current ($\overline{RE}$ and $\overline{CE}$ Cycling, t_{RC}=120ns & t_{SCC}=20ns -60, t_{RC}=130ns & t_{SCC}=23ns -70)	-60	—	160	—	100	mA	1,2,3,6,7
		-70	—	150	—	150		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RE}$ δV_{IL} Min., $\overline{CE}$ Cycling, t_{PC}=40ns -60, t_{PC}=45ns -70)	-60	—	80	—	80	mA	1,2,4,6,7
		-70	—	70	—	70		
I_{CC5}	Fast Page Mode Current (Serial) Average Power Supply Current, Fast Page/Serial ($\overline{RE} \leq V_{IL}$ Min., $\overline{CE}$ Cycling, t_{PC}=40ns & t_{SCC}=20ns -60, t_{PC}=45ns & t_{SCC}=23ns -70)	-60	—	85	—	85	mA	1,2,7
		-70	—	75	—	75		
I_{CC6}	Standby Supply Current Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ =V_{CC}, SC=0V)	-60	—	400	—	400	µA	
		-70	—	400	—	400		
I_{CC7}	Data Transfer Current Average Power Supply Current (t_{RC}=120ns -60, t_{RC}=130ns -70, SC=0V)	-60	—	130	—	130	mA	
		-70	—	120	—	120		
I_{CC8}	Data Transfer Current Average Power Supply Current (t_{SCC}=20ns -60, t_{SCC}=23ns -70)	-60	—	140	—	140	mA	
		-70	—	130	—	130		
$I_{I(L)}$	Input Leakage Current, any input (0.0≤V_{IN}≤(V_{CC}+1.0V)), All Other Pins Not Under Test=0V		-10	+10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0≤V_{OUT}≤V_{CC}Max.)		-10	+10	-10	10	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT}=-1mA, Random and Serial)		2.4	—	2.4	—	V	4
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT}=+2.0mA, Random and Serial)		—	0.4	—	0.4	V	4

1.I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}, I_{CC5}, I_{CC7} and I_{CC8} depend on cycle rate.
2.I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}, I_{CC5}, I_{CC7} and I_{CC8} depend on output loading. Specified values are obtained with the output open.
3.Measured with one address change per $\overline{RE}$ cycle.
4.Measured with one column address change per page cycle.
5.V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6.Measured with $\overline{TRG}$ =V_{IH} when $\overline{CE}$ =V_{IL}.
7.Measured with $\overline{SE}$ =V_{IH}.

AC Characteristics (T_A=0 to +70°C)

Read, Write, Read-Modify-Write and Ref. Cycles (Part 1 of 2) (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{ASC}	Column address setup time	0	—	0	—	ns	
t_{ASR}	Row address setup time	0	—	0	—	ns	
t_{AR}	Column address hold time after $\overline{RE}$ low	20	—	25	—	ns	
t_{CAH}	Column address hold time after $\overline{CE}$ low	6	—	8	—	ns	5
t_{CAS}	$\overline{CE}$ pulse width	15	16K	17	16K	ns	
t_{CHCL}	First $\overline{CE}$ to return high to last $\overline{CE}$ going low	6	—	8	—	ns	
t_{CLCH}	Last $\overline{CE}$ going low to first $\overline{CE}$ to return high	6	—	8	—	ns	
t_{CP}	$\overline{CE}$ precharge time	6	—	8	—	ns	
t_{CRP}	$\overline{CE}$ high before $\overline{RE}$ low precharge	5	—	10	—	ns	8
t_{CSH}	$\overline{CE}$ hold time	60	—	70	—	ns	
$t_{H(SFC)}$	DSF hold time after $\overline{CE}$ low	6	—	8	—	ns	
$t_{H(SFR)}$	DSF hold time after $\overline{RE}$ low	6	—	8	—	ns	
t_{MH}	Write mask hold time after $\overline{RE}$ low	6	—	8	—	ns	
t_{MS}	Data-in setup before $\overline{RE}$ low	0	—	0	—	ns	
t_{RAD}	$\overline{RE}$ to column address delay time	11	35	13	40	ns	4
t_{RAH}	Row address hold time after $\overline{RE}$ low	6	—	8	—	ns	
t_{RAS}	$\overline{RE}$ pulse width	60	16K	70	16K	ns	
t_{RC},t_{WC}	Random read or write cycle time	95	—	110	—	ns	1,2
t_{RCD}	Delay from $\overline{RE}$ low to $\overline{CE}$ low.	16	45	18	53	ns	3,5
t_{RP}	$\overline{RE}$ precharge time	25	—	30	—	ns	1,6,7
t_{RSH}	$\overline{RE}$ hold time	15	—	17	—	ns	
t_{RWH}	$\overline{W}$ hold time after $\overline{RE}$ low	6	—	8	—	ns	
$t_{SU(SFC)}$	DSF setup time before $\overline{CE}$ low	0	—	0	—	ns	

1.An initial pause of 100µs is required after power-up followed by 8 $\overline{RE}$ only refresh cycles or 8 $\overline{CE}$ before $\overline{RE}$ refresh for proper device operation

2.AC measurements assume t_T=5ns.

3.Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

4.Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

5.t_{RCD} and t_{CAH} cannot be at minimum values simultaneously. t_{RCD} + t_{CAH} >= 45ns (60ns t_{RAC} product), t_{RCD} + t_{CAH}>= 50ns (70ns t_{RAC} product).

6.t_{RWL} and t_{RP} cannot be at minimum values simultaneously. t_{RWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{RWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

7.t_{CWL} and t_{RP} cannot be at minimum values simultaneously. t_{CWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{CWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

8.t_{CRP} must be 15ns (60ns t_{RAC}) or 17ns (70ns t_{RAC}) if a write-per-bit mask is used on the following $\overline{RE}$ cycle due to the fact that t_{OFF} must be met.

Read, Write, Read-Modify-Write and Ref. Cycles (Part 2 of 2) (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{SU(SFR)}$	DSF setup time before $\overline{RE}$ low	0	—	0	—	ns	
t_T	Transition time (rise and fall)	3	50	3	50	ns	
t_{TLH}	$\overline{TRG}$ hold time after $\overline{RE}$ low	6	—	8	—	ns	
t_{TLS}	$\overline{TRG}$ setup time before $\overline{RE}$ low	0	—	0	—	ns	
t_{WSR}	Write setup time before $\overline{RE}$ low	0	—	0	—	ns	
t_{WCR}	Write hold time after $\overline{RE}$ low	20	—	25	—	ns	

1.An initial pause of 100µs is required after power-up followed by 8 $\overline{RE}$ only refresh cycles or 8 $\overline{CE}$ before $\overline{RE}$ refresh for proper device operation

2.AC measurements assume t_T=5ns.

3.Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

4.Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

5.t_{RCD} and t_{CAH} cannot be at minimum values simultaneously. t_{RCD} + t_{CAH} >= 45ns (60ns t_{RAC} product), t_{RCD} + t_{CAH}>= 50ns (70ns t_{RAC} product).

6.t_{RWL} and t_{RP} cannot be at minimum values simultaneously. t_{RWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{RWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

7.t_{CWL} and t_{RP} cannot be at minimum values simultaneously. t_{CWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{CWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

8.t_{CRP} must be 15ns (60ns t_{RAC}) or 17ns (70ns t_{RAC}) if a write-per-bit mask is used on the following $\overline{RE}$ cycle due to the fact that t_{OFF} must be met.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CWL}	Write Command setup before $\overline{CE}$ high	15	—	17	—	ns	4
t_{DH}	Data-in hold time after $\overline{CE}$ low	6	—	8	—	ns	1
t_{DHR}	Data-in hold time after $\overline{RE}$ low	20	—	25	—	ns	
t_{DSC}	Data-in setup before $\overline{CE}$ low	0	—	0	—	ns	
t_{DSW}	Data-in setup before $\overline{W}$ low	0	—	0	—	ns	
t_{GHD}	$\overline{TRG}$ high before data-in applied on primary port data pins	15	—	17	—	ns	
t_{RWL}	Write setup time before $\overline{RE}$ high	15	—	17	—	ns	3
t_{WCH}	Write hold time after $\overline{CE}$ low	6	—	8	—	ns	
t_{WCS}	Early write command setup before $\overline{CE}$ Low	0	—	0	—	ns	1,2
t_{WP}	Write command pulse width	6	—	8	—	ns	

1.Data-in set-up and hold is measured from the later of the two timings - $\overline{CE}$ / $\overline{UCE}$ / $\overline{LCE}$ or $\overline{W}$ / $\overline{UW}$ / $\overline{LW}$.

2.t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If t_{WCS}>=t_{WCS}(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), and Tcpw>=Tcpw (min) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

3.t_{RWL} and t_{RP} cannot be at minimum values simultaneously. t_{RWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{RWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

4.t_{CWL} and t_{RP} cannot be at minimum values simultaneously. t_{CWL} + t_{RP} >= 60ns (60ns t_{RAC} product), t_{CWL} + t_{RP} >= 70ns (70ns t_{RAC} product).

Read-Modify-Write-Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{AWD}	Column address to $\overline{W}$ low	50	—	60	—	ns	1
t_{CWD}	$\overline{CE}$ low to $\overline{W}$ low	35	—	40	—	ns	1
t_{OEH}	Output disable ($\overline{TRG}$ high) hold time from $\overline{W}$ low	15	—	17	—	ns	
t_{RWC}	Read-modify-write cycle time	135	—	155	—	ns	
t_{RWD}	$\overline{RE}$ low to $\overline{W}$ low	80	—	95	—	ns	1

1.t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If t_{WCS}>=t_{WCS}(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), and Tcpw>=Tcpw (min) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{AA}	Access time from column address	—	30	—	35	ns	2,3
t_{CAC}	Access time from $\overline{CE}$	—	15	—	17	ns	1,2,3
t_{OEA}	Access time from $\overline{TRG}$	—	15	—	17	ns	
t_{OES}	Output enable setup ($\overline{TRG}$ low) to $\overline{RE}$ high	10	—	10	—	ns	
t_{OEZ}	Primary output disable from $\overline{TRG}$ high	0	15	0	17	ns	
t_{OFF}	Primary output disable from $\overline{CE}$	0	15	0	17	ns	5
t_{RAC}	Access time from $\overline{RE}$	—	60	—	70	ns	1,2,3
t_{RAL}	Column address to $\overline{RE}$ high	30	—	35	—	ns	
t_{RCH}	Read hold time after $\overline{CE}$ goes high	0	—	0	—	ns	4
t_{RCS}	Read command setup time	0	—	0	—	ns	
t_{RRH}	Read command hold time to $\overline{RAS}$	0	—	0	—	ns	4

1.Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

2.Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

3.Measured with the specified current and 50 pF load for the primary port. Output referenced levels: V_{OH}=2.0V and V_{OL}=0.8V.

4.Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

5.t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Read-Modify-Write-Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RWCP}	Fast page mode read-modify-write Cycle Time	74	—	84	—	ns	

Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{ACP}	Access time from $\overline{CE}$ precharge	—	35	—	40	ns	
t_{HPC}	Extended data out cycle time	25	—	30	—	ns	
t_{PC}	Fast page mode cycle time	35	—	40	—	ns	

Refresh Cycle

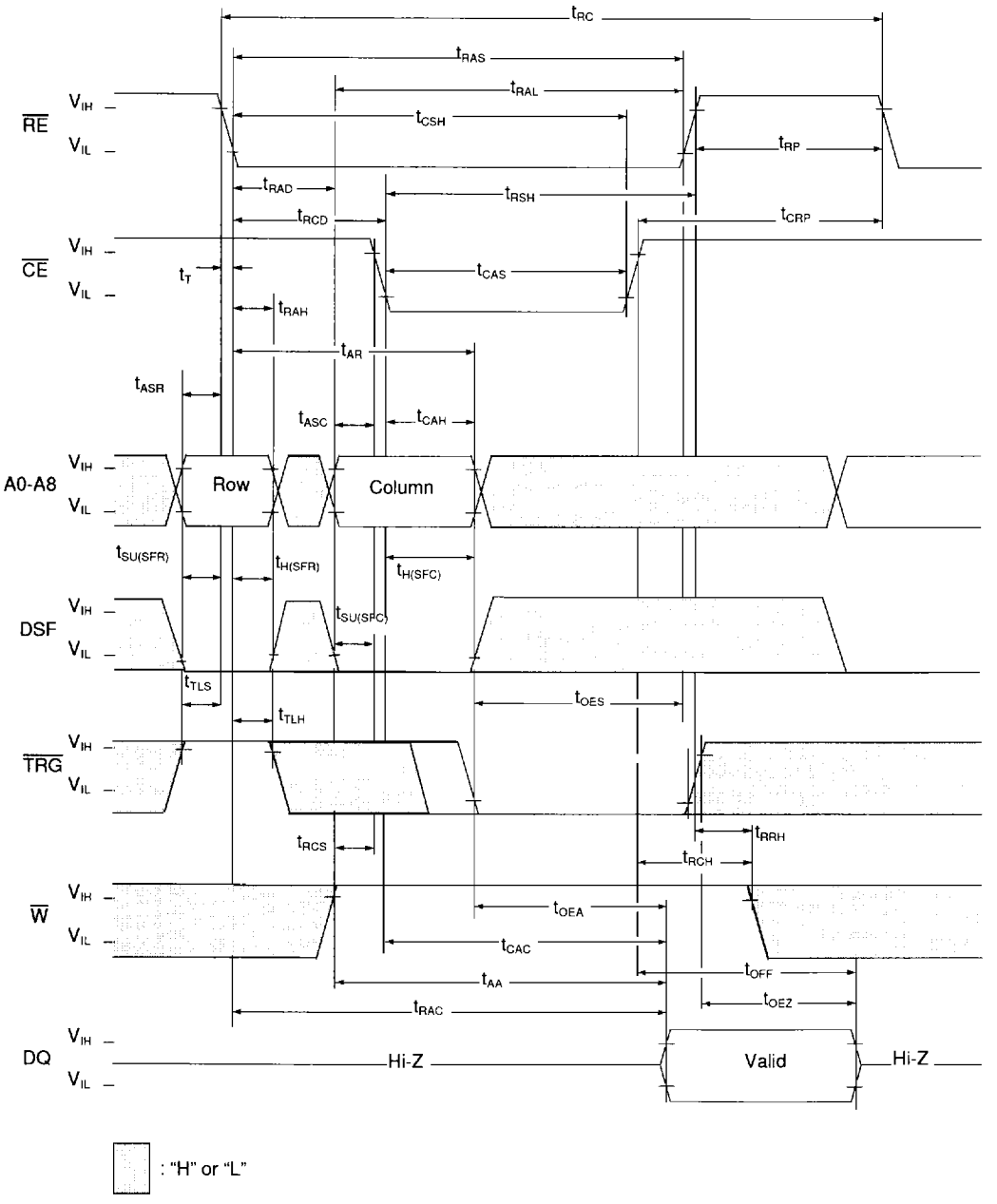
Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CHR}	$\overline{CE}$ held low after $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	6	—	8	—	ns	
t_{CSR}	$\overline{CE}$ low setup before $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	5	—	5	—	ns	
t_{REF}	Refresh period	—	32	—	32	ms	
t_{RPC}	$\overline{RE}$ high to $\overline{CE}$ low precharge	0	—	0	—	ns	

Serial Read, Write and Transfer Cycle

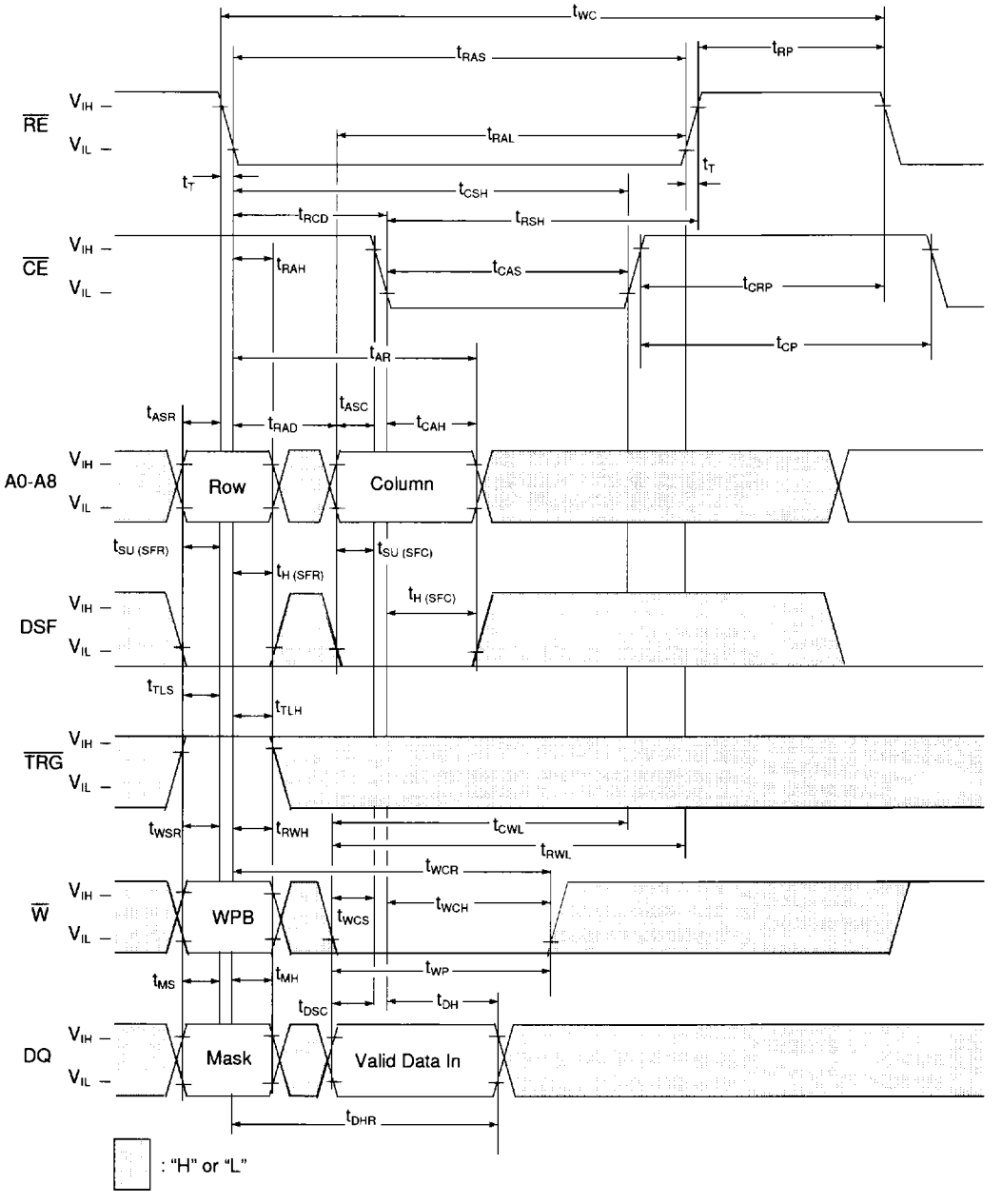
Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CSD}	$\overline{CE}$ low to first SC high after $\overline{TRG}$ goes high	15	—	17	—	ns	
t_{CTH}	Delay time from $\overline{CE}$ ow to $\overline{TRG}$ high	15	—	15	—	ns	
$t_{d(RHMS)}$	Delay time, $\overline{RE}$ high to last (most significant rising edge of SC before boundary switch during split read transfer Cycles	20	—	20	—	ns	
t_{DTH}	$\overline{TRG}$ hold after $\overline{RE}$ high	5	—	5	—	ns	
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RE}$ low during split read transfer cycles	15	—	17	—	ns	
t_{ESR}	$\overline{SE}$ setup before $\overline{RE}$ low	0	—	0	—	ns	
t_{RSD}	$\overline{RE}$ low to first SC high after $\overline{TRG}$ goes high	60	—	70	—	ns	
t_{RTH}	$\overline{RE}$ low to $\overline{TRG}$ high	45	—	55	—	ns	
t_{SC}	Width of SC high	6	—	7	—	ns	
t_{SCA}	Access time from SC going high	3	15	3	17	ns	1
t_{SCC}	Serial clock cycle time	18	—	20	—	ns	
t_{SCP}	Width of SC low	6	—	7	—	ns	
t_{SDH}	Serial data-in hold time after SC high	5	—	5	—	ns	
t_{SDS}	Serial data-in setup time to SC high	2	—	2	—	ns	
t_{SEA}	Access time from $\overline{SE}$ going low	2	8	2	10	ns	
t_{SFD}	Serial enable setup time to SC high	3	—	3	—	ns	
t_{SEZ}	Serial output disable from $\overline{SE}$ high	0	8	0	10	ns	
t_{SOH}	Old serial data out hold time after SC High	3	—	3	—	ns	
t_{SRS}	SC going high to $\overline{RE}$ low	8	—	10	—	ns	
t_{SWS}	$\overline{TRG}$ high to SC high (first serial clock after real time transfer)	8	—	10	—	ns	
t_{TCH}	$\overline{TRG}$ hold time to $\overline{CE}$ high	5	—	5	—	ns	
t_{TRH}	$\overline{TRG}$ hold to $\overline{RE}$ high	8	—	10	—	ns	
t_{TRP}	$\overline{RE}$ high to SC high (serial write transfer)	15	—	20	—	ns	
t_{TSL}	SC high delay to $\overline{TRG}$ high during a real time read transfer	5	—	5	—	ns	

1.Measured with the specified current and 30 pF load for the serial port. Output referenced levels: V_{OH}=2.0V and V_{OL}=0.8V.

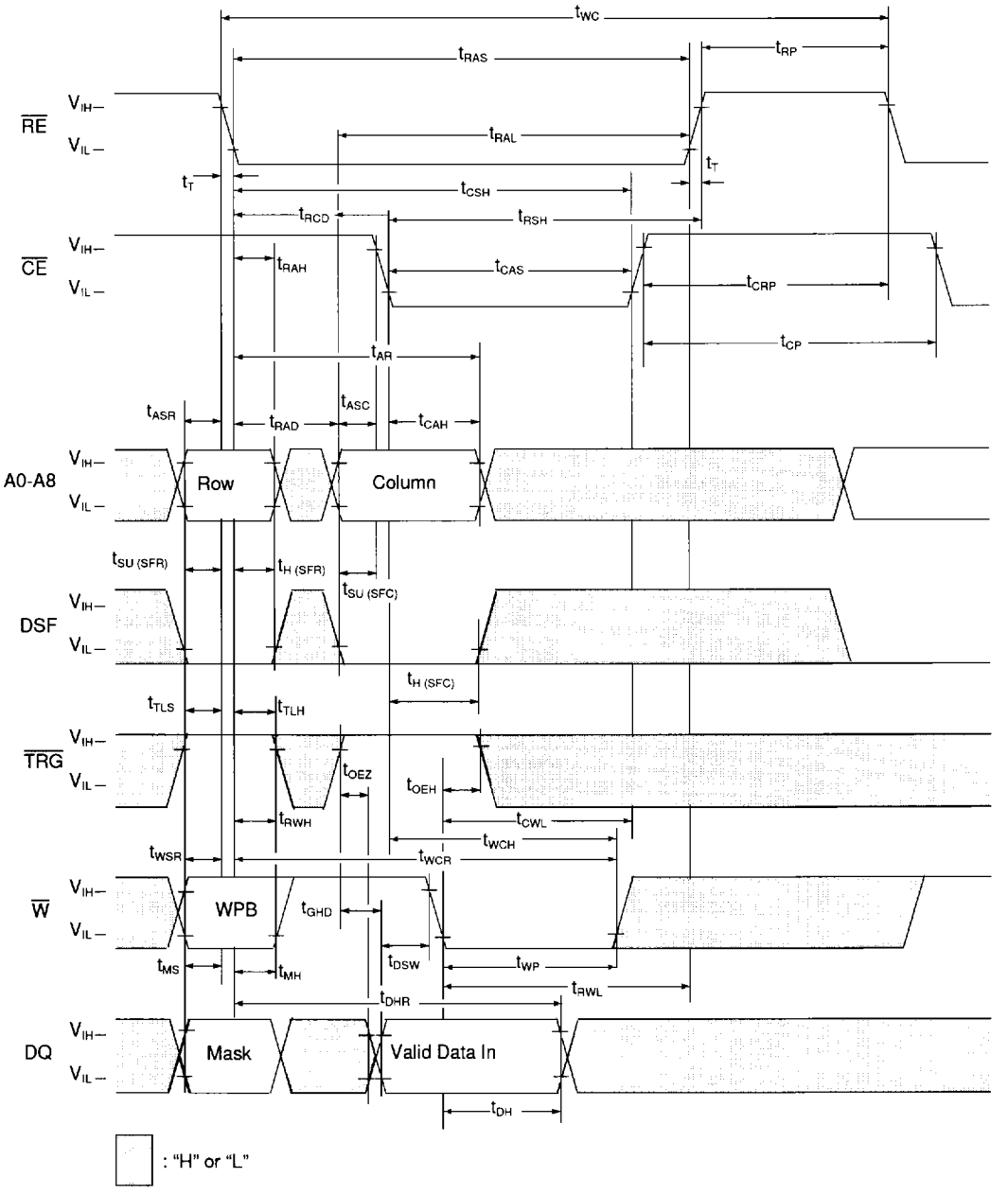
Read Cycle Timings (**Note**: Either t_{RRH} or t_{RCH} must be met on read cycles.)



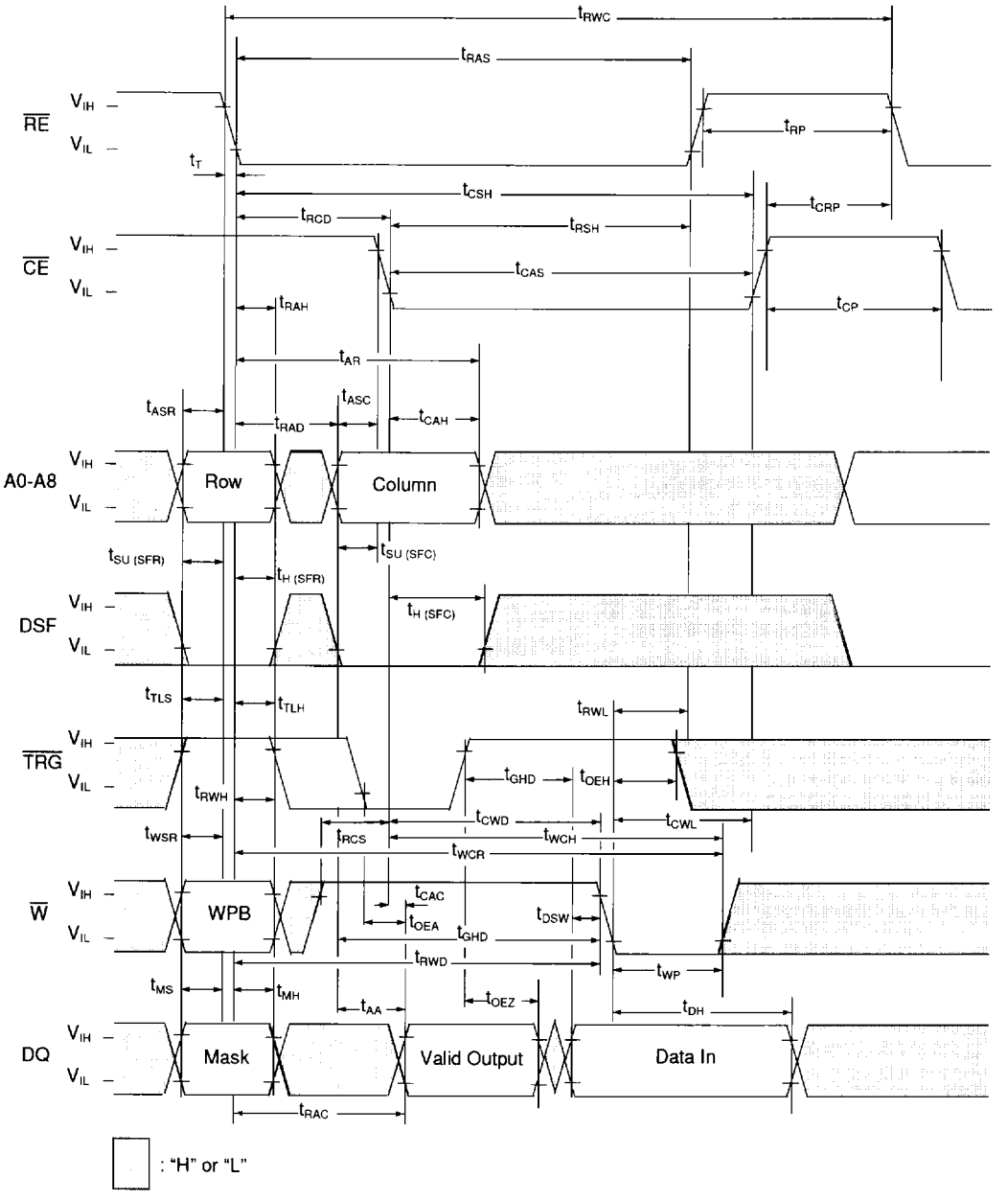
Write Cycle (Early Write)



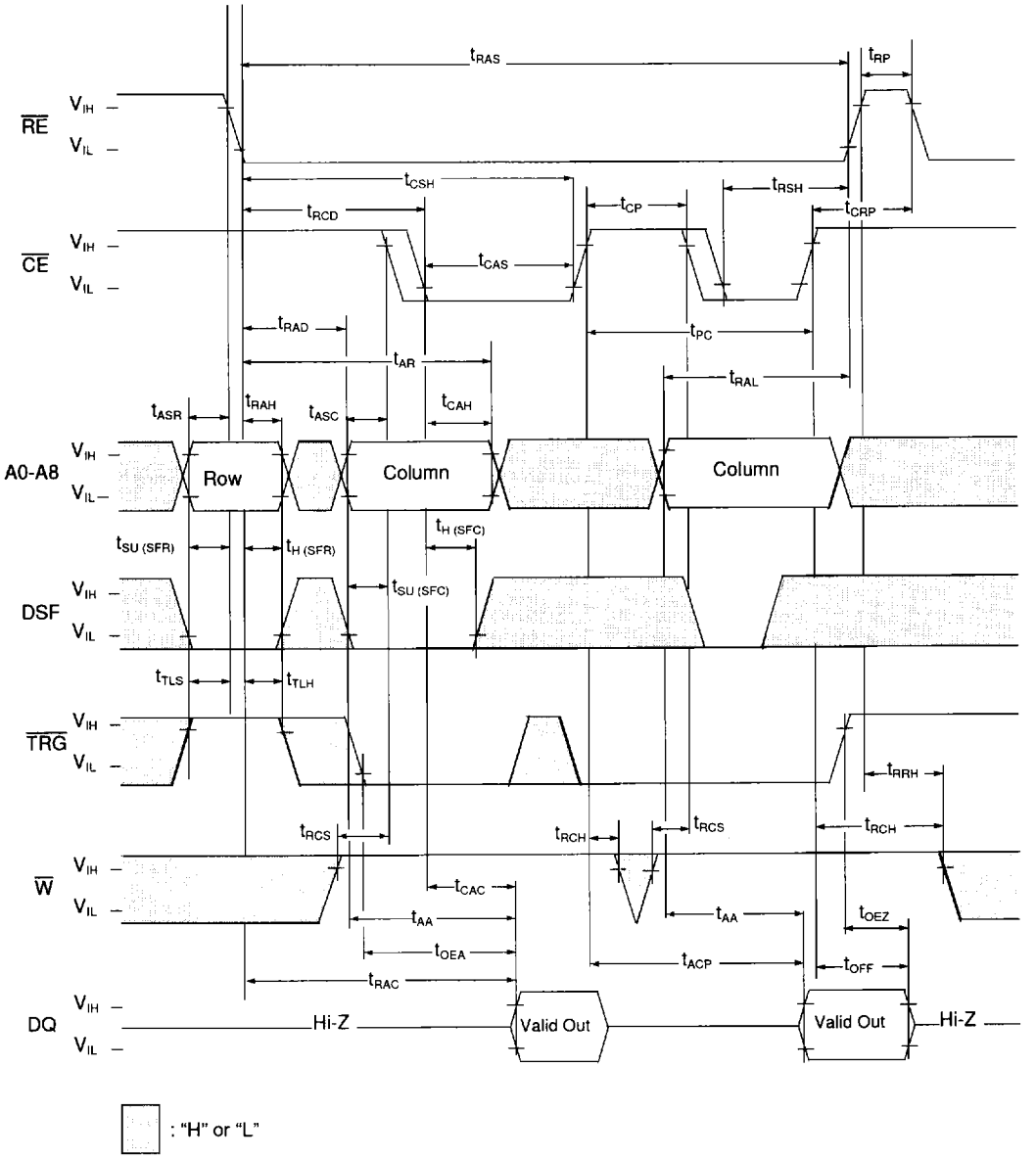
Write Cycle (Late Write)



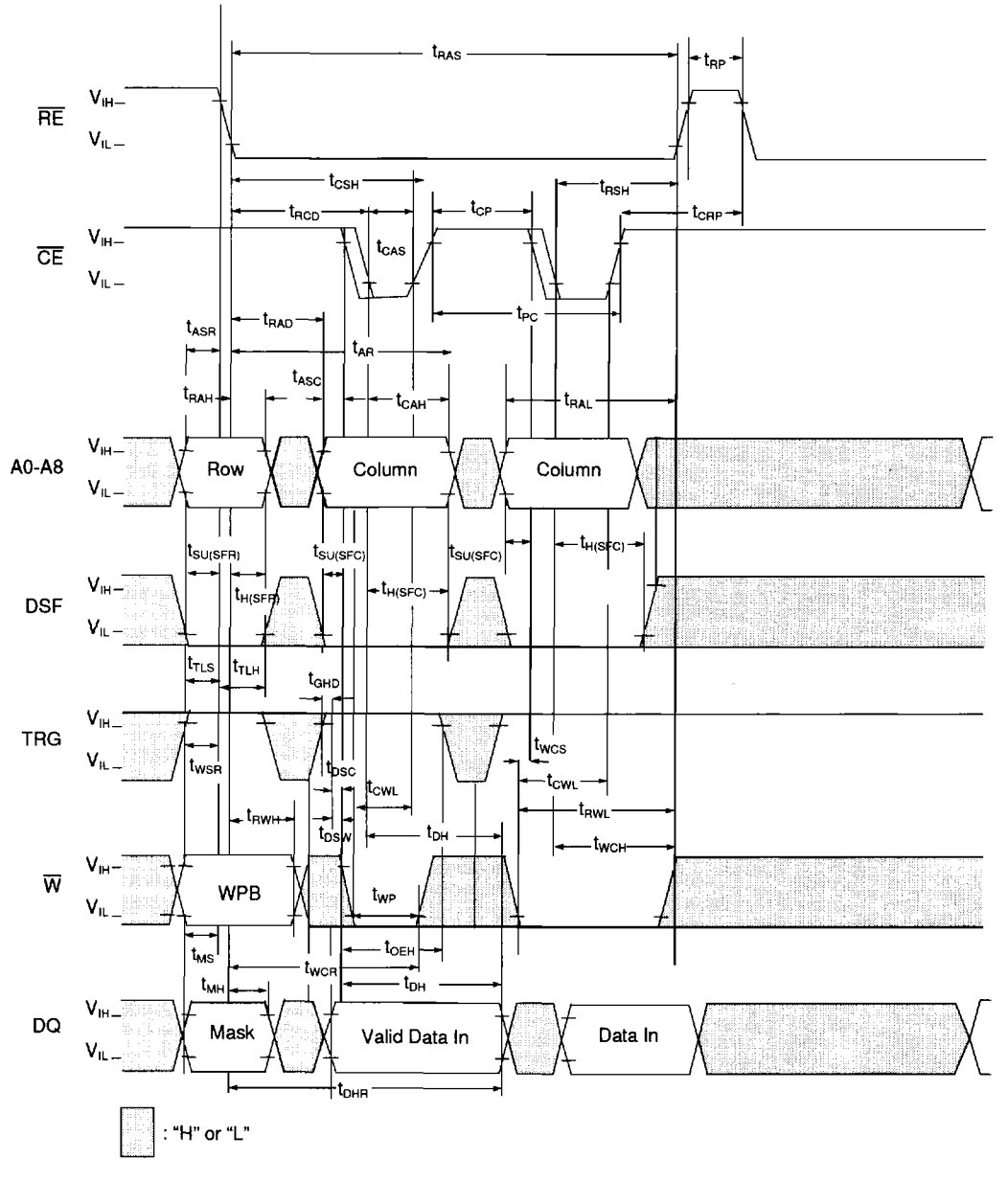
Read-Modify-Write Cycle



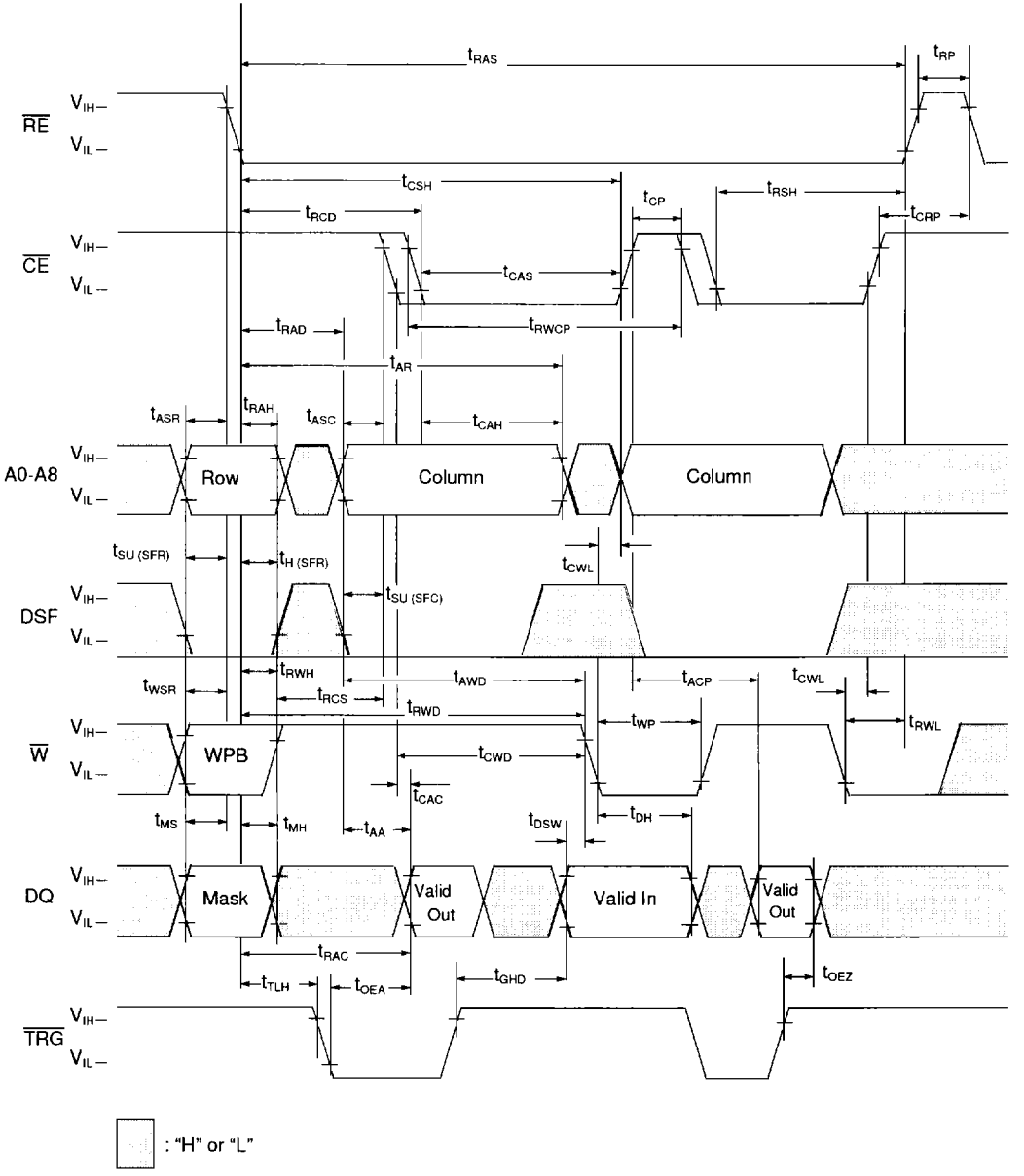
Fast Page Mode Read Cycle (Note: t_{CAL}, t_{ASC}, t_{CAH}, apply to all page mode cycles.)



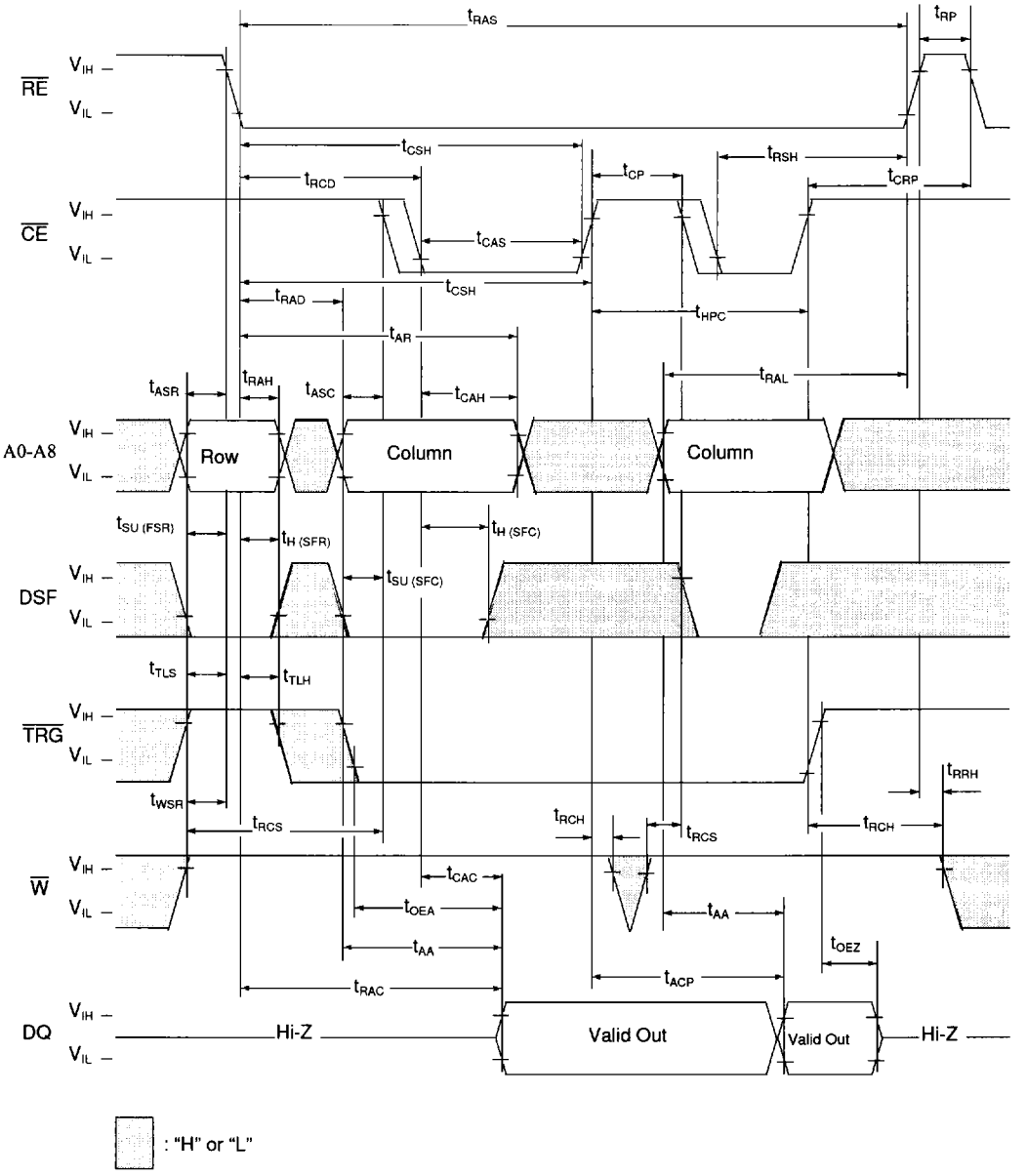
Fast Page Mode Write Cycle (Note: t_{DSC} must be met on early write cycles. t_{DSW} must be met on late write cycles.)



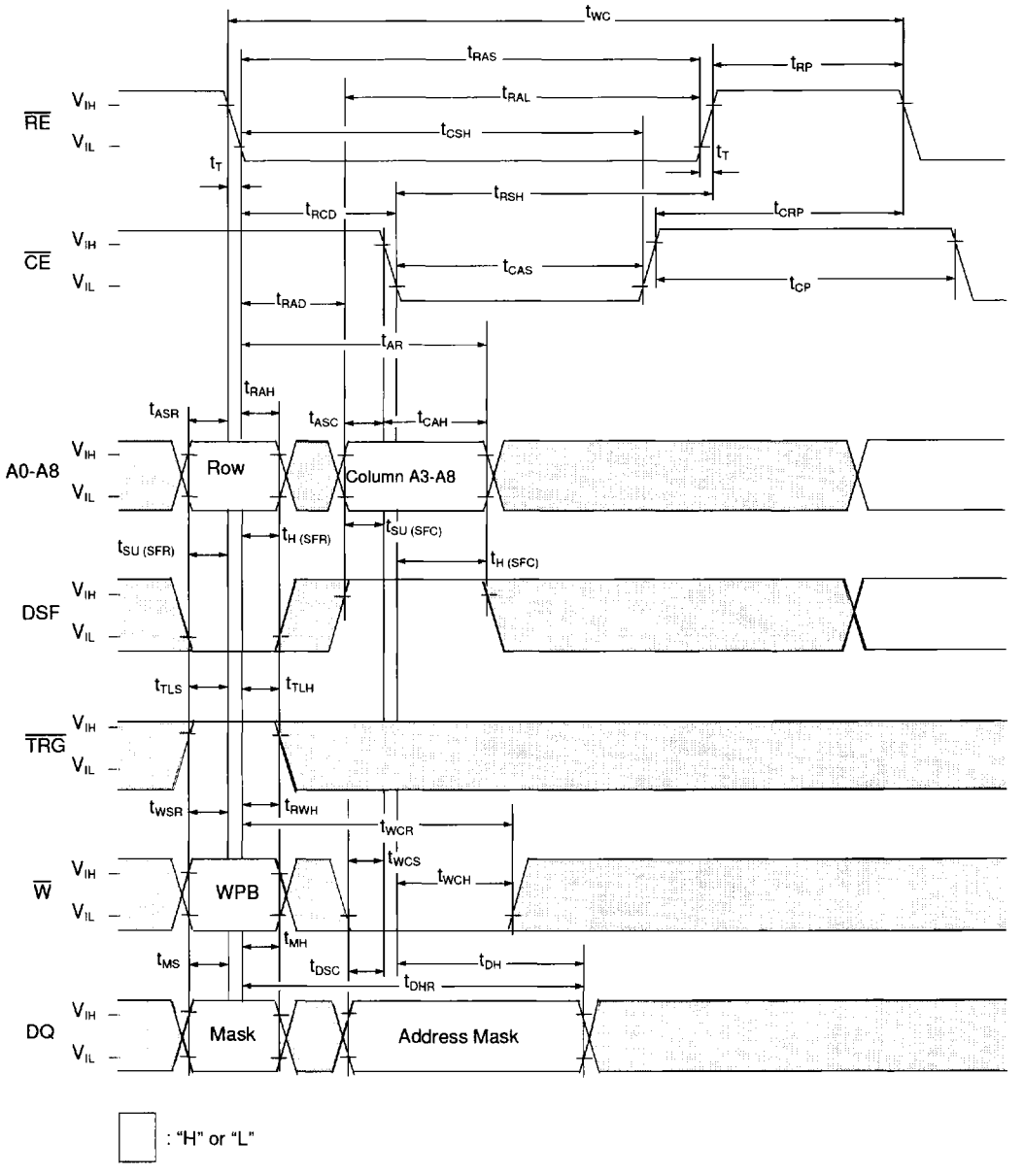
Fast Page Mode Read-Modify-Write Cycle



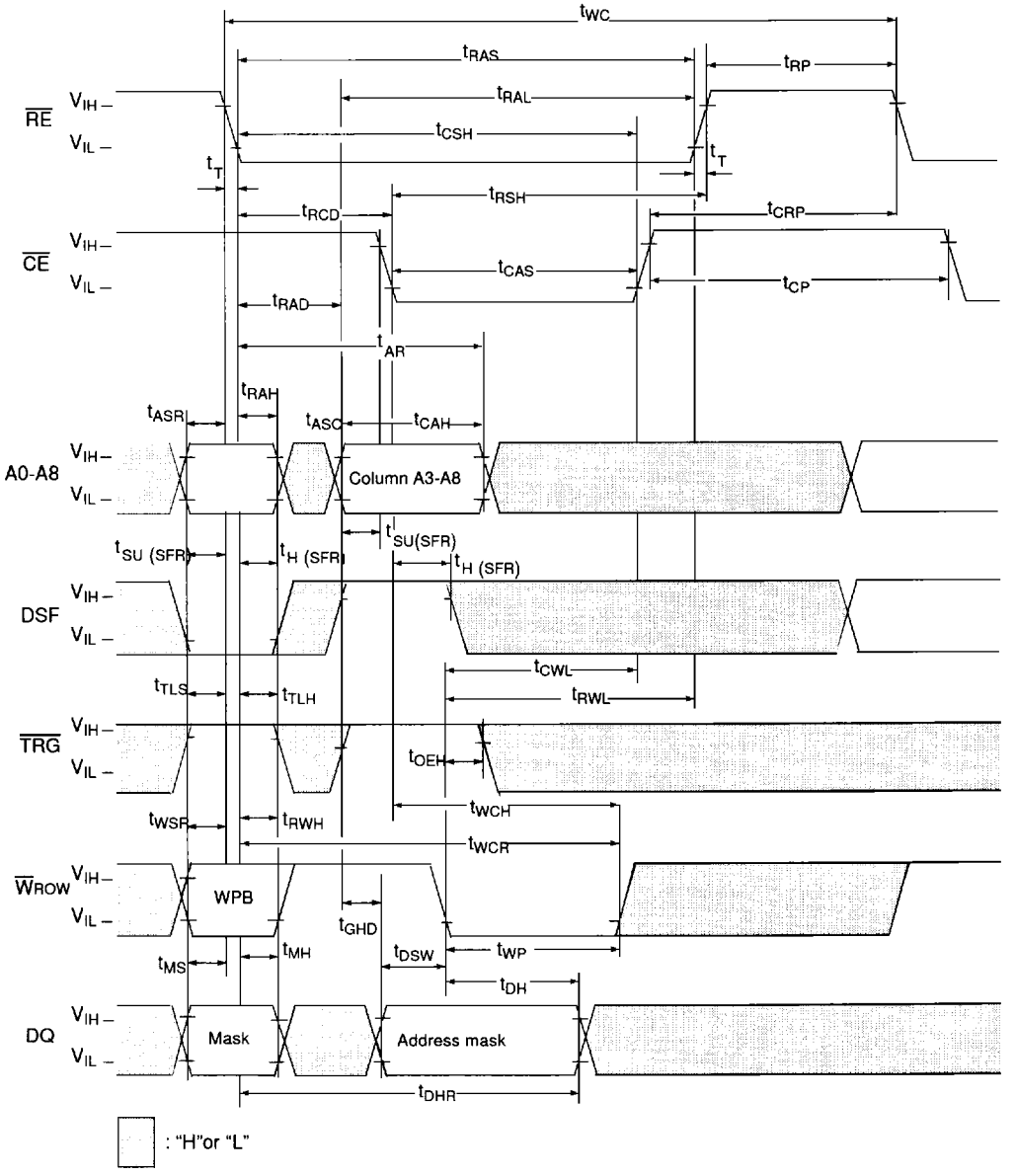
Extended Data Out Read



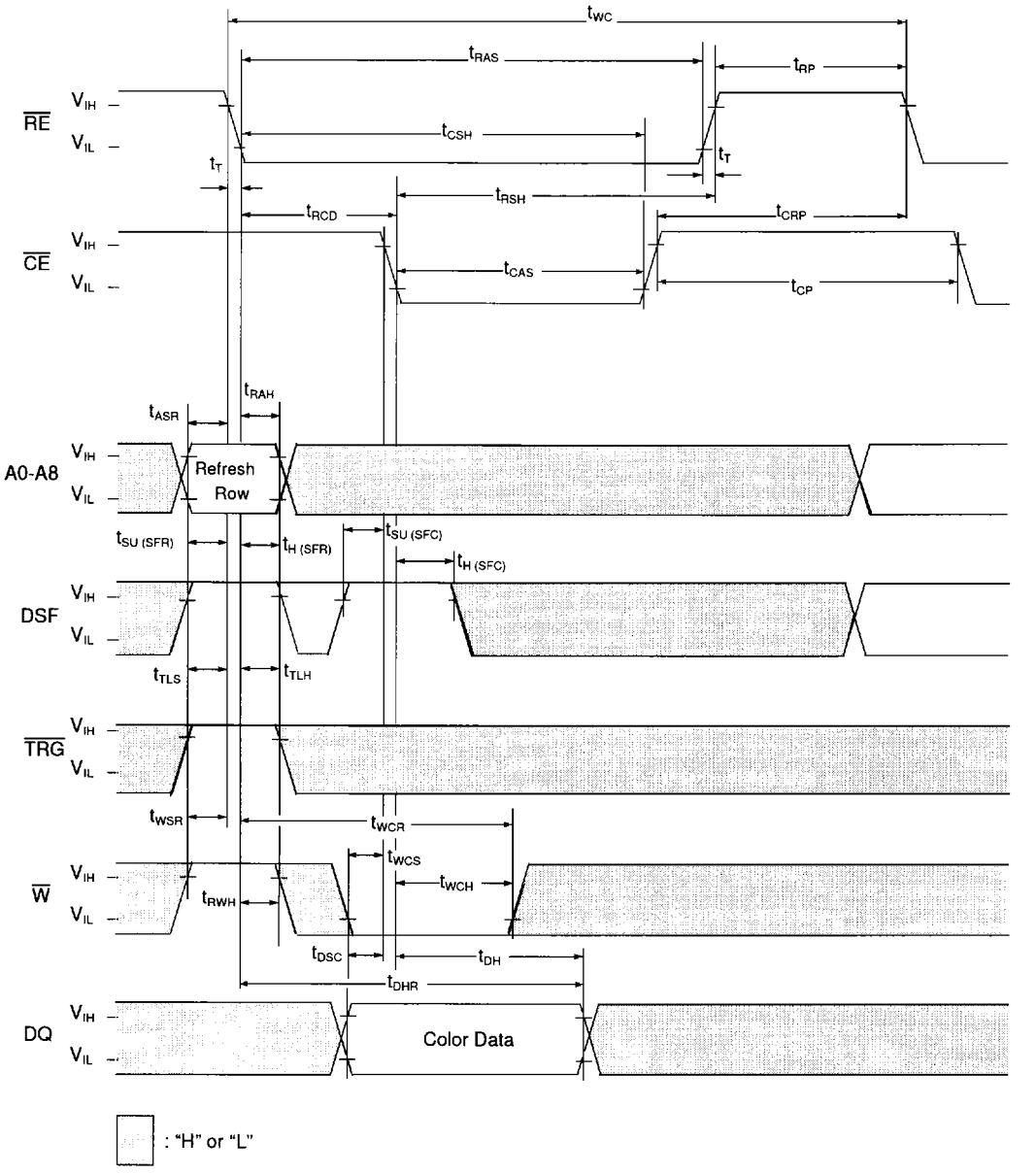
Block Write (Early Write)



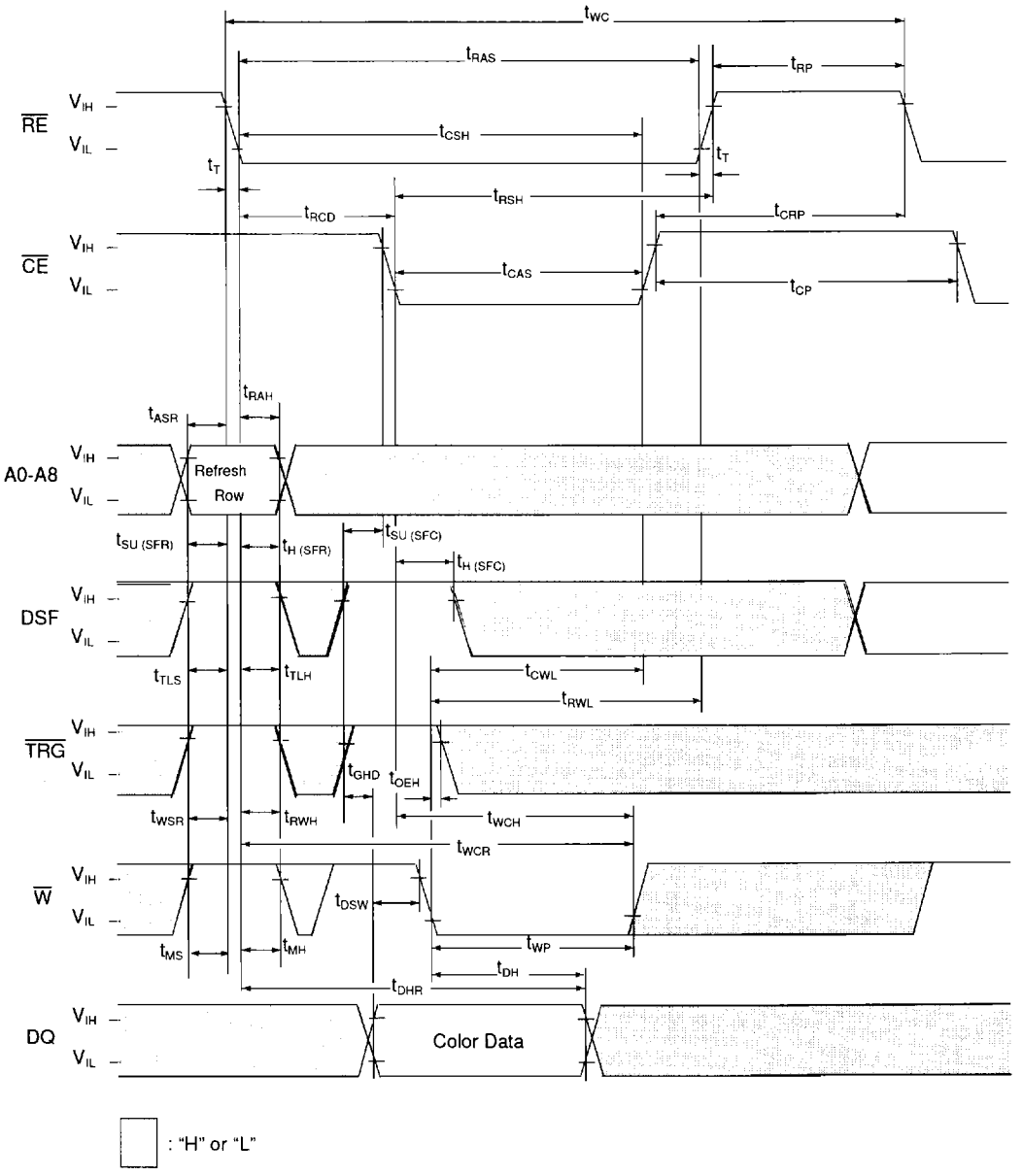
Block Write Cycle (Late Write)



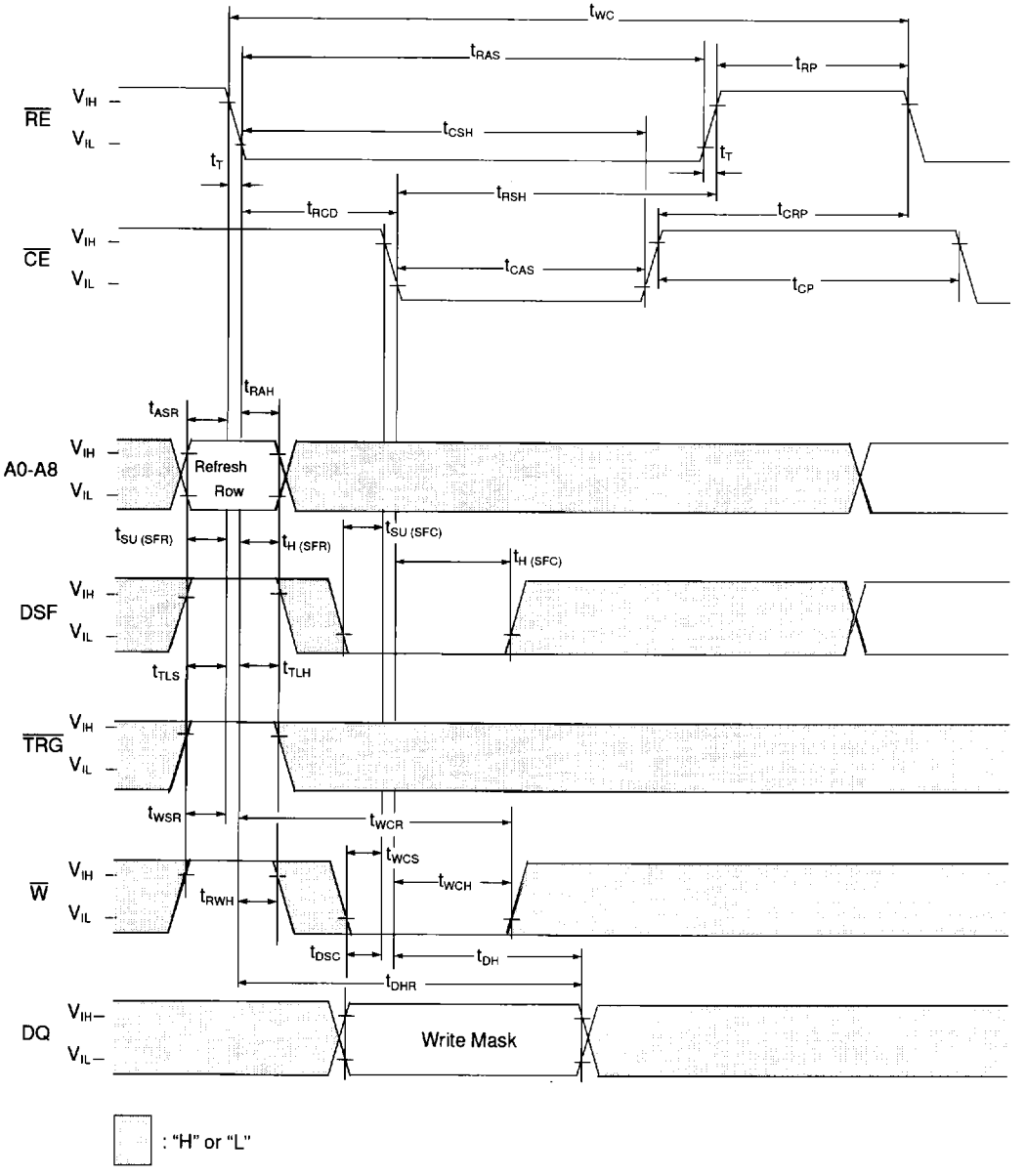
Load Color Register (Early Load)



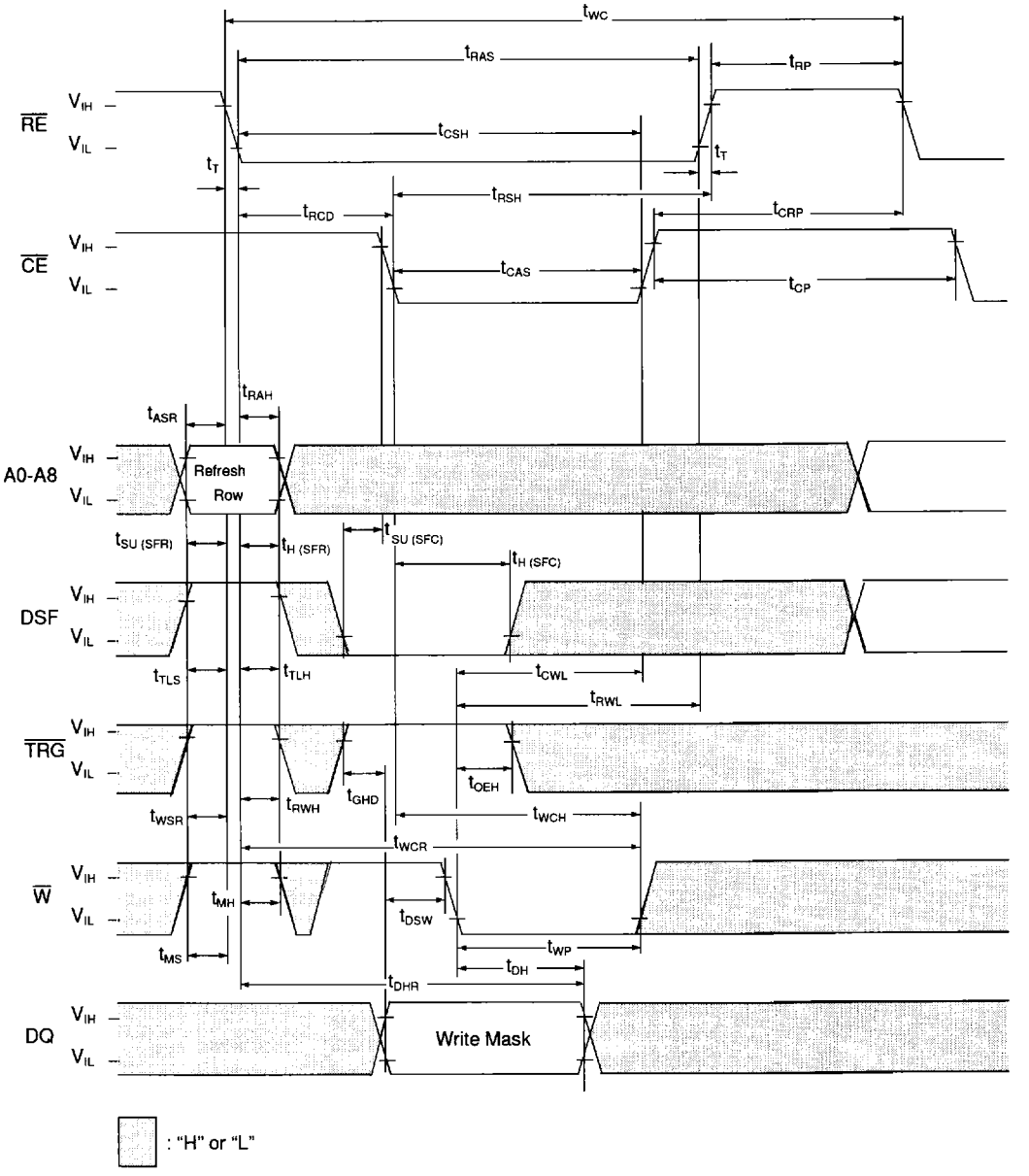
Load Color Register (Late Load)



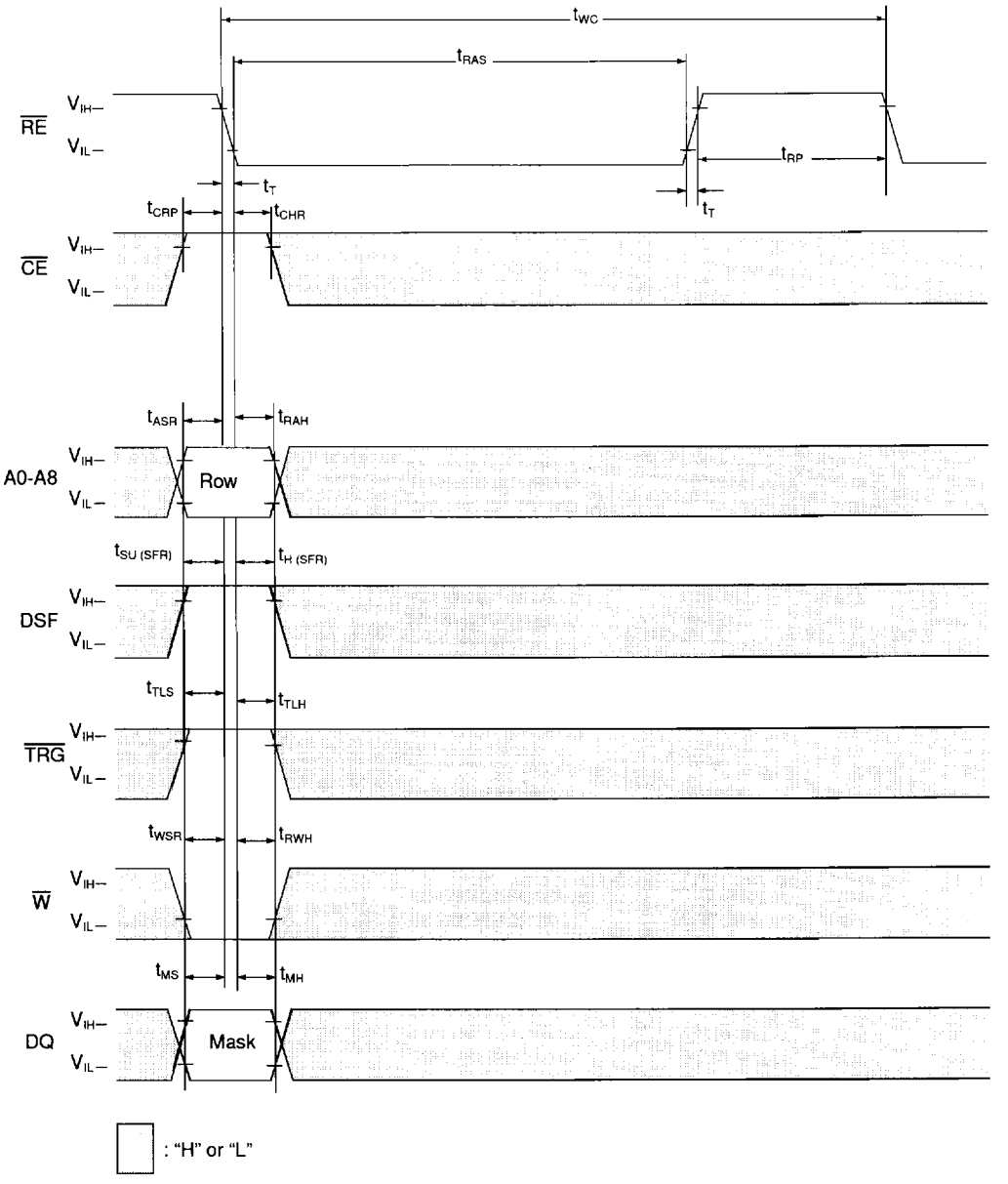
Load Mask Register (Early Load)



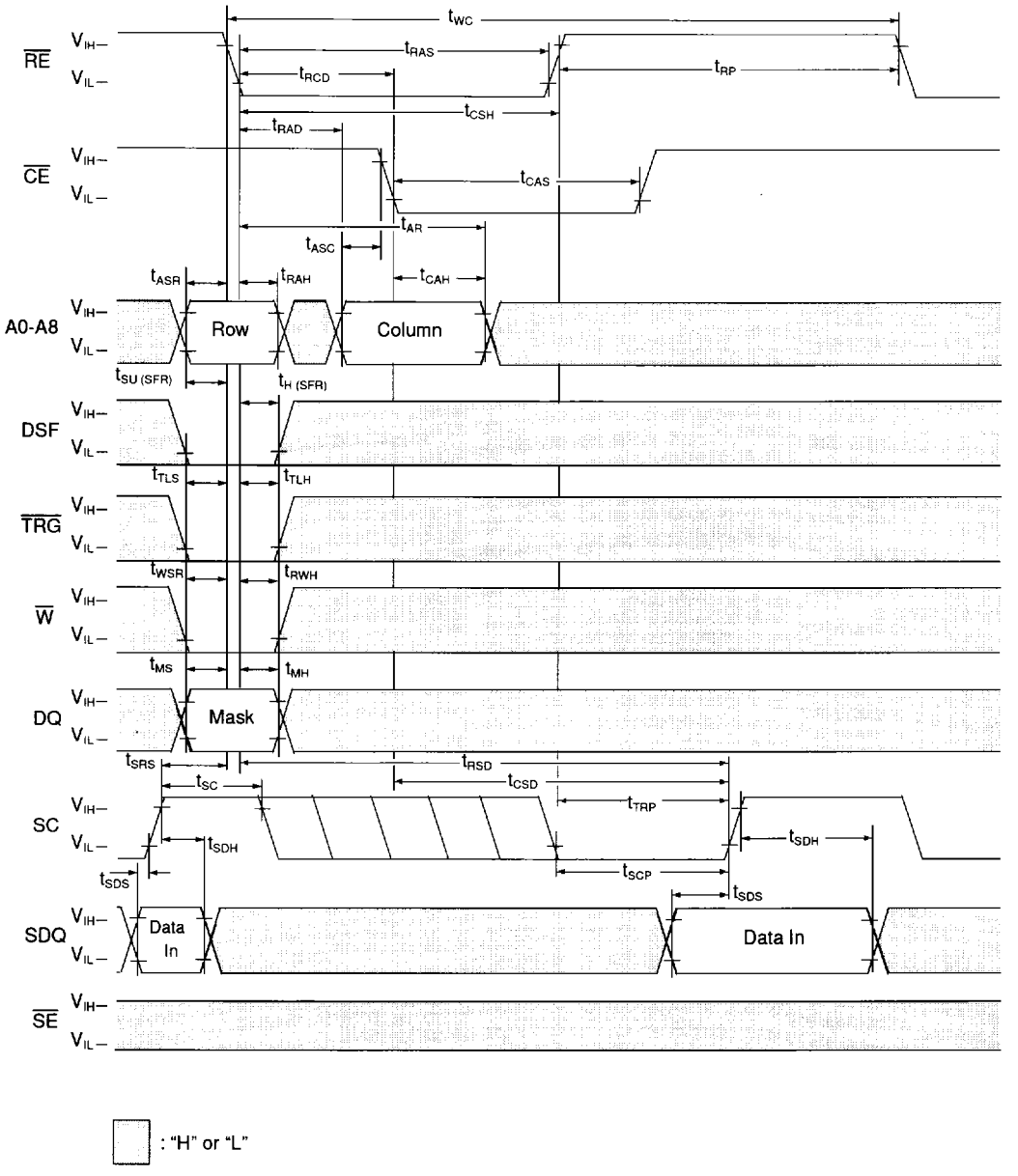
Load Mask Register (Late Load)



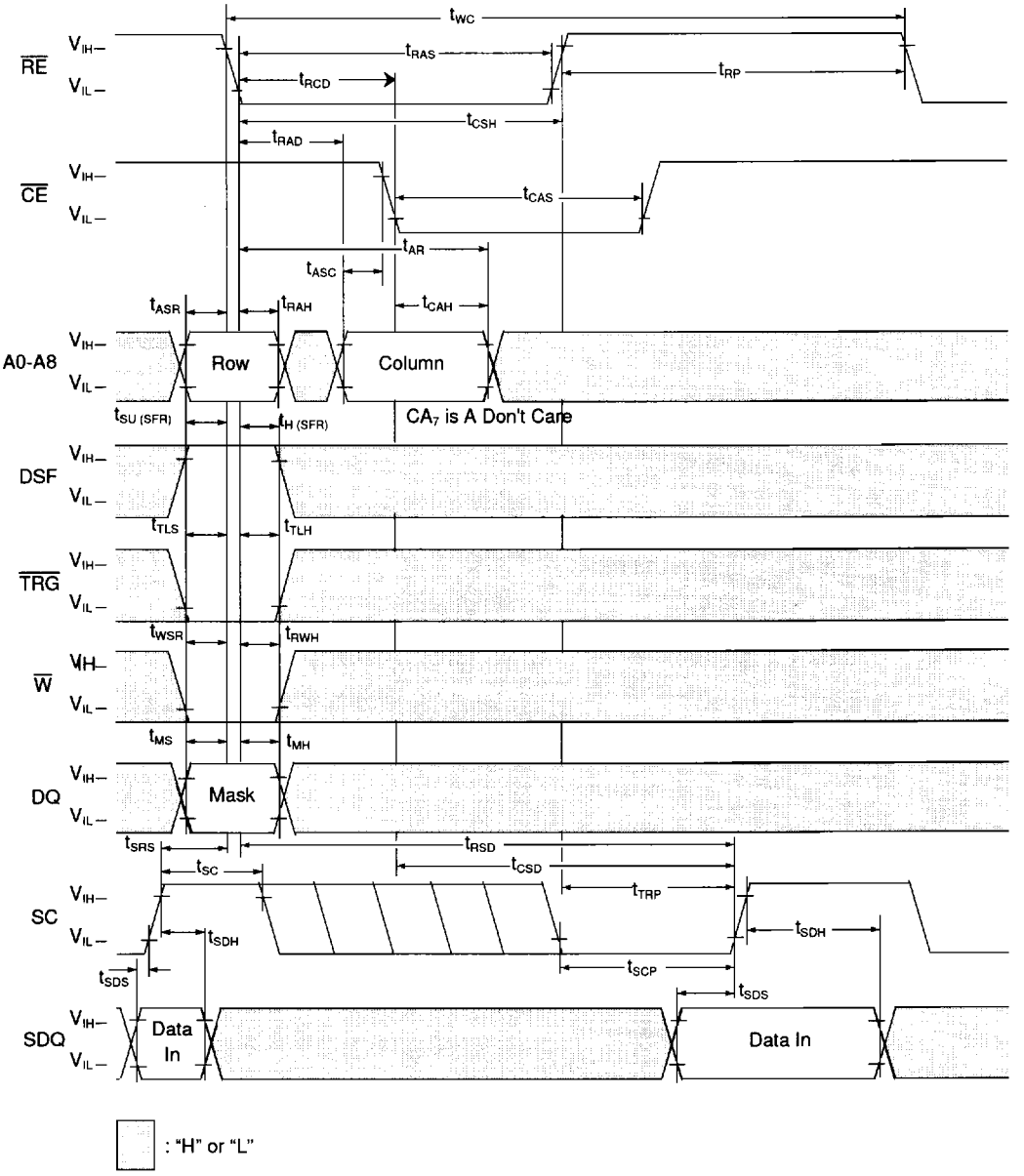
Flash Write Cycle



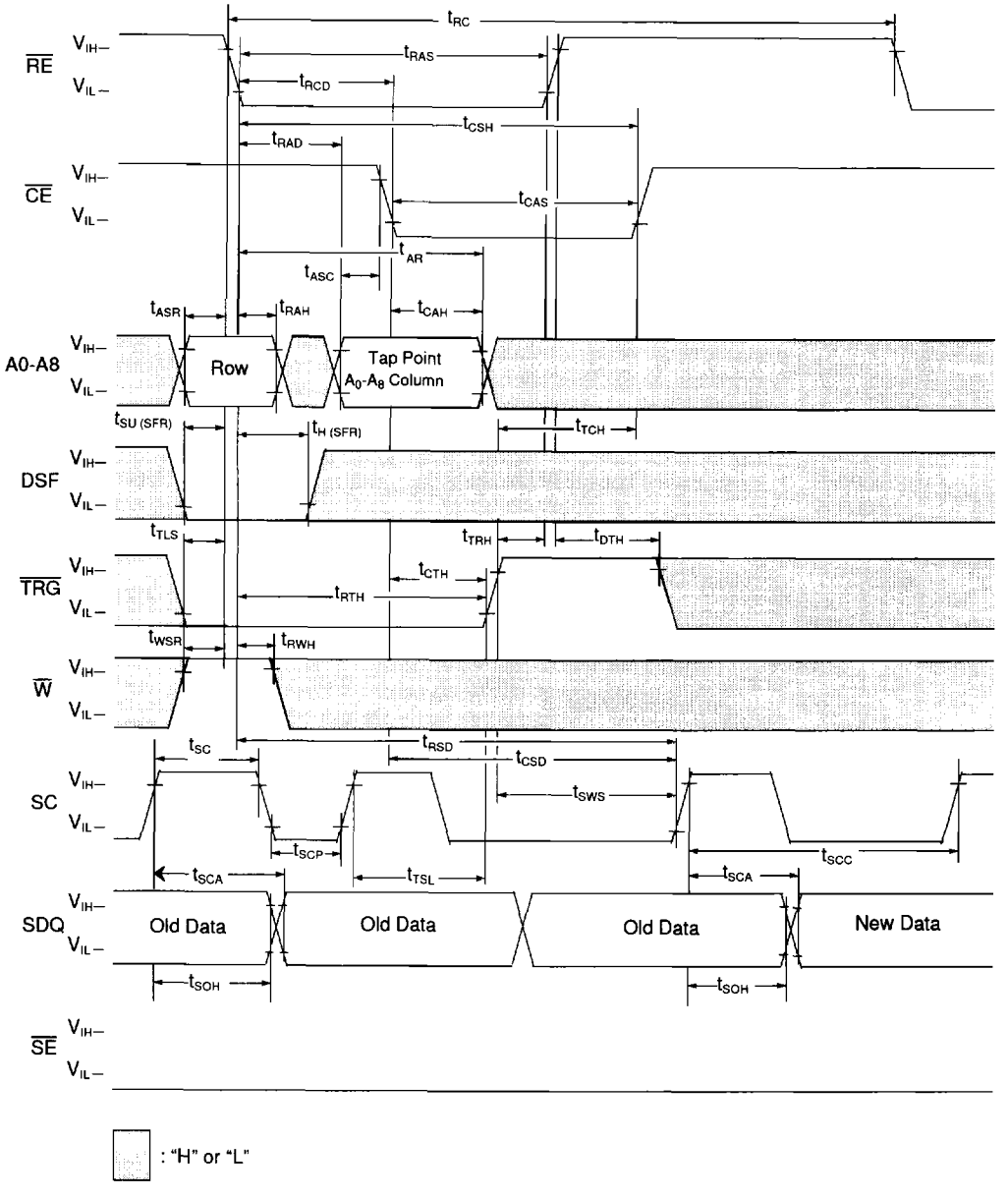
SAM → RAM Data Transfer



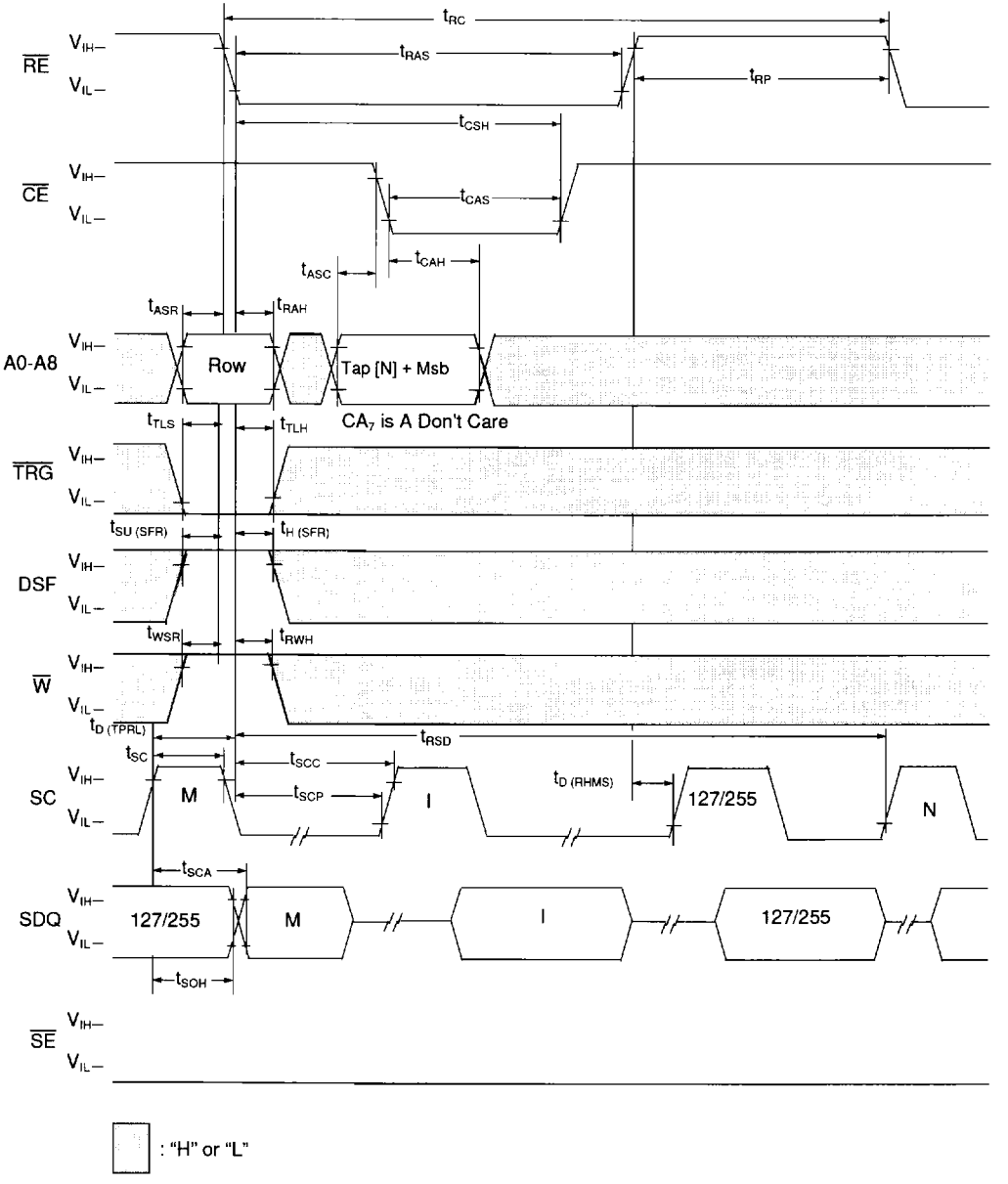
Split Write Transfer Timing



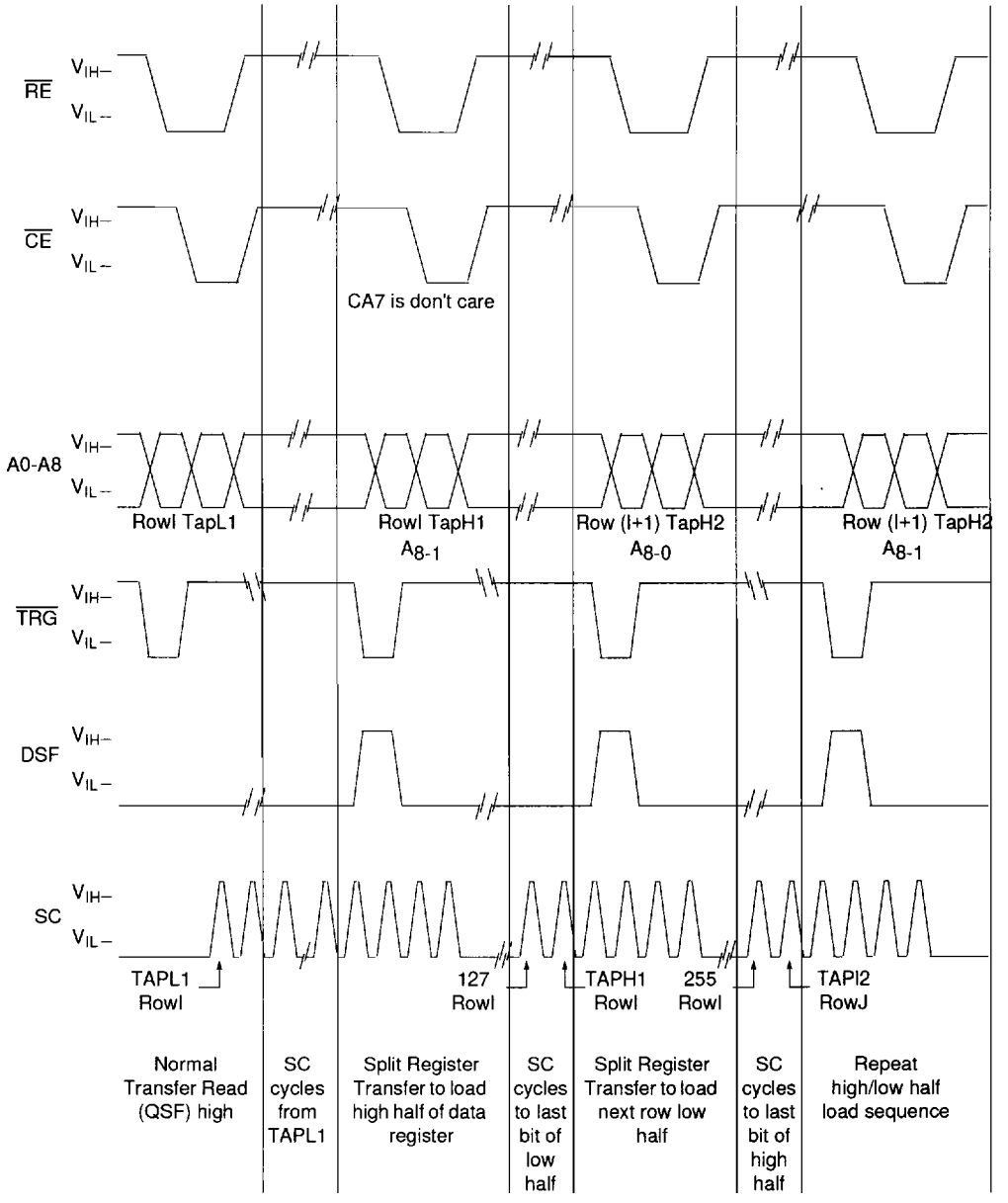
RAM → SAM Data Transfer



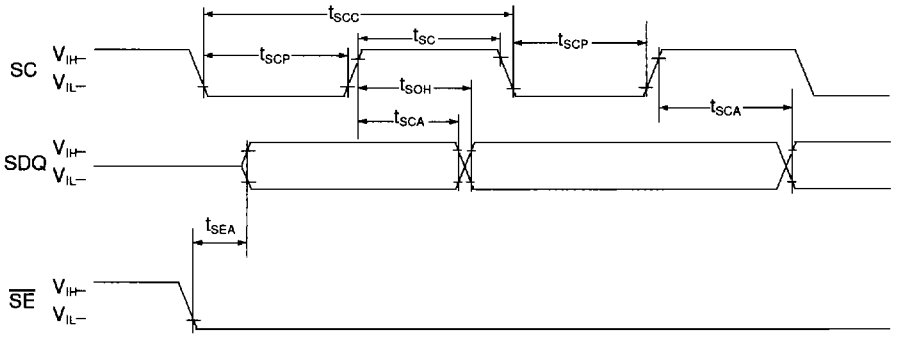
Split Read Transfer Timing



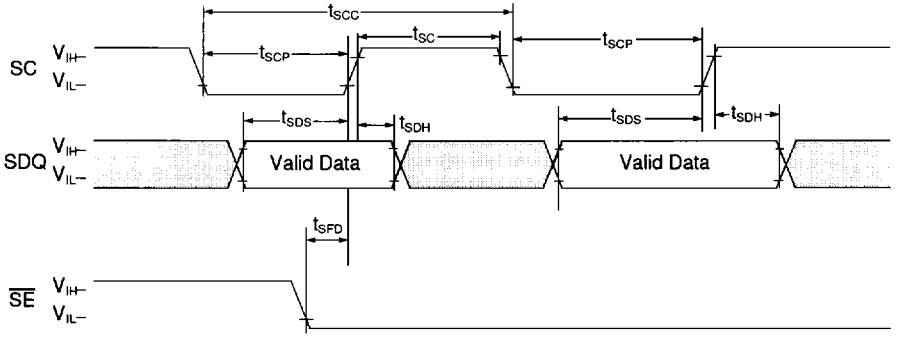
Split Register Operating Sequence



Serial Read

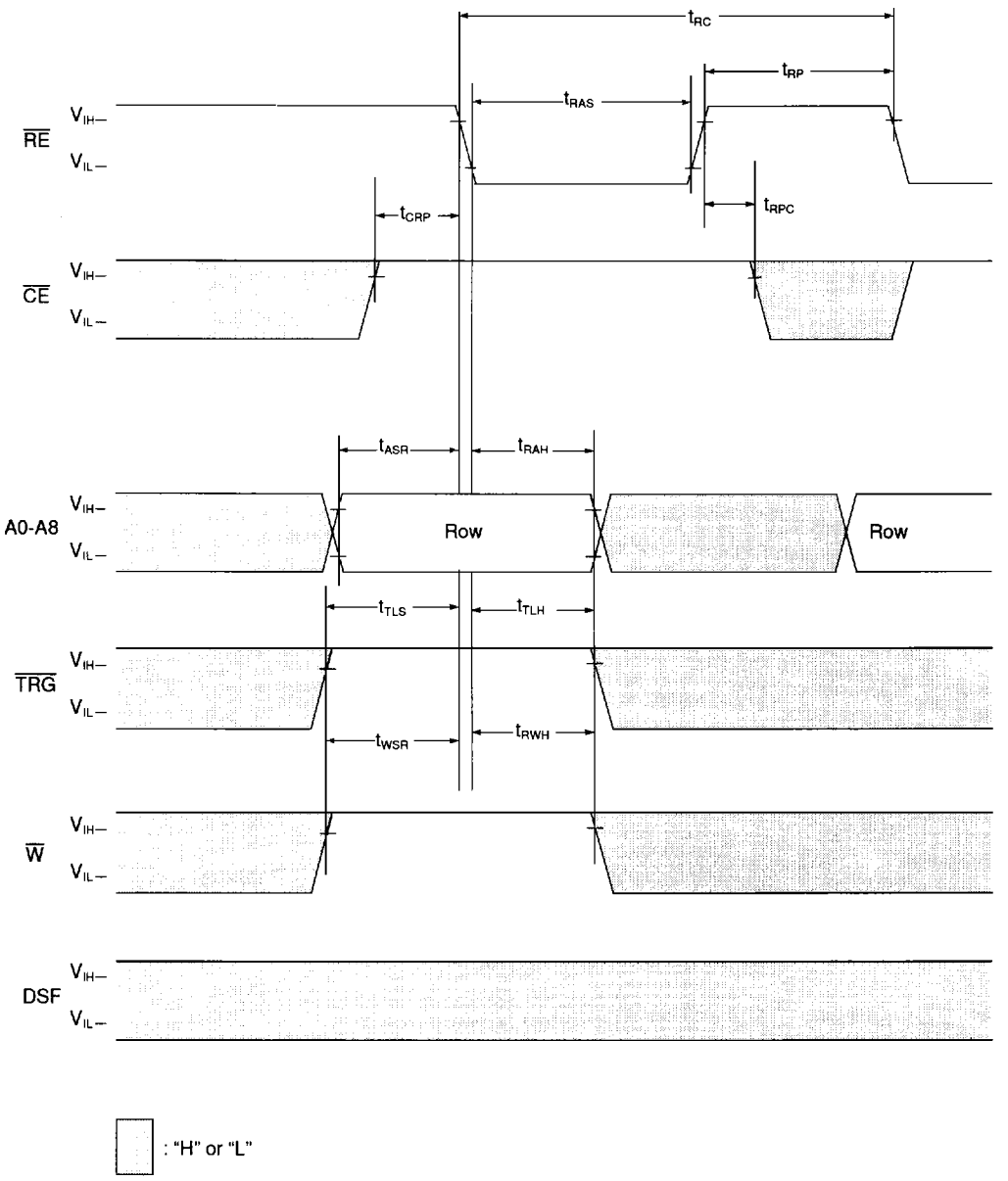


Serial Write

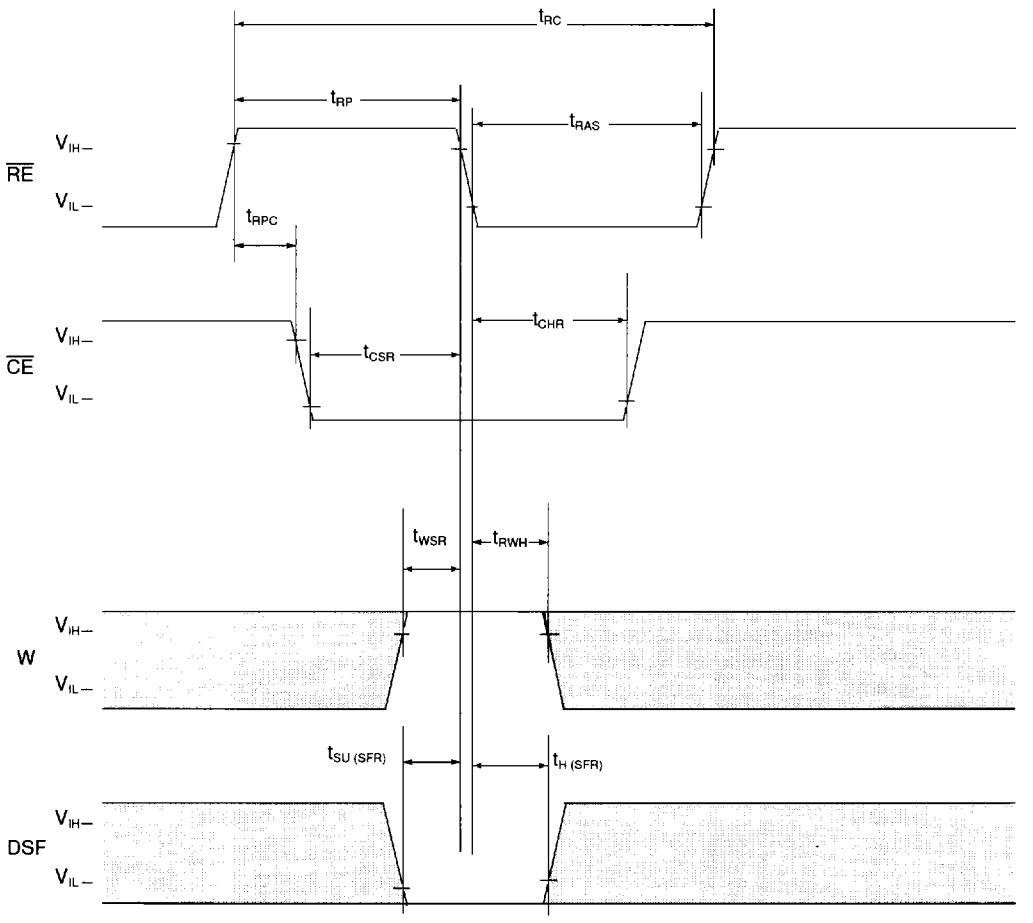


: "H" or "L"

$\overline{RE}$ Only Refresh

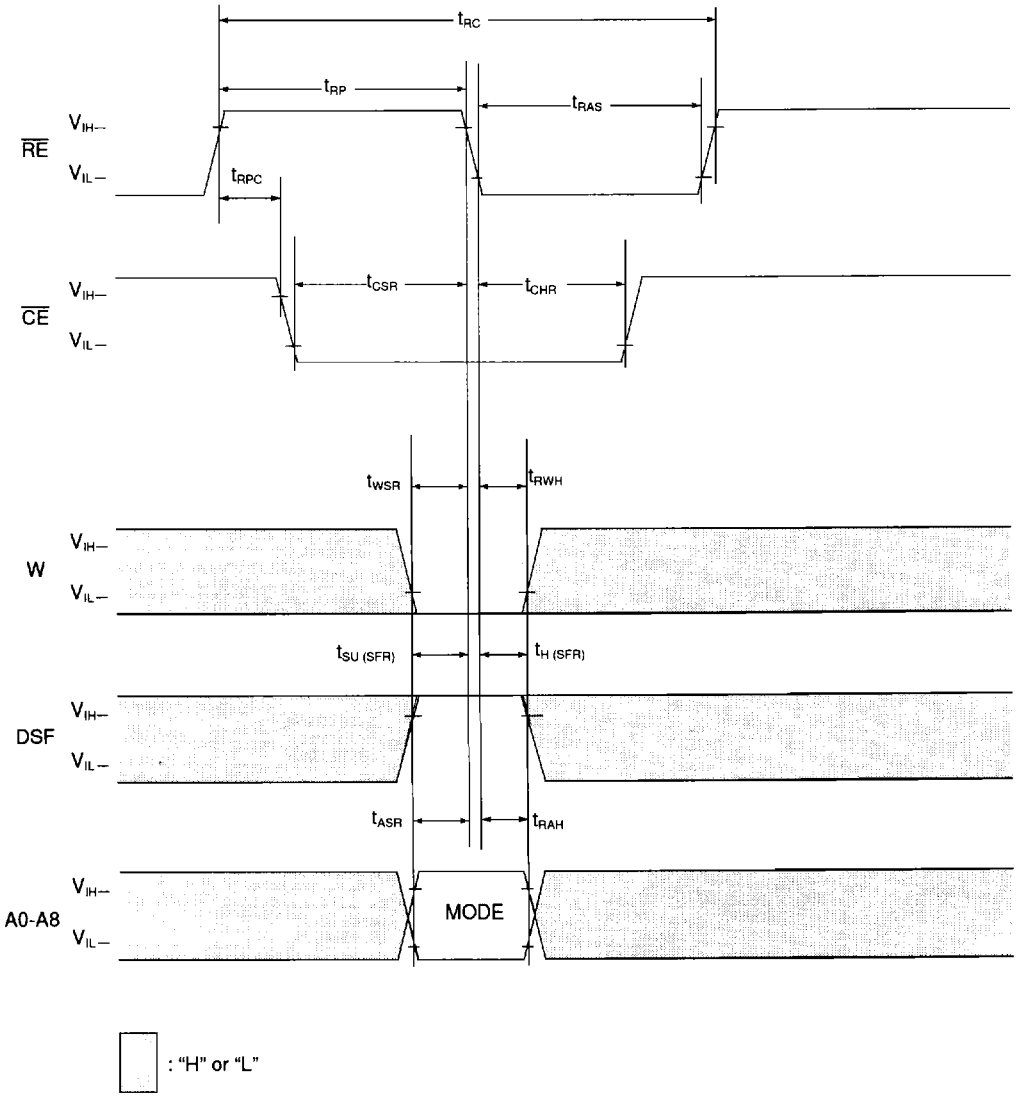


$\overline{CE}$ Before $\overline{RE}$ Refresh (CBR-with Mode Reset)

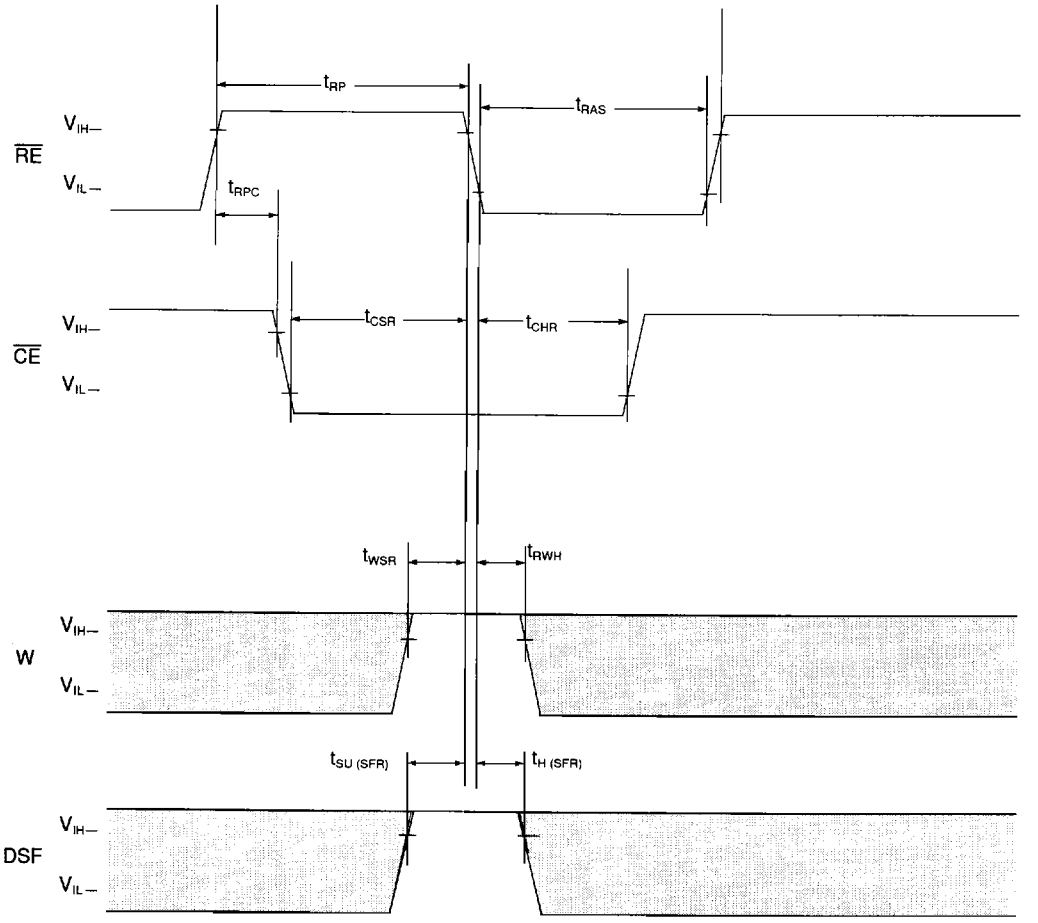


: "H" or "L"

$\overline{CE}$ Before $\overline{RE}$ Refresh (CBRS-with Mode Set)

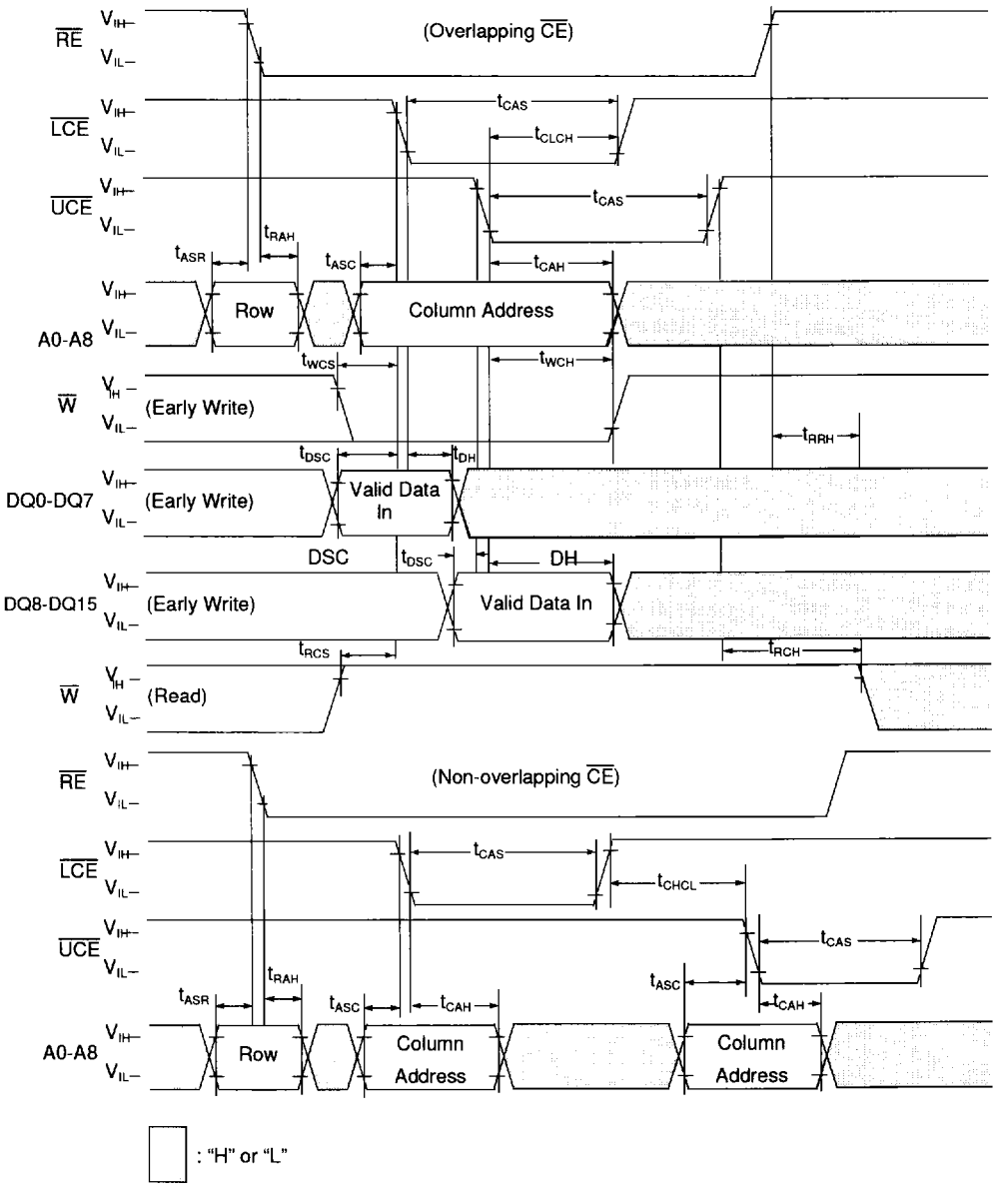


$\overline{CE}$ Before $\overline{RE}$ Refresh (CBRN-No Mode Reset)

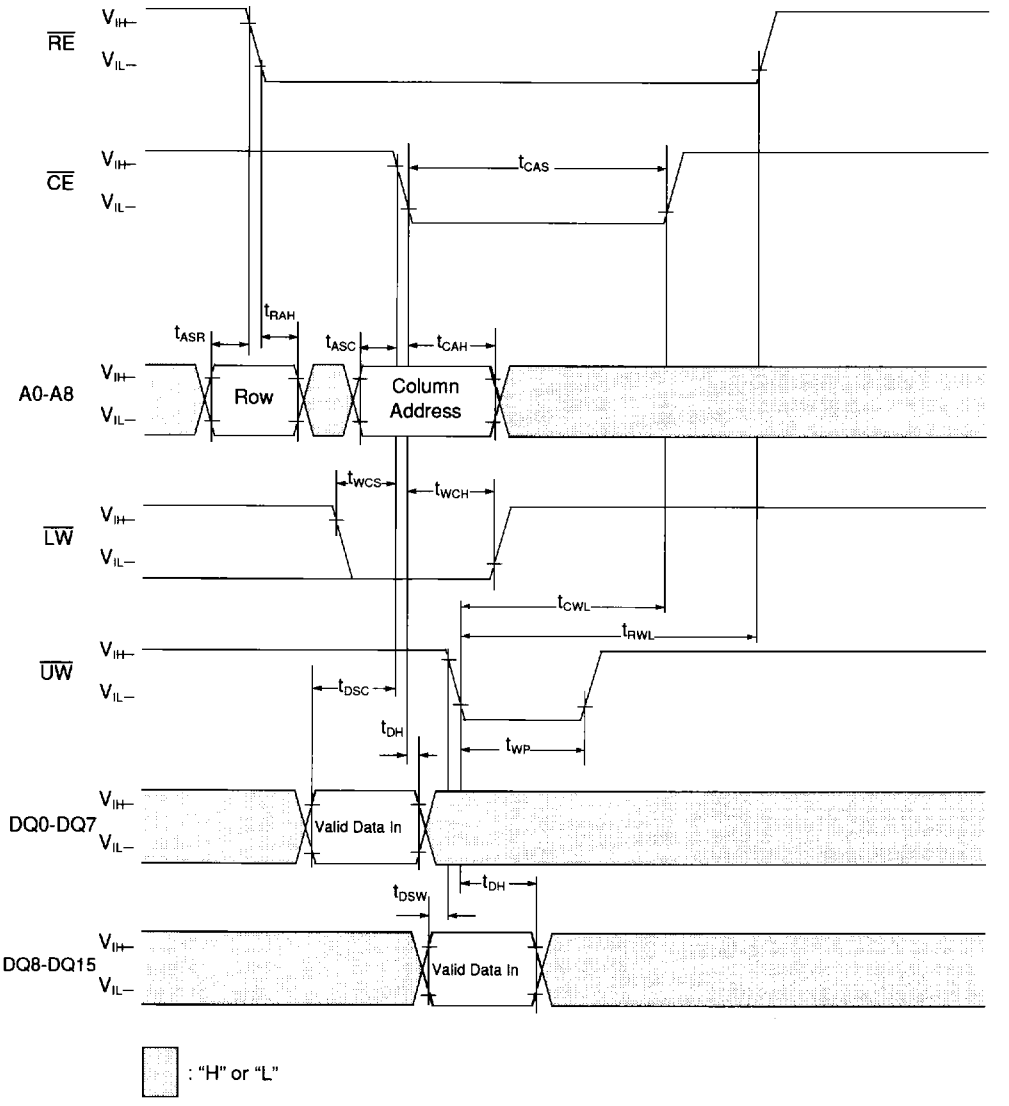


: "H" or "L"

Skewed $\overline{CE}$



Skewed $\overline{W}$



Functional Description

The primary port is organized 512 rows by 512 columns by 16 bits wide. The chip is capable of performing the standard set of Dynamic Random Access Memory (DRAM) functions as well as the VRAM specific functions: read transfer, split read transfer, write transfer, split write transfer, block write, flash write, and extended data out.

Half of the 512x16 bits in any given row can be loaded, based on column address CA_8 (or CA_7 in SRS mode) into the 4096 bit Serial Access Memory (SAM) that is organized 256x16. The SAM positions are mapped to the eight low order column addresses with CA_0 being the lowest order address bit and CA_7 being the highest order address bit. In full transfer with SRS mode, the SAM is mapped to address CA_8 and CA_6 to CA_0. CA_7 is used to choose the half of the row that is loaded. Once data is loaded, the SAM can be accessed serially starting with the start address register, TAP. The register is loaded with the address specified by CA_7-CA_0 during the $\overline{CE}$ portion of the full and split transfer cycle.

The truth table lists the logical condition of the input signals to invoke the primary port and the transfer operation. $\overline{WE}$ at $\overline{RE}$ time controls whether write cycles and write transfer cycles are to be masked. $\overline{TRG}$ at $\overline{RE}$ time controls whether the $\overline{RE}$ cycle will be a transfer cycle or a normal DRAM cycle.

Primary Port Operations

All primary port operations are initiated by holding the $\overline{TRG}$ pin high and bringing the $\overline{RE}$ pin low. The exception to this rule is the $\overline{CE}$ before $\overline{RE}$ operation in which $\overline{TRG}$ pin is ignored. The specific primary port operation to be executed is defined by the state of the $\overline{CE}$, $\overline{W}$, DSF, at the falling edges of $\overline{RE}$ and $\overline{CE}$. The truth table shows the logic conditions required to perform a specific primary port operation.

Both primary port write cycles and write transfer cycles can be optionally masked with the WPBM. If either $\overline{UW}$ or $\overline{LW}$ is low at $\overline{RE}$ time, the 16 bits present on the DQ_i pins are loaded into the WPBM register. Any write operation is blocked for each DEI whose corresponding bit in the WPBM register is 0.

Please note the following rules for dual $\overline{CE}$ operation:

1. The earlier falling edge is used for latching addresses and DSF and for measuring t_{CP}.
2. The later rising edge is used for measuring t_{CPA} and t_{CP}.
3. All other timing parameters must be met considering each $\overline{CE}$ individually.

$\overline{CE}$ Before $\overline{RE}$ Refresh (CBR)

The CBR operation is selected by bringing $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping DSF low. An internal address counter selects the row address to be refreshed. This cycle will reset any special modes set by the CBRS cycle.

$\overline{CE}$ Before $\overline{RE}$ Refresh with mode set (CBRS)

The CBRS operation is selected by bringing $\overline{W}$ and $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping DSF high. An internal address counter selects the row address to be refreshed.

This cycle is used to set the chip into specialized modes. SRS is available to modify the operation of the inter-

nal serial port address counter and to modify the mapping of primary port address to the SAM. Full compatibility is provided between half and full depth SAM by performing split transfer in SRS mode of 128 or less.

In SRS mode, CA7 and CA8 are internally swapped to allow full compatibility between half depth SAM (256 x 16) and full depth SAM (512 x 16). A read/write performed to an address in normal cycle will not be identical to a read/write performed to the same address in SRS mode due to internal address swapping. Further discussion on SRS mode is provided in section title Transfer Operations.

The state of the A_i pins selects the mode the chip is set to as specified in the table title User Modes. After power-on, the chip is set to SRS mode off (jump address set to 128). Any mode changes are retained until power-off or until reset by a CBR cycle. A CBR cycle must be implemented once to clear any modes that may have been set inadvertently at power up before a CBRS cycle is used.

User Modes

No	Description	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	Select SRS mode and set serial boundary to 16	X	0	0	0	0	1	1	X	X
2	Select SRS mode and set serial boundary to 32	X	0	0	0	1	1	1	X	X
3	Select SRS mode and set serial boundary to 64	X	0	0	1	1	1	1	X	X
4	Reset boundary address to 128	X	0	1	1	1	1	1	X	X

$\overline{CE}$ Before $\overline{RE}$ Refresh without mode reset (CBRN)

The CBRN operation is selected by bringing $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping DSF and $\overline{W}$ high. The internal address counter selects the row address to be refreshed. This cycle will not reset any special modes set by the CBRS cycle.

Read/Write Cycles

All normal DRAM cycles can be performed through the primary port including page mode, early and late write, and read-modify-write. In a read operation, the chip will read the 16 bits addressed by RA_8-RA_0 and CA_8-CA_0, on the DQ_i pins. A write operation is performed at the given address if either $\overline{W}$ is brought low at the appropriate time as shown in the timing diagrams. The data on the DQ_i pins is written (subject to the write-per-bit mask) at the specified row and column address. If only one of the $\overline{W}$ is brought low then only that byte is written.

Early Write Cycle

$\overline{W}$ is low before $\overline{CE}$ fall for early write. The input data is strobed by $\overline{CE}$ with setup and hold time referenced to this signal.

Late Write Cycle

$\overline{W}$ is brought low after $\overline{CE}$ goes low. The input data is strobed by $\overline{W}$ with setup and hold times referenced to this signal.

Read-Modify-Write cycle

A read-modify-write is performed by first doing a normal read, tri-stating the DQ_i pins with $\overline{TRG}$, placing data

to be written on the DQ_i pins, and then signaling a write operation by bringing either $\overline{W}$ low. A write-per-bit mask (WPBM) can be loaded at falling edge of $\overline{RE}$. The data out is strobed in reference to $\overline{CE}$. During a write, data-in is strobed in reference to $\overline{W}$.

Load Color Register (LCR) Cycle

The load color register cycle is used to load the 16 bit color register which is used for data-in during flash write and block write operations. At $\overline{RE}$ fall, the address is used as refresh address. Refer to truth table for the state of the input pins needed to select the LCR cycle.

Load Non-Persistent Write-Per-Bit Mask

Write-per-bit mask is loaded from the DQ_{15}-DQ_0 when $\overline{W}$ is low at the falling edge of $\overline{RE}$.

Load Persistent Write-Per-Bit Mask Cycle (WPBM)

The load persistent mask cycle loads the write-per-bit mask registers and enables the persistent write-per-bit mask function. This write mask is then functional on Block, Flash, Write Transfer, Split Write Transfer, and Write cycles. In this mode, the data on the DQ_i pins at $\overline{RE}$ fall is ignored. The chip will remain in persistent write-per-bit mode until a CBR cycle is performed. The chip will then be in the non-persistent write-per-bit mode. Refer to truth table for the state of the input pins needed to select the LMR cycle.

Fast Page Mode Cycles

Fast page mode cycles allow faster memory access by using the same row address while successive column address are strobed onto the chip. Fast page mode read, write, read-modify-write can be executed. Write-per-bit mask can be provided at $\overline{RE}$ which is maintain throughout the next fast page mode write cycle. In fast page mode read, the DQ_{15}-DQ_0 are in high impedance state until valid data out at access time.

Extended Data Out

In extended data out mode, the primary port output drivers are not reset on the rising edge of $\overline{CE}$ during page mode cycle as shown in the timing diagrams. The mode operates as regular DRAM read or fast page mode read with data held valid after $\overline{CE}$ goes high as long as $\overline{TRG}$ and $\overline{RE}$ are low. When $\overline{RE}$ rises data is again controlled by the rising edge of $\overline{CE}$. Data out is turned off by the $\overline{TRG}$ pin and must be shut off before a write operation begins to drive data into the chip. Extended dataout does not require t_{OFF} parameter which allows faster page mode access. In dual $\overline{CE}$ control, the upper and lower bytes are individually controlled.

Flash Write

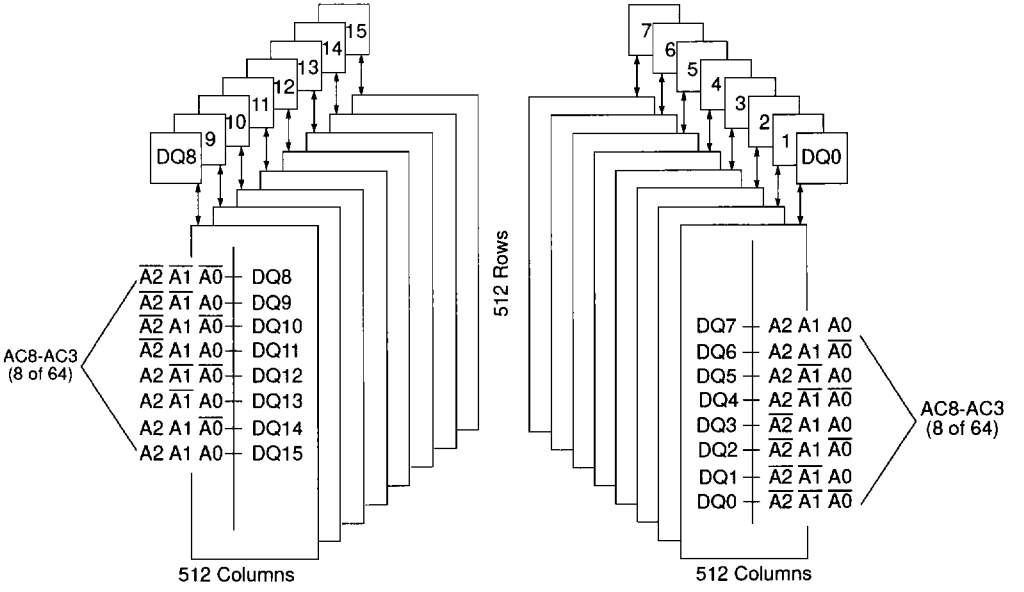
The Flash Write operation causes an entire row (512x16 bits) of data to be written with the contents of the color register. Each bit of the 16 bit color register supplies data for the corresponding DQ_i. The color register must be loaded on a previous LCR cycle (further description is provided in Load Color Register cycle). Note Flash Write is always write-per-bit, and therefore the WPBM can be used to mask writes to any given DQ_i. If the mask register is loaded, the mask is persistent; otherwise, the mask is non-persistent.

Block Write

The block write operation writes the color register at any or all of the 8 addresses specified by CA_8-CA_3 (CA_2-CA_0 are ignored). Data-in (DQ_{15} through DQ_0) is used to select which of the 8 column addresses are actually

stored and is referred to as the address mask for the block write operation. The DQ_i are divided into two bytes, L (DQ_7-DQ_0) and U (DQ_{15}-DQ_8). DQ_0 corresponds to the first address for byte L (CA_2-CA_0 being set to 000), DQ_1 corresponds to the second address for byte L (CA_2-CA_0 being set to 001), and so on. DQ_8 corresponds to the first address for byte U (CA2-CA0 being set to 000), DQ9 corresponds to the second address for byte U (CA_2-CA_0 being set to 001), and so on. The data in the color register is written to each address whose corresponding address mask bit is 1. The WPBM can be used to mask writes to any given DQ_i. Block write is illustrated in the following two figures.

Block Write



Byte Control

The 4Mb VRAM is available with either Dual $\overline{W}$ or Dual $\overline{CE}$. All primary port operations can be performed on both ports. A dual $\overline{CE}$ part has an upper and a lower $\overline{CE}$. The $\overline{UCE}$ and $\overline{LCE}$ allows individual byte control of the DQs during read and write operations. The $\overline{UCE}$ controls DQ_{15}-DQ_8 while the $\overline{LCE}$ controls DQ_7-DQ_0. Skewed $\overline{CE}$ operation is illustrated in the timing diagram.

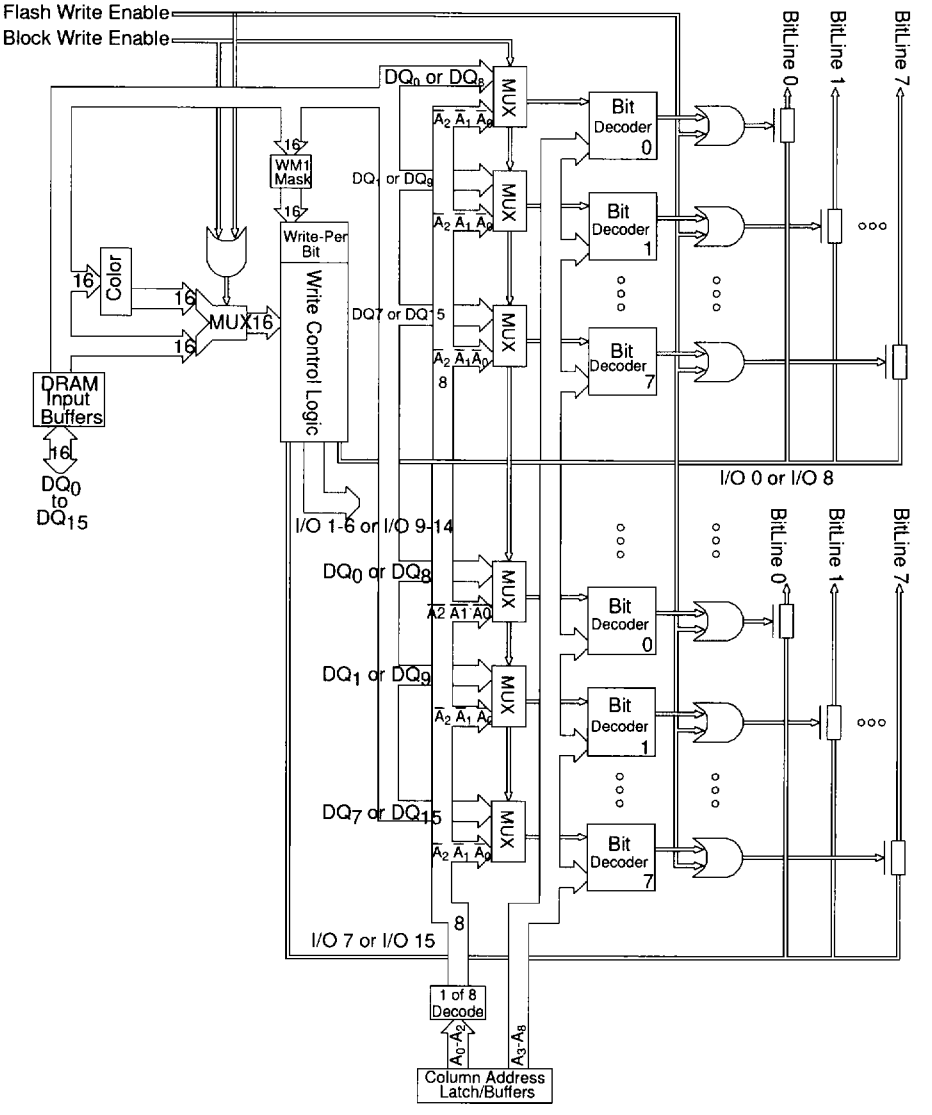
A dual $\overline{W}$ part has an upper and a lower $\overline{W}$. The $\overline{UW}$ and $\overline{LW}$ allows individual byte control of the DQs during write operations. The $\overline{UW}$ controls DQ_{15}-DQ_8 while the $\overline{LW}$ controls DQ_7-DQ_0. Skewed $\overline{W}$ operation is illustrated in the timing diagram. Individual byte control can be applied to the DRAM read, write, block write, load mask register and load color register cycles.

Power Up

After V_{CC} has reached its appropriate operating condition, (100 µs minimum), 8 CBR or $\overline{RE}$ only refresh must

be executed to reset mode(s) which may be set during powerup. The serial port will be initialized with the jump address of 128 bit at powerup

Block Write Operation



Serial Port Operation

The serial port is always in either read mode or write mode. To switch between modes, the chip must receive a transfer operation of the appropriate type as described in section title Transfer Operations. When $\overline{SE}$ is set low, each serial clock will cause a read or write of the SAM bit addressed by the internal serial port address counter. When $\overline{SE}$ is high, the serial port is disabled for both read and write, and the SDQ_i are set to tri-state.

Addresses are internally controlled by the serial port address counter. Each SC causes the internal address counter to increment independent of the state of $\overline{SE}$.

If the chip is in normal transfer mode, the internal counter will continue to increment until the next full (i.e. non-split) transfer cycle. At the rising edge of $\overline{TRG}$ in this transfer cycle, the serial port counter will be loaded with the start address as shown in read transfer timing.

If a split transfer operation has occurred, the chip is in split transfer mode. Instead of immediately loading the counter with the start address, the address is stored in the tap point register. The serial port address counter will continue to increment until it reaches the Serial Register Stop (SRS) address (also called jump address). If the serial port counter is less than 128, the stop address is equal to

1. 128 if the chip is in normal mode
2. 16, 32, 48, 64, 80, 96, 112, or 128 whichever occurs first if the chip is in SRS mode and the boundary address is set to 16
3. 32, 64, 96, or 128 whichever occurs first if the chip is in SRS mode and the boundary address is set to 32
4. 64 or 128 whichever occurs first if the chip is in SRS mode and the boundary address is set to 64

If the serial port counter is between 128 and 255, the stop address is equal to 128 plus the number(s) specified above. When the counter reaches the stop address, the counter is loaded with the tap point register that was saved during the split transfer cycle. Incrementing continues from the new address until the stop address is reached again. Note that the counter increments up to but not including the stop address.

Serial Port Read

If $\overline{SE}$ is low and the serial port is in read mode, each SC pulse causes 16 bits to be read from the SAM at the address pointed to by the internal serial address counter.

Continuous serial data out can be achieved either by performing a split read transfer before the internal address counter reaches the stop address or by performing a read transfer just as the serial port is running out of data. In the latter case, the transfer operation must time the rise of $\overline{TRG}$ to the proper SC pulse. See section on Transfer Operation (in preceding pages) for more information.

Serial Port Write

The serial port must be set to write mode by performing a write transfer operation (usually with all DQ's masked off to prevent writing) before attempting to write to the serial port.

If $\overline{SE}$ is low and the serial port is in write mode, each SC pulse causes the 16 bits on the SDQ_i pins to be written to the SAM at the address pointed to by the internal serial port address counter. Continuous serial port writes can be achieved in a manner identical to continuous serial port reads.

Transfer Operations

Transfer operations are listed in the truth table. Different transfer operations are selected by the state of the DSF and $\overline{W}$ pins at $\overline{RE}$ and $\overline{CE}$ times. For write transfers, the WPBM is loaded with the DQ_i at $\overline{RE}$ time unless the chip is in persistent write mask mode (see section on Load Persistent Write Mask Cycle).

The serial port is either in read mode or write mode. A read transfer operation will put the serial port into read mode if it is not already in read mode. A write transfer will switch the serial port into write mode if it is not already in write mode. To prevent storing of the current contents of the SAM when first switching to write mode, a transfer operation with the write per bit mask set to block all sixteen bits should be performed.

All transfer operations require:

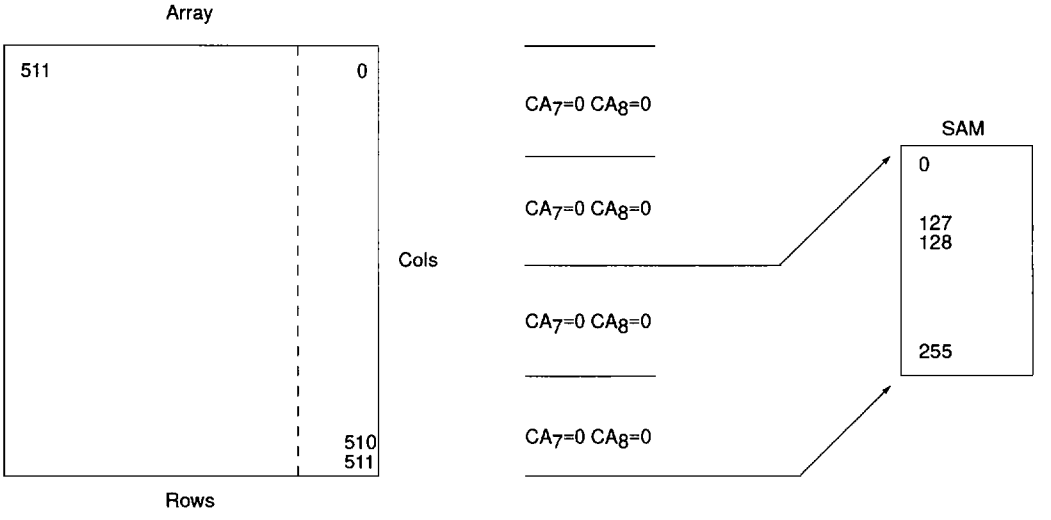
1. a row address, that is supplied when $\overline{RE}$ falls, and
2. CA_8 and a start pointer defined by CA_7-CA_0 that is supplied when $\overline{CE}$ falls. When performing a split transfer, the internal address counter determines which half of SAM is loaded.

Read Transfer Operations

Full Read Transfer

The full read transfer is used to start reading from the serial port and must be used as the first transfer before using the split read transfer described in the next section. This operation will load the entire serial register (256 x 16 bits) from the designated row address and CA_8. CA_8 controls which half of the wordline to load. CA_8 equals one will load the upper half of the wordline while CA_8 equals zero will load the lower half of the wordline. The start address register is loaded from the rest of the column address, CA_7 through CA_0. CA_7 equals zero is associated with the lower half of the SAM and CA_7 equals one is associated with the upper half of the SAM. In the below, a full read transfer of a wordline from DRAM to SAM is illustrated.

Full Read Transfer in Normal Mode

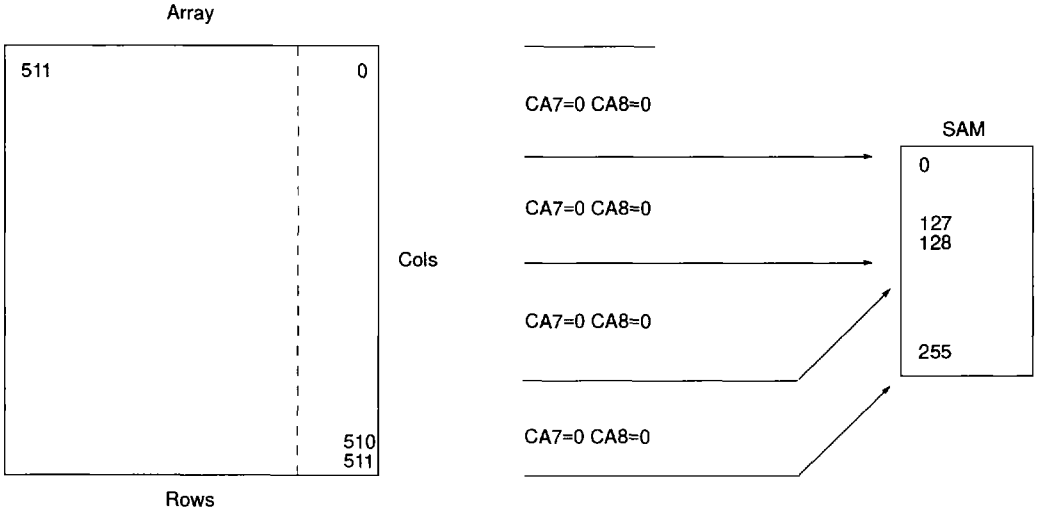


The example shows a transfer based on CA8=1. The serial port counter is set to the address specified by the user (CA_7-CA_0).

The next SC following the transfer will start reading data from this point in the serial register. Reading will continue until the end of the register and will wrap around. To keep serial data out continuous, either a split read transfer or a full read transfer must be performed as the serial register runs out of data. See the timing diagrams for the necessary timing requirements for either method of loading the register.

In a full read transfer with SRS mode, 256 bits are transferred from DRAM to SAM based on CA_7. In the SRS mode, CA_8 and CA_7 are internally swapped to allow full compatibility to full depth SAM. CA_8 equals zero is associated with lower half of the SAM while the CA8 equals one is associated with upper half of the SAM. In the following figure, a full read transfer in SRS mode between DRAM and SAM is illustrated.

Full Read Transfer in SRS Mode

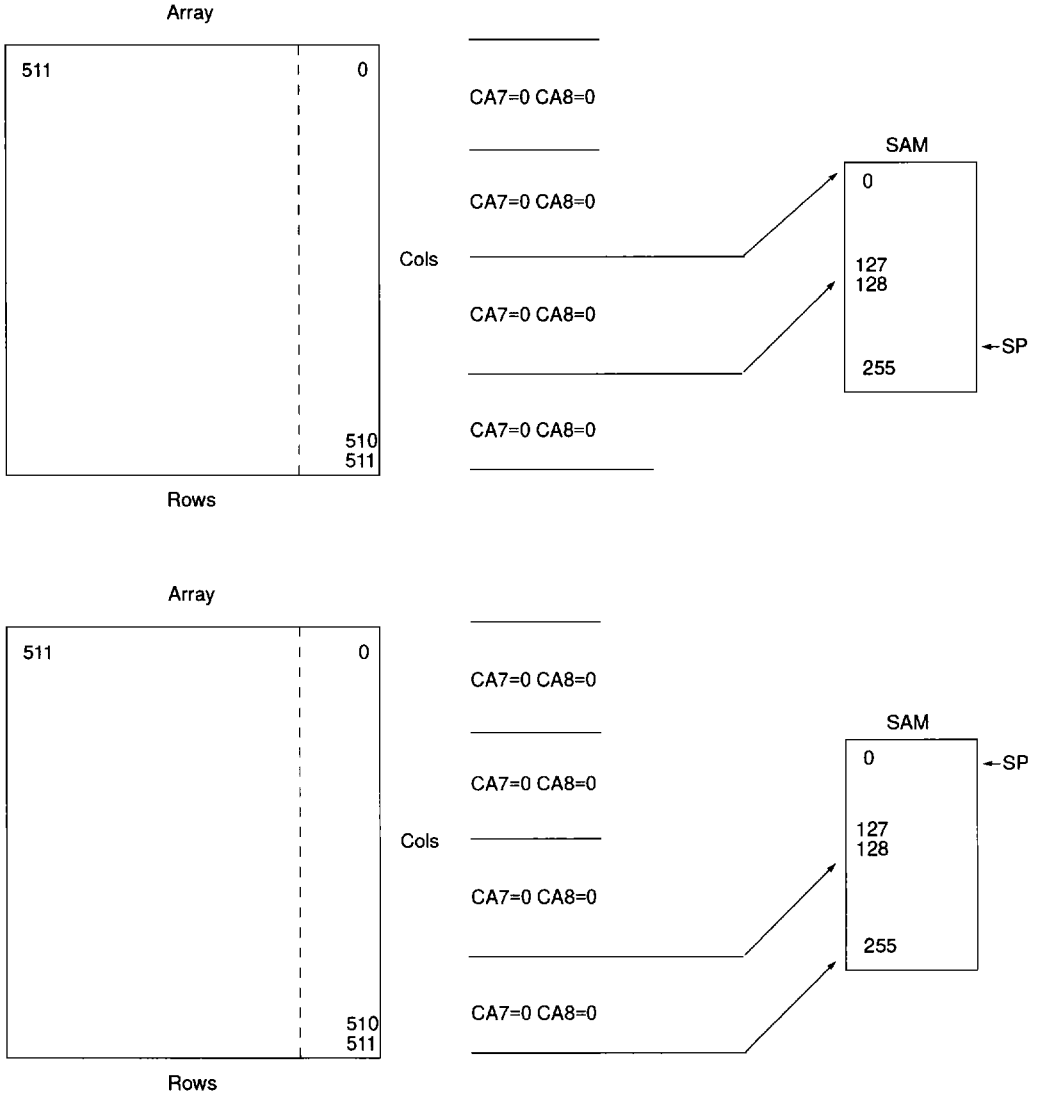


The example illustrates a full transfer in SRS mode based on CA_7=1.

Split Read Transfer

This transfer operation loads 128x16 bits of a wordline into half of the serial register. CA_8 and an internally generated address (CA_7) determine which quarter of the 512 bits of a wordline are loaded. Address pin A_7 at $\overline{CE}$ fall is a don't care and CA_7 is internally generated. This way, the SAM can be loaded with new data while data is being read out of the other half. The start address is given by CA_6 through CA_0 as in the normal read transfer but is held until the previous read transfer reaches its jump address at which time serial data reading will continue at the new start address. In the following figure, a split read transfer in normal mode of a word-line from DRAM to the SAM is illustrated.

Split Read Transfer in Normal Mode

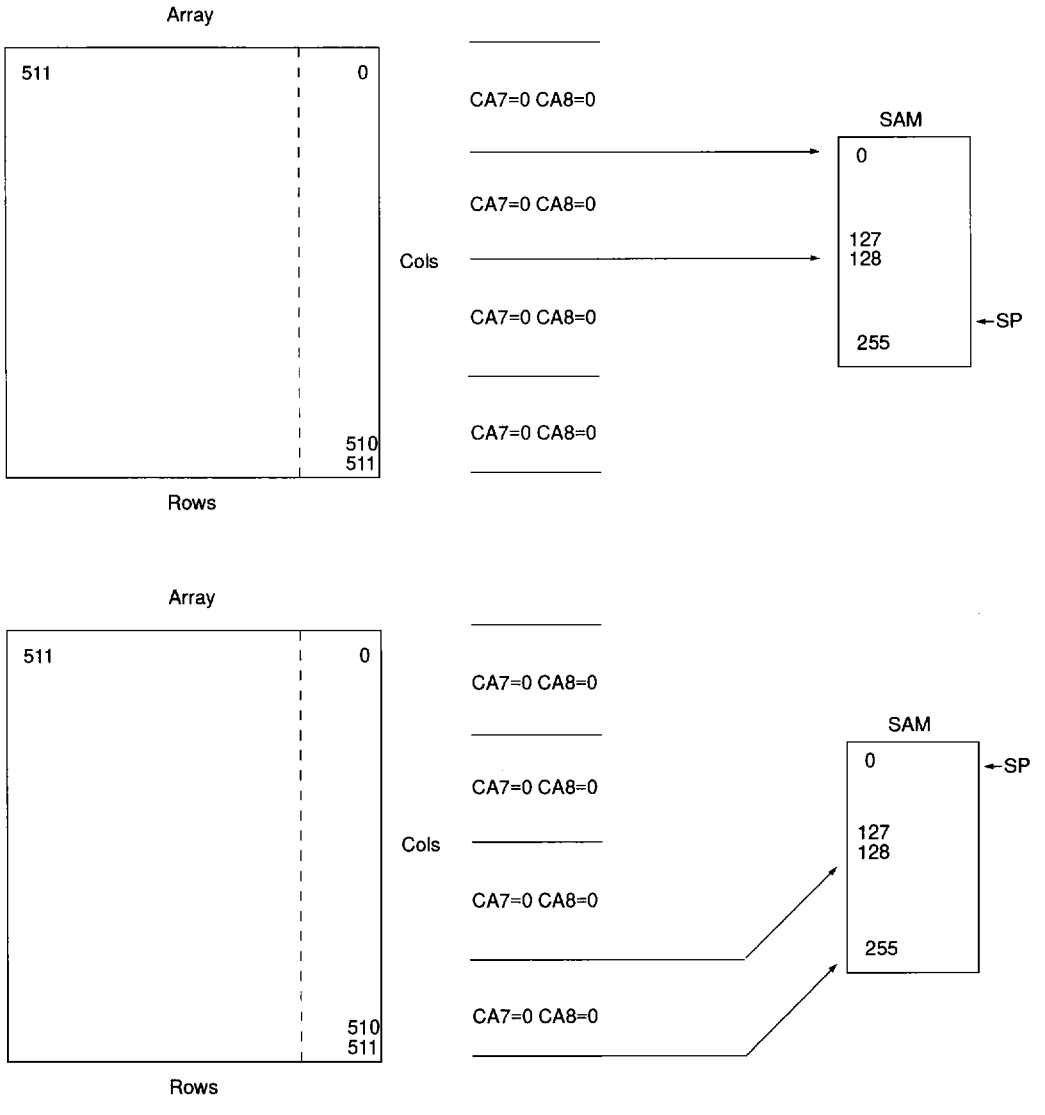


The example illustrates a split transfer between DRAM and SAM based on CA_8. In the first example, the serial port is active using data in the upper half of the SAM and the transfer is forced to lower half (CA_7=0). In the second example, the serial port is active using data in the lower half of the SAM and the transfer is forced to the upper half.

Note that there must be a full read transfer prior to any split read transfers. After the first load, any number of split read transfers can be performed. Each one will be started when the previous read transfer reaches the jump address. This allows the split read transfer to occur anytime prior to when the new data is needed.

In split read transfer with SRS mode, 128 or less bits are transferred from the selected row based on CA_7 and serial port internal address, CA_8. In the SRS mode, CA_8 and CA_7 are internally swapped for full compatibility to full depth SAM. After the swap, CA_8 equals zero is associated with the lower half of the SAM while CA_8 equals one is associated with the upper half of the SAM. In the following figure, a split read transfer in SRS mode is illustrated.

Split Read Transfer in SRS Mode



In the first example, the transfer is based on CA_7=1 and the serial port counter forced the transfer to occur in the lower half (CA_8=0). In the second example, the transfer is based on CA_7=1 and the serial port counter forced the upper half to be transferred (CA_8=1).

Full Depth SAM Compatibility

The 256 x 16 half depth SAM is fully compatible to a full depth SAM. The compatibility is provided by setting the VRAM in SRS mode of 128 or less and performing split transfer operations.

With the full and half depth SAM in SRS 128 mode, the split transfer to the unused portion of the SAM is based on CA_8. In reference to the figure on the next page, the following describes how compatibility between half and full depth SAM is achieved.

The serial port read begins with a full transfer, CA_7=CA_8=0. As a function of the serial clock (SC), the SAM is read until the jump/stop address is reached. Simultaneously, a split transfer is performed to the unused SAM based on CA_8. The new start address and new stop address are provided with this split transfer. Upon reaching the jump address, the SAM read continues from the new start address.

Write Transfer Operations

Masked Write Transfer Operation

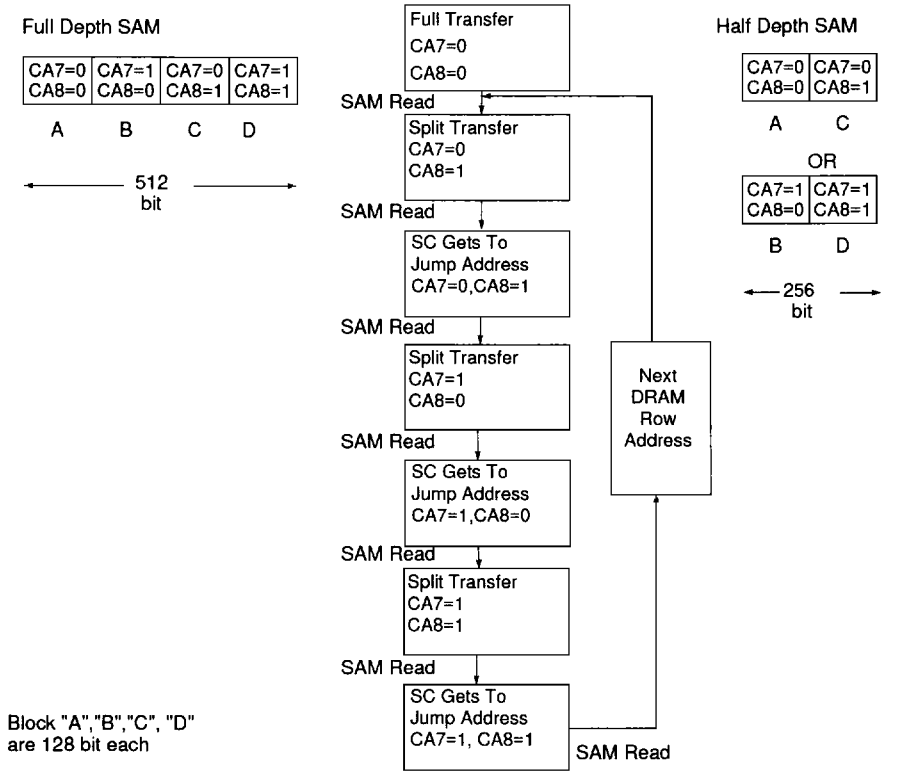
The write transfer operation will store the contents of the SAM at the address specified by RA8 through RA0 and CA_8. A total of 256x16 bits will be stored. The write transfer operation is masked by the write-per-bit mask in the I/O dimension. The start address is updated with CA_7-CA_0 and is used on the next SC following the transfer.

Masked Split Write Transfer Operation

A split write transfer stores 128x16 of the 256x16 bits in the SAM at the selected row address. CA_7 determines which half of the serial port register is stored. As in the write transfer operation, RA_8 through RA_0 determines which row is to be written and CA_8 determines which half of the row is written. Split write transfer is masked by the write-per-bit mask in the I/O dimension.

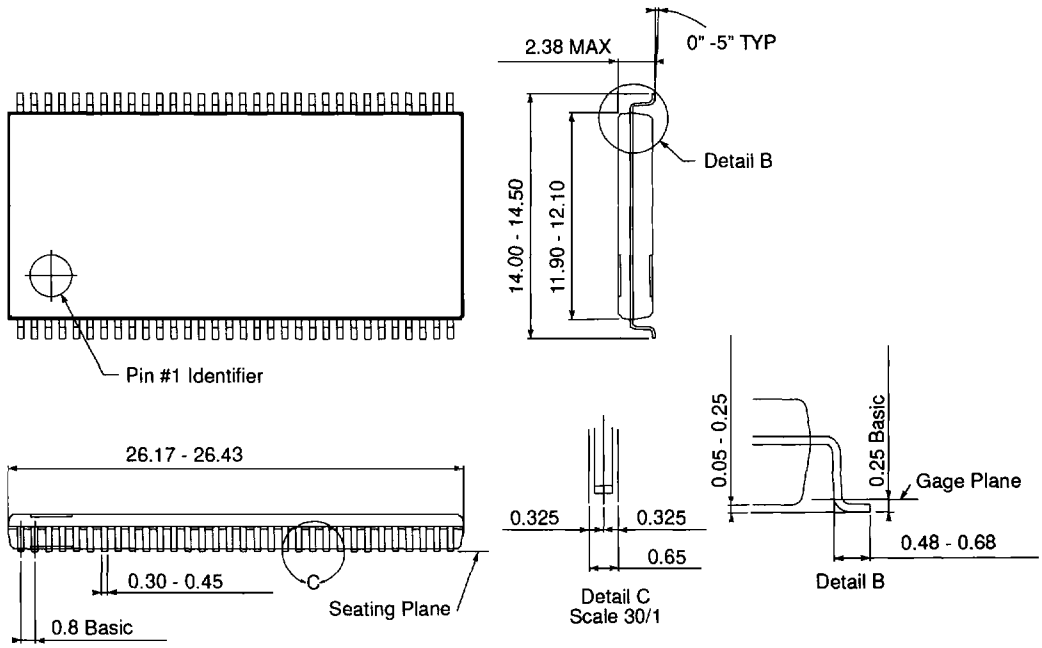
The split write transfer operation allows uninterrupted flow of data into the serial port by permitting half of the serial register to be stored into the RAM while the other half receives data-in from the serial data lines (SDQ_{15}-SDQ_0). The start address, given by CA_6 through CA_0 is held until the serial port reaches the jump address at which time serial data writing will continue at the new start address in the other split (CA_7) of the SAM.

Flow Chart of Half to Full Depth SAM Compatibility



Mechanical Drawing

Dwg. SSOG (dimensions in millimeters)



Dwg. TSOP (dimensions in millimeters)