OKI Semiconductor

MSC23T/D1721C-xxBS20

1,048,576-Word × 72-Bit DRAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The OKI MSC23T/D1721C-xxBS20 is a fully decoded 1,048,576-word × 72-bit CMOS Dynamic Random Access Memory Module composed of sixteen 4-Mb DRAMs (1M × 4) and four 2-Mb DRAMs (1M × 2) in TSOP or SOJ packages mounted with twenty decoupling capacitors on an 168-pin glass epoxy dual-inline package supports any application where high density and large capacity of storage memory are required.

FEATURES

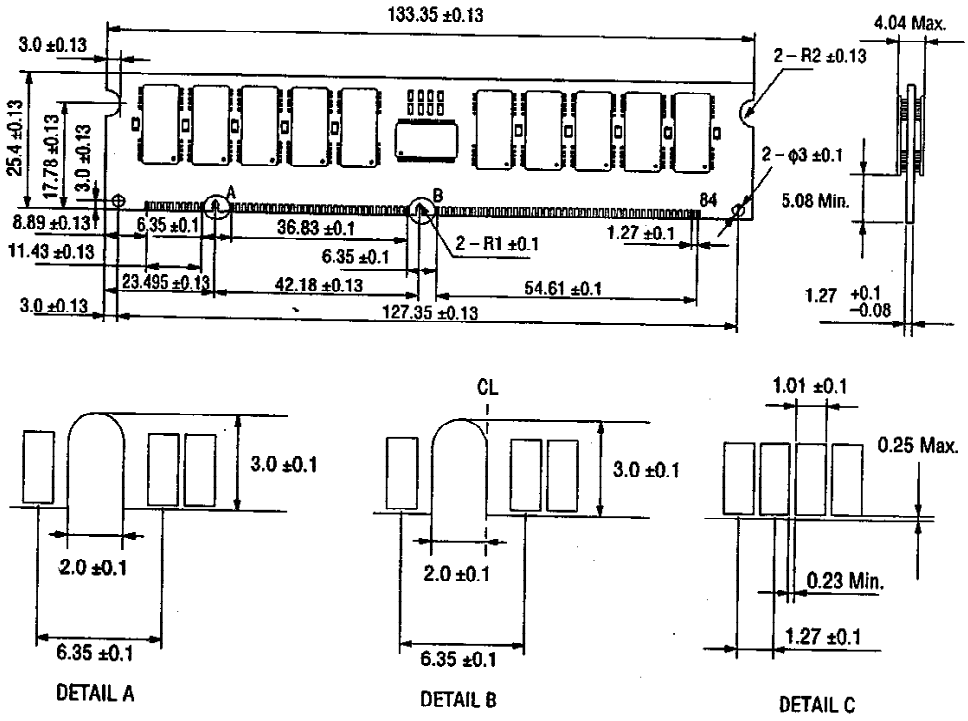
- 1-Meg × 72-bit (8 Byte Parity) organization
- 4-Mb DRAMs package
  MSC23T1721C-xxBS20 : TSOP
  MSC23D1721C-xxBS20 : SOJ
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Buffered inputs (except $\overline{RAS}$, DQ's)
- 4 Byte interleave enabled, dual address 0 input (A0/B0)
- Refresh : 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

PRODUCT FAMILY

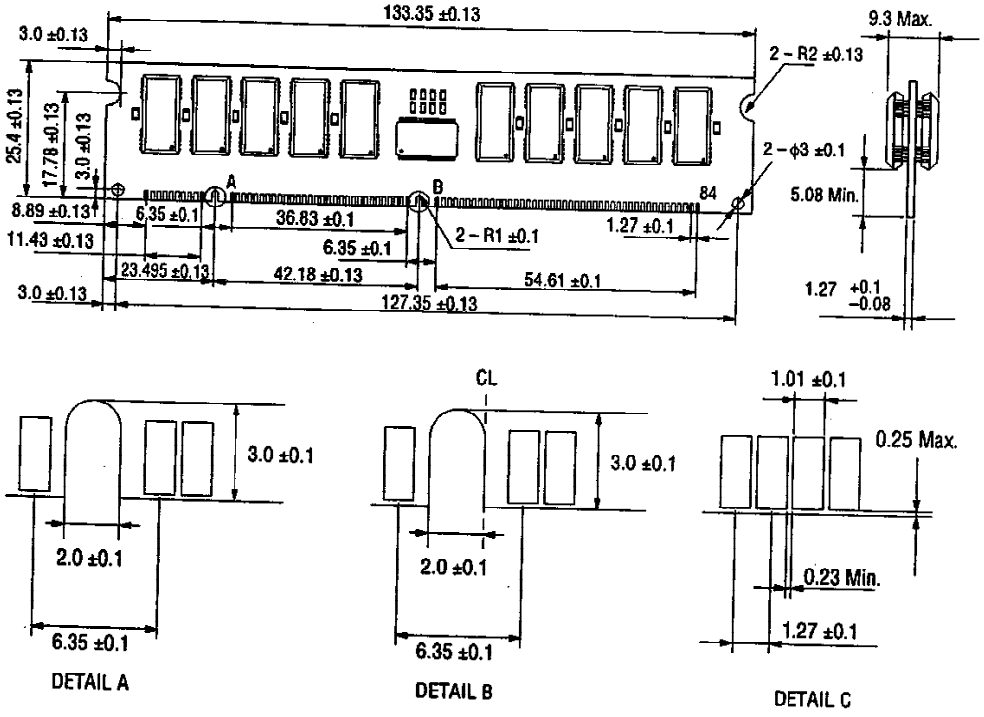
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSC23T/D1721C-60BS20	60 ns	36 ns	20 ns	20 ns	110 ns	11220 mW	143 mW (MOS level)
MSC23T/D1721C-70BS20	70 ns	41 ns	25 ns	25 ns	130 ns	10120 mW	
MSC23T/D1721C-80BS20	80 ns	46 ns	25 ns	25 ns	150 ns	9020 mW	

PIN CONFIGURATION

MSC23T1721C-xxBS20



MSC23D1721C-xxBS20



Front Side

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	18	V_{CC}	35	A4	52	DQ18	69	DQ28
2	DQ0	19	DQ14	36	A6	53	DQ19	70	DQ29
3	DQ1	20	DQ15	37	A8	54	V_{SS}	71	DQ30
4	DQ2	21	DQ16	38	NC	55	DQ20	72	DQ31
5	DQ3	22	DQ17	39	NC	56	DQ21	73	V_{CC}
6	V_{CC}	23	V_{SS}	40	V_{CC}	57	DQ22	74	DQ32
7	DQ4	24	NC	41	NC	58	DQ23	75	DQ33
8	DQ5	25	NC	42	NC	59	V_{CC}	76	DQ34
9	DQ6	26	V_{CC}	43	V_{SS}	60	DQ24	77	DQ35
10	DQ7	27	$\overline{WE0}$	44	$\overline{OE2}$	61	NC	78	V_{SS}
11	DQ8	28	$\overline{CAS0}$	45	$\overline{RAS2}$	62	NC	79	PD1
12	V_{SS}	29	$\overline{CAS2}$	46	$\overline{CAS4}$	63	NC	80	PD3
13	DQ9	30	$\overline{RAS0}$	47	$\overline{CAS6}$	64	NC	81	PD5
14	DQ10	31	$\overline{OE0}$	48	$\overline{WE2}$	65	DQ25	82	PD7
15	DQ11	32	V_{SS}	49	V_{CC}	66	DQ26	83	ID0
16	DQ12	33	A0	50	NC	67	DQ27	84	V_{CC}
17	DQ13	34	A2	51	NC	68	V_{SS}		

Back Side

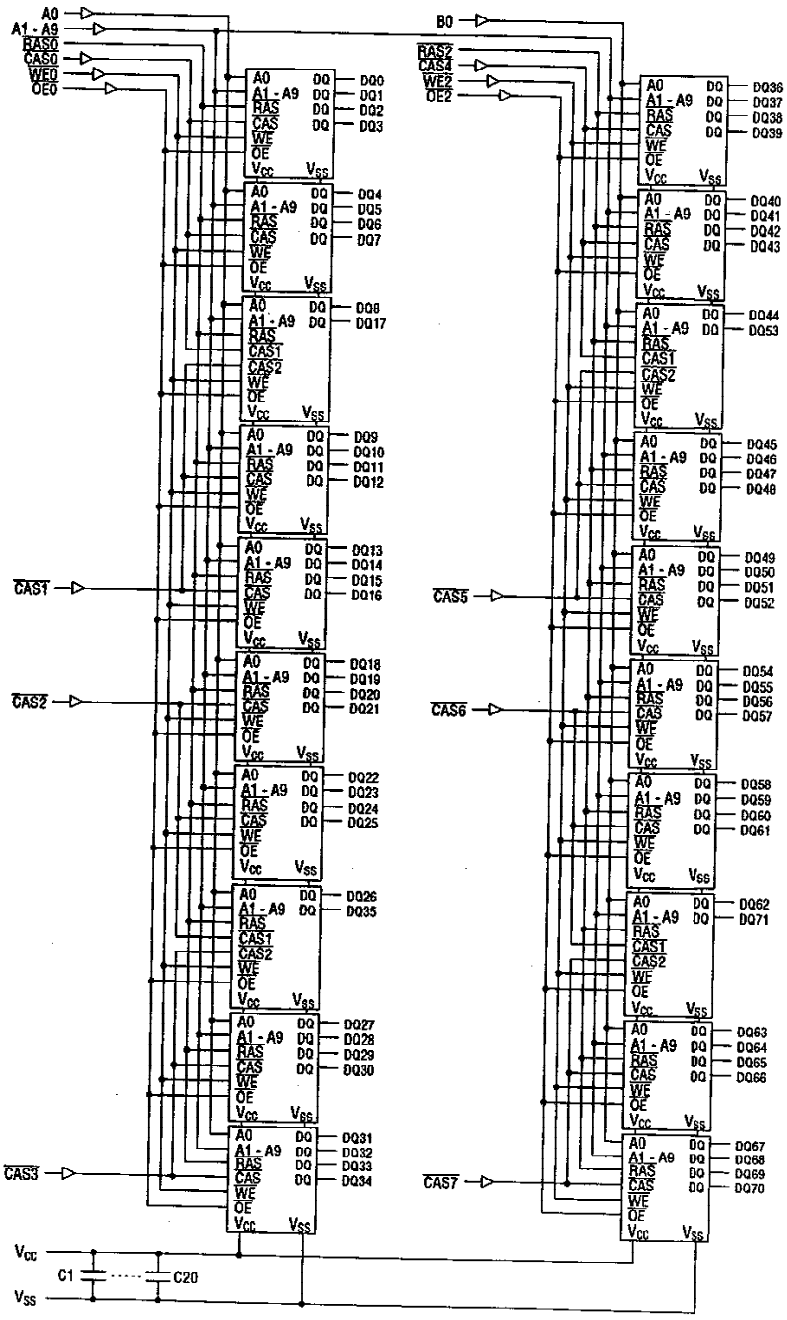
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
85	V_{SS}	102	V_{CC}	119	A5	136	DQ54	153	DQ64
86	DQ36	103	DQ50	120	A7	137	DQ55	154	DQ65
87	DQ37	104	DQ51	121	A9	138	V_{SS}	155	DQ66
88	DQ38	105	DQ52	122	NC	139	DQ56	156	DQ67
89	DQ39	106	DQ53	123	NC	140	DQ57	157	V_{CC}
90	V_{CC}	107	V_{SS}	124	V_{CC}	141	DQ58	158	DQ68
91	DQ40	108	NC	125	NC	142	DQ59	159	DQ69
92	DQ41	109	NC	126	B0	143	V_{CC}	160	DQ70
93	DQ42	110	V_{CC}	127	V_{SS}	144	DQ60	161	DQ71
94	DQ43	111	NC	128	NC	145	NC	162	V_{SS}
95	DQ44	112	$\overline{CAS1}$	129	NC	146	NC	163	PD2
96	V_{SS}	113	$\overline{CAS3}$	130	$\overline{CAS5}$	147	NC	164	PD4
97	DQ45	114	NC	131	$\overline{CAS7}$	148	NC	165	PD6
98	DQ46	115	NC	132	$\overline{PDE}$	149	DQ61	166	PD8
99	DQ47	116	V_{SS}	133	V_{CC}	150	DQ62	167	ID1
100	DQ48	117	A1	134	NC	151	DQ63	168	V_{CC}
101	DQ49	118	A3	135	NC	152	V_{SS}		

Presence Detect Pins

Pin No.	Pin Name	MSC23T/D1721C -60BS20	MSC23T/D1721C -70BS20	MSC23T/D1721C -80BS20
79	PD1	V_{OL}	V_{OL}	V_{OL}
163	PD2	V_{OL}	V_{OL}	V_{OL}
80	PD3	V_{OH}	V_{OH}	V_{OH}
164	PD4	V_{OL}	V_{OL}	V_{OL}
81	PD5	V_{OL}	V_{OL}	V_{OL}
165	PD6	V_{OH}	V_{OL}	V_{OH}
82	PD7	V_{OH}	V_{OH}	V_{OL}
166	PD8	V_{OH}	V_{OH}	V_{OH}
83	ID0	NC	NC	NC
167	ID1	V_{SS}	V_{SS}	V_{SS}

Note : PD1 - PD8 (Buffered Output)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to 7.0	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	20	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, B0)	C_{IN1}	—	10	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN2}	—	80	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS7}$, $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	C_{IN3}	—	10	pF
I/O Capacitance (DQ0 - DQ71)	C_{DQ}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSC23T/D1721C -60BS20		MSC23T/D1721C -70BS20		MSC23T/D1721C -80BS20		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	−100	100	−100	100	−100	100	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V	−10	10	−10	10	−10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	2040	—	1840	—	1640	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	46	—	46	—	46	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2 V	—	26	—	26	—	26	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	2040	—	1840	—	1640	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	2040	—	1840	—	1640	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	1680	—	1460	—	1280	mA	1, 3

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23T/D1721C -60BS20		MSC23T/D1721C -70BS20		MSC23T/D1721C -80BS20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	185	—	205	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	84	—	99	—	104	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	—	25	ns	4, 5
Access Time from Column Address	t_{AA}	—	36	—	41	—	46	ns	4, 6
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	25	—	25	ns	4
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	40	—	45	—	50	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t_{OFF}	2	20	2	25	2	25	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	2	20	2	25	2	25	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	58	—	68	—	78	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	18	40	18	45	18	55	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	13	24	13	29	13	34	ns	6
Row Address Set-up Time	t_{ASR}	6	—	6	—	6	—	ns	
Row Address Hold Time	t_{RAH}	8	—	8	—	8	—	ns	
Column Address Set-up Time	t_{ASC}	2	—	2	—	2	—	ns	
Column Address Hold Time	t_{CAH}	17	—	17	—	17	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	36	—	41	—	46	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23T/D1721C -60BS20		MSC23T/D1721C -70BS20		MSC23T/D1721C -80BS20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	2	—	2	—	2	—	ns	
Read Command Hold Time	t_{RCH}	2	—	2	—	2	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	2	—	2	—	2	—	ns	8
Write Command Set-up Time	t_{WCS}	2	—	2	—	2	—	ns	9
Write Command Hold Time	t_{WCH}	12	—	12	—	12	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	50	—	60	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	17	—	22	—	22	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	17	—	22	—	22	—	ns	
Data-in Set-up Time	t_{DS}	−2	—	−2	—	−2	—	ns	10
Data-in Hold Time	t_{DH}	20	—	20	—	20	—	ns	10
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	20	—	25	—	25	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40	—	50	—	50	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	56	—	66	—	71	—	ns	9
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	57	—	67	—	72	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	3	—	3	—	3	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	8	—	8	—	8	—	ns	
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	30	—	35	—	40	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	15	—	15	—	15	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	8	—	8	—	8	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	
$\overline{PDE}$ to PD Data Output Delay Time	t_{RPD}	—	10	—	10	—	10	ns	
$\overline{PDE}$ to PD Data Output Buffer Turn-off Delay Time	t_{FPD}	2	—	2	—	2	—	ns	

Notes:

1. A start-up delay of 200 μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
   When using the internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.
2. AC mesurement assume $t_T = 5$ ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves an open circuit condition and are not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data output pin will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and the data output pin will contain data read from the selected cell. If neither conditions is satisfied, the data output logic state (at access time) is undefined.
10. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle, and to $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle or a read modify write cycle.
11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
    The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
12. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM G for AC Timing Waveforms