YAMAHA LSI

YTZ420

FCC

Fieldbus Communication Contoroller LSI

YAMAHA CORPORATION

YTZ420 CATALOG
CATALOG No. : LSI-4TZ420A6
2008.10

General Description

YTZ420 is a communication controller intended for use in a node of fieldbus operating per International standard, IEC 1158. **YTZ420** is based on a latest sub micron CMOS technology. Its provides 100% compatible Physical Layer functionality to IEC 1158-2, and ISA S50.2. Lower part of Data Link Layer is also implemented to conform IEC Committee Draft SC65C(Secretariat) 106. See Figure 1 for block diagram. A low power consumption feature of **YTZ420** is an ideal solution for Intrinsic-Safety (I.S.) devices. **YTZ420** shall be used in cooperation with a microcontroller / microprocessor that serves for higher part of communication protocol.

Features

General

- Small Package: 44 pin plastic LQFP or QFP
- Low Power consumption: less than 3mW
- Wide supply voltage range: 3~5V
- Flexible 8 bit parallel interface directly connectable to both Intel and Motorola type microcontrollers
- Two-mode DMA interface to reduce interrupts
- Programmable prescaler to allow 0.5, 1, 2, 4, 8, and 16MHz clock input

Physical Layer

- 100% compatible to IEC 1158-2
- Data rate: 31.25kbps and 1Mbps
- Manchester encoder/decoder
- Two useful signal driving methods including standard MDA-MAU interface
- Automatic correction of signal polarity
- Addition and deletion of preamble, start- and stop-delimiters
- Internal Jabber timer (4096 bit time)
- Internal and external loop back capability for self diagnostics

Data Link Layer

- Automatic calculation of 16 bit FCS
- Internal data buffers to reduce microcontroller overhead (32 stage transmit-FIFO and 32 stage receive FIFO)
- DL-timer (NODE time and Token hold time)
- Timers for time-dependent operation

Applications

- Distributed Control System
- Single Loop Controller
- Temperature Controller
- Field transmitter
- Field actuator

Block Diagram

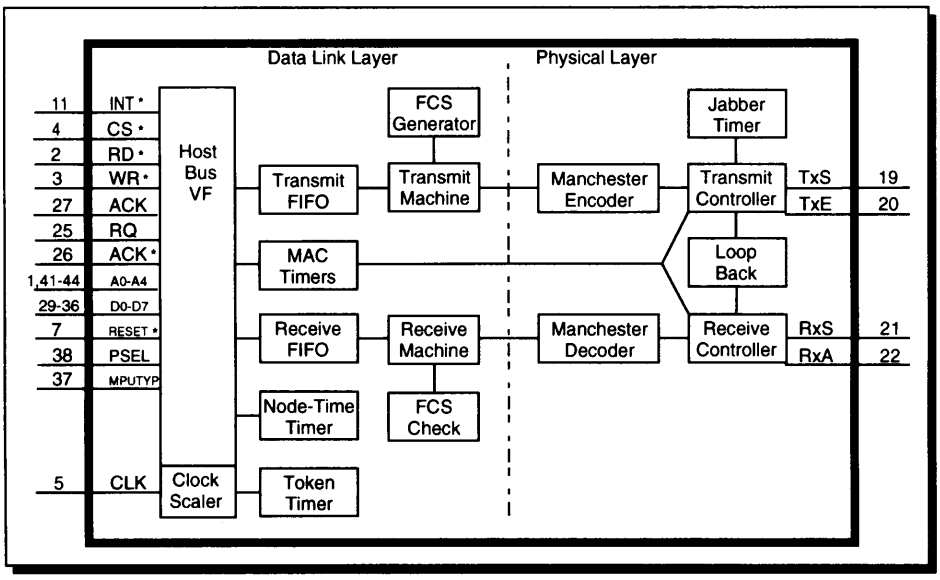


Figure 1 Block Diagram of YTZ420

Absolute Maximum Ratings

Description	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	Vss-0.5	Vss+7.0	V	
Input Voltage	V_I	Vss-0.5	V_{DD}+0.5	V	
Output Voltage	V_O	Vss-0.5	V_{DD}+0.5	V	
Operating Temperature	Topr	-40	85	℃	
Storage Temperature	Tstg	-40	+125	℃	
Input HIGH Current	I_{OH}	-	+20	mA	$V_O = V_{DD}$
Input LOW Current	I_{OL}	-20	-	mA	V_O = 0V
Power Dissipation	P_D	0	100	mW	

Recommended Operating Condition

Description	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	5.5	V	
Ambient Temperature	T_A	0	70	℃	
Clock Frequency	F_{CLK}	0.5	4	MHz	V_{DD} = 3V
		0.5	16		V_{DD} = 5V

Package

YTZ420 is packaged in a plastic surface-mount flat package(LQFP) of 44 pins to occupy minimum space in your electronicsciruit bodrd. Figure 2 shows the package dimension.

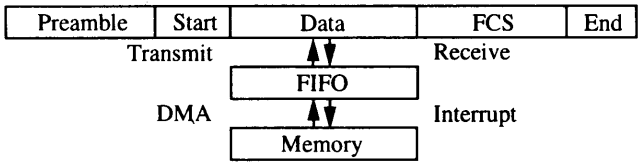
- Lead-free plating LQFP44 (YTZ420-VZ) ; in production
- Lead-free plating QFP44 (YTZ420-FZ) ; discontinued

How it works

YTZ420 transmits data blocks of assigned length stored in the transmit FIFO buffer by adding preamble, start-delimiter, frame check sequence (FCS) and end delimiter. It also observes input signal to find preamble for bit synchronization and start-delimiter for octet synchronization. It stores received data into the receive FIFO buffer by deleting preamble, delimiters and FCS. A DMA interface capability does them without making interrupt to the microcontroller.

YTZ420 evaluates validity of received frames by delimiters and FCS to generate an interrupt when an error is detected.

YTZ420 also provides various timers for time-critical part of Data Link Layer. They are NODE Time timer, Remaining timer for token holding time, timer to guarantee minimum time period between data frame and timer to detect inactivity of the fieldbus.



Chip Specification

Pin Configuration

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	A4	12	MO0	23	TST0	34	D5
2	RD*/E	13	MO1	24	TST1	35	D6
3	WR*/RW	14	MO2	25	RQ	36	D7
4	CS*	15	MO3	26	ACK*	37	MPUTYP
5	CLK	16	MO4	27	RDY	38	PSEL
6	VSS	17	V_{DD}	28	V_{SS}	39	V_{DD}
7	RESET*	18	V_{SS}	29	D0	40	V_{SS}
8	MS0	19	TxS	30	D1	41	A0
9	MS1	20	TxE*/ADD	31	D2	42	A1
10	MS2	21	RxS	32	D3	43	A2
11	INT*	22	RxA	33	D4	44	A3

Asterisk (*) indicates negative (LOW active) signal

Signal Description

Signal	Pins	I/O	Description
VDD	17, 39	-	Power supply. 3~5V DC (5%) is expected.
VSS	6, 18, 28, 40	-	Ground level
RESET*	7	I	Reset input. LOW input at this pin and at least four (4) cycle of CLK input are required to reset YTZ420.
CLK	5	I	Clock input. Frequency is expected as one from 1, 2, 4 and 8MHz.
CS*	4	I	Chip Select. A LOW input to this pin enables bus access to YTZ420.
A0-A4	1, 42-44	I	Address input from host processor.
D0-D7	29-36	I/O	Data bus for host processor. These pins are initialized to high impedance by reset.
MPUTYP	37	I	Selects bus operation type: Low: Intel type 8 bit bus HIGH: Motorola type 8 bit bus
PSEL	38	I	Selects bus access protocol: LOW: asynchronous bus cycle to use RDY signal HIGH: RDY signal is not used.
RD*/E	2	I	Read strobe (RD*) in Intel mode (MPUTYP = LOW) Enable (E) in Motorola mode (MPUTYP = HIGH)
WR*/RW	3	I	Write strobe (WR*) in Intel mode (MPUTYP = LOW) Read/Write select (R/W*) in Motorola mode (MPUTYP = HIGH)
RDY	27	O	Access ready signal to host processor. This signal is available only when PSEL = LOW. This signal is always HIGH when PSEL = HIGH. This signal is initialized to HIGH by reset.
INT*	11	O	Interrupt to host processor. This signal is initialized to HIGH by reset.
RQ	25	O	Data transfer request to DMA controller.
ACK*	26	I	Data transfer acknowledge from DMA controller.
TxS	19	O	Transmit signal to medium attachment unit. This signal is a Manchester-encoded and initialized to LOW by reset. This signal stays LOW when YTZ420 is not transmitting or in internal loop back mode.
TxE*/ADD	20	O	Transmit control to medium attachment unit.
RxS	21	I	Receive Signal from medium attachment unit
RxA	22	I	Receive activity (carrier detect) from medium attachment unit
TST0-TST1	23-24	I	Input for chip test. These pins should be connected to Vss in normal operation.
MS0-MS2	8-10	I	Input for chip test. These pins should be connected to Vss in normal operation.
MO0-MO4	12-16	O	Output for chip test. These pin should be kept open in normal operation.

Note: Since INT*, RDY and RQ outputs are not "open-drain" type, you are not able to make wired-or with other signals.

DC Characteristics

Description	Symbol	Min	Max	Unit	Condition
High Input Voltage	V_{IH}	2.2	-	V	V_{DD} = 3.0V ± 10%
		3.5	-		V_{DD} = 5.0V ± 10%
LOW Input Voltage	V_{IL}	-	0.5	V	V_{DD} = 3.0V ± 10%
		-	1.0		V_{DD} = 5.0V ± 10%
High Output Voltage	V_{OH}	V_{DD}-0.6	-	V	V_{DD} = 3.0V, I_{OH} = -1mA
		V_{DD}-1.0	-		V_{DD} = 5.0V, I_{OH} = -2mA
Low Output Voltage	V_{OL}		V_{SS}+0.4	V	V_{DD} = 3.0V, I_{OL} = 1mA
			V_{SS}+0.4		V_{DD} = 5.0V, I_{OL} = 2mA
Supply Current	I_{CC}	-	0.2	mA	Static Operation *
Input Capacitance	C_{IN}	-	8	pF	T_A=25C, F_{CLK}=1MHz
Output Capacitance	C_{OUT}	-	10	pF	V_{DD} = VI = 0V
I/O pin capacitance	C_{IO}	-	12	pF	

* Static Operation:
F_{CLK} = 1MHz; V_{DD} = 5.0V; D0-D7 = V_{DD}, RxS = RxA = TST0-TST1 = MS0-MS2 = V_{SS};
RESET* = V_{DD}; Other inputs = V_{DD}; all outputs are open.

AC Characteristics

3V ± 10% operation

Description	Symbol	Min	Max	Unit	Condition
Clock frequency	FCLK	0.50±0.1%		MHz	PRD ϕ = 1B
		1.0±0.1%			CLOCK ϕ = 00B
		2.0±0.1%			CLOCK ϕ = 01B
		4.0±0.1%			CLOCK ϕ = 10B
CLK pulse width (LOW)	tPWL	100	-	ns	
CLK pulse width (HIGH)	tPWH	100	-	ns	
RESET* pulse width	tRST	4	-	tCYC	stays in LOW
Bit time of RxS	tBT	32±0.9		µs	
Rise time of RxS, RxA	tIR	-	100	ns	
Fall time of RxS, RxA	tIF	-	100	ns	
Positive jitter of RxS	tPJ	-	0.15	tBT	
Negative jitter of RxS	tPN	-	0.15	tBT	
RxA setup time	tCDS	0	-	ns	
RxA hold time	tCDH	0	-	ns	
RD* pulse width	tPWRD	200	-	ns	
WR* pulse width	tPWWR	200	-	ns	
E pulse width	tPWEH	200	-	ns	
Address setup time	tAS	9	-	ns	
Address hold time	tAH	0	-	ns	
Data setup time	tDS	2	-	ns	
Data hold time	tDH	9	-	ns	
CS* setup time	tCS	0	-	ns	
CS* hold time	tCH	0	-	ns	
R/W* setup time	tRWS	1	-	ns	
R/W* hold time	tRWH	1	-	ns	
Data output delay time	tDDR	-	86	ns	
Read data hold time	tDHR	14	65ϕ2	ns	
RDY output delay time	tRDW	-	60	ns	
RDY pulse width	tPWRL	0	4	tCYC	
RDY hold time	tRDWH	0	-	ns	
Read data valid to RDY	tDVR	-	1	tCYC	Period(RDY=LOW)
TxS to TxE/ADD (jitter)	tJCR	-3.5	3.5	ns	
TxS to TxE/ADD (jitter)	tJSM	-0.7	0.7	ns	
ACK* setup time	tAKS	3	-	ns	
ACK* hold time	tAKH	0	-	ns	
RQ clear time	tRQC	-	60	ns	

VDD = 3.0V ± 10%, TA = -40~85℃, Output Load = 50pF.

Note ϕ : PRD bit in Clock Mode register and CLOCK bits in Mode register

ϕ2: Data bus is in Hi-z status at tDHR Max

5V ± 10% operation

Description	Symbol	Min	Max	Unit	Condition
Clock frequency	FCLK	0.50±0.1%		MHz	PRD ✞= 1B
		1.0±0.1%			CLOCK ✞= 00B
		2.0±0.1%			CLOCK ✞= 01B
		4.0±0.1%			CLOCK ✞= 10B
		8.0±0.1%			CLOCK ✞= 11B
		16.0±0.1%			PRD ✞= 1B
CLK pulse width (LOW)	tPWL	25	-	ns	
CLK pulse width (HIGH)	tPWH	25	-	ns	
RESET* pulse width	tRST	4	-	tCYC	stays in LOW
Bit time of RxS	tBT	32±0.9		µs	31.25kbps
		1.0±0.025		µs	1Mbps
Rise time of RxS, RxA	tIR	-	100	ns	
Fall time of RxS, RxA	tIF	-	100	ns	
Positive jitter of RxS	tPJ	-	0.15	tBT	
Negative jitter of RxS	tPN	-	0.15	tBT	
RxA setup time	tCDS	0	-	ns	
RxA hold time	tCDH	0	-	ns	
RD* pulse width	tPWRD	50	-	ns	
WR* pulse width	tPWWR	50	-	ns	
E pulse width	tPWEH	50	-	ns	
Address setup time	tAS	5	-	ns	
Address hold time	tAH	0	-	ns	
Data setup time	tDS	2	-	ns	
Data hold time	tDH	5	-	ns	
CS* setup time	tCS	0	-	ns	
CS* hold time	tCH	0	-	ns	
R/W* setup time	tRWS	1	-	ns	
R/W* hold time	tRWH	1	-	ns	
Data output delay time	tDDR	-	39	ns	
Read data hold time	tDHR	5	36 ✞2	ns	
RDY output delay time	tRDW	-	30	ns	
RDY pulse width	tPWRL	0	4	tCYC	Period(RDY=LOW)
RDY hold time	tRDWH	0	-	ns	
Read data valid to RDY	tDVR	-	1	tCYC	
TxS to TxE/ADD (jitter)	tJCR	-1.5	1.5	ns	
TxS to TxE/ADD (jitter)	tJSM	-0.6	0.6	ns	
ACK* setup time	tAKS	3	-	ns	
ACK* hold time	tAKH	0	-	ns	
RQ clear time	tRQC	-	30	ns	

VDD = 5.0V ± 10%, TA = -40~85℃, Output Load = 50pF.

Note ✞ : PRD bit in Clock Mode register and CLOCK bits in Mode register

✞2: Data bus is in Hi-z status at tDHR Max

5V ± 5% operation

Description	Symbol	Min	Max	Unit	Condition
Clock frequency	FCLK	0.50±0.1%		MHz	PRD ϕ = 1B
		1.0±0.1%			CLOCK ϕ = 00B
		2.0±0.1%			CLOCK ϕ = 01B
		4.0±0.1%			CLOCK ϕ = 10B
		8.0±0.1%			CLOCK ϕ = 11B
		16.0±0.1%			PRD ϕ = 1B
CLK pulse width (LOW)	tPWL	25	-	ns	
CLK pulse width (HIGH)	tPWH	25	-	ns	
RESET* pulse width	tRST	4	-	tCYC	stays in LOW
Bit time of RxS	tBT	32±0.9		µs	31.25kbps
		1.0±0.025		µs	1Mbps
Rise time of RxS, RxA	tIR	-	100	ns	
Fall time of RxS, RxA	tIF	-	100	ns	
Positive jitter of RxS	tPJ	-	0.15	tBT	
Negative jitter of RxS	tPN	-	0.15	tBT	
RxA setup time	tCDS	0	-	ns	
RxA hold time	tCDH	0	-	ns	
RD* pulse width	tPWRD	50	-	ns	
WR* pulse width	tPWWR	50	-	ns	
E pulse width	tPWEH	50	-	ns	
Address setup time	tAS	5	-	ns	
Address hold time	tAH	0	-	ns	
Data setup time	tDS	2	-	ns	
Data hold time	tDH	4	-	ns	
CS* setup time	tCS	0	-	ns	
CS* hold time	tCH	0	-	ns	
R/W* setup time	tRWS	1	-	ns	
R/W* hold time	tRWH	1	-	ns	
Data output delay time	tDDR	-	30	ns	
Read data hold time	tDHR	20	32 ϕ2	ns	
RDY output delay time	tRDW	-	26	ns	
RDY pulse width	tPWRL	0	4	tCYC	Period(RDY=LOW)
RDY hold time	tRDWH	0	-	ns	
Read data valid to RDY	tDVR	-	1	tCYC	
TxS to TxE/ADD (jitter)	tJCR	-1.5	1.5	ns	
TxS to TxE/ADD (jitter)	tJSM	-0.6	0.6	ns	
ACK* setup time	tAKS	3	-	ns	
ACK* hold time	tAKH	0	-	ns	
RQ clear time	tRQC	-	26	ns	

VDD = 5.0V ± 5%, TA = 0~70℃, Output Load = 50pF.

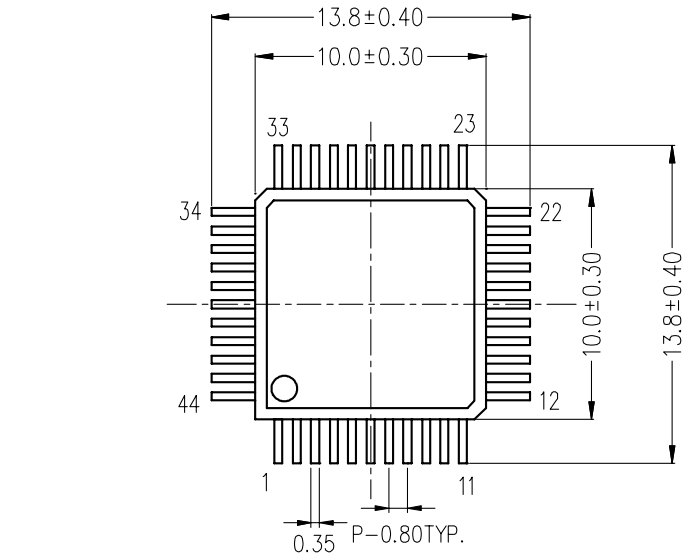
Note ϕ : PRD bit in Clock Mode register and CLOCK bits in Mode register

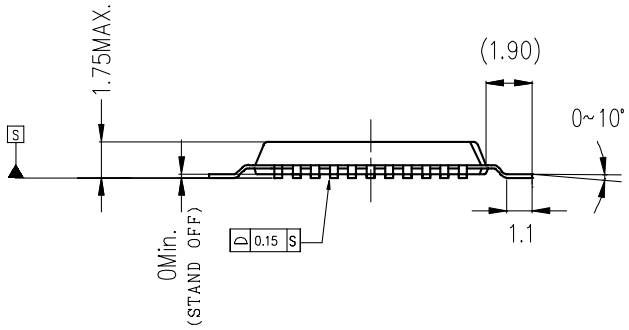
ϕ2: Data bus is in Hi-z status at tDHR Max

Package Dimension

1. YTZ420-VZ

C-PK44VP1-1





端子厚さ / Lead Thickness : 0.17

モールドコーナー形状は、本図面と若干異なるタイプもあります。
We have a different corner type of plastic body from this drawing.

カッコ内の寸法値は参考値とする。
The value parenthesized is not specified.

モールド外形寸法はバリを含まない。
Plastic body dimensions do not include burr of resin.

UNIT: mm

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Note: The storage and soldering of LSIs for surface mounting need special consideration.
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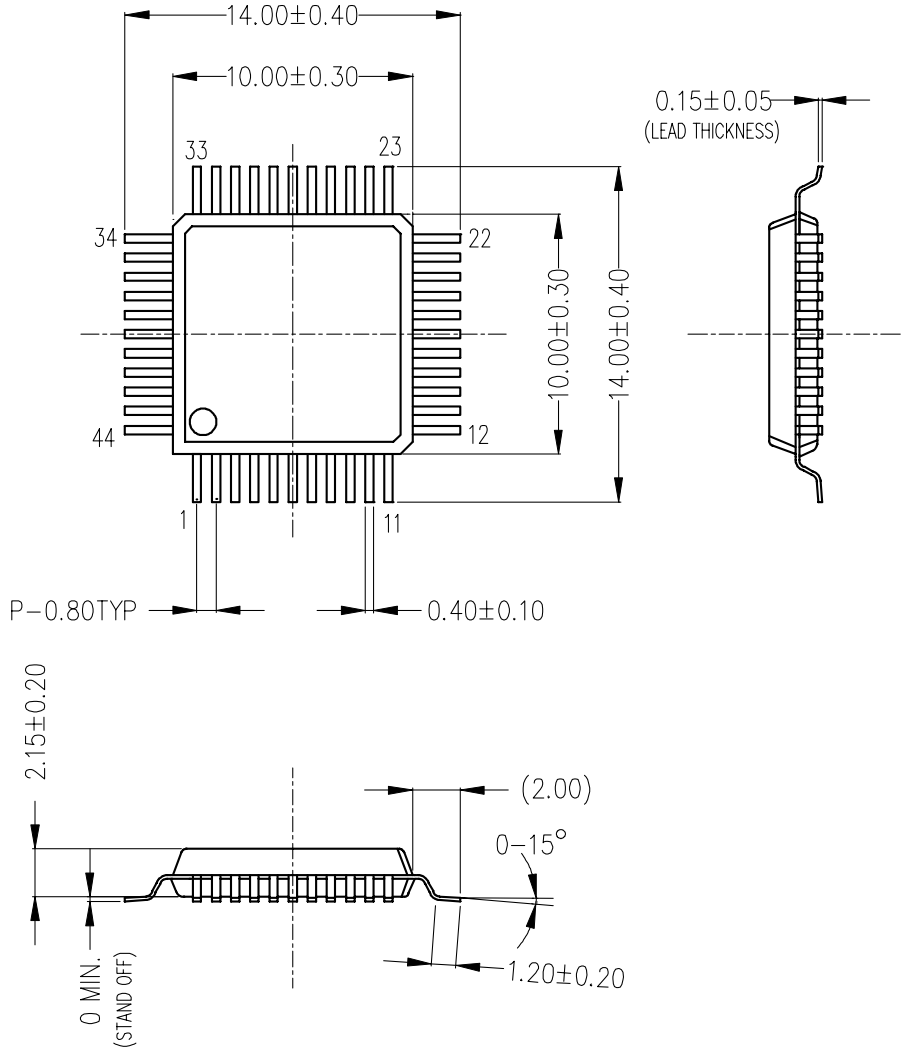
2. YTZ420-FZ

C-PK44FP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
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