TMC2210
CMOS Multiplier-Accumulator
16 x 16 Bit, 65, 80, 95 ns

Description

The TMC2210 is a high-speed 16 x 16 bit digital multiplier-accumulator which is available in speed bins of 65, 80 or 95 ns. Input data may be specified as two's complement or unsigned magnitude, yielding a 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit Extended Product (XTP), a 16-bit Most Significant Product (MSP) and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and MSP. The LSP is multiplexed with the Y operand inputs. The output register can be preloaded directly via the output ports.

The TMC2210 is a drop in replacement for the TMC2010 and the TMC2110, and is pin and function compatible with the industry standard Raytheon Semiconductor La Jolla TDC1010, the LMA1010/2010, IDT7210 and CY7510.

Features

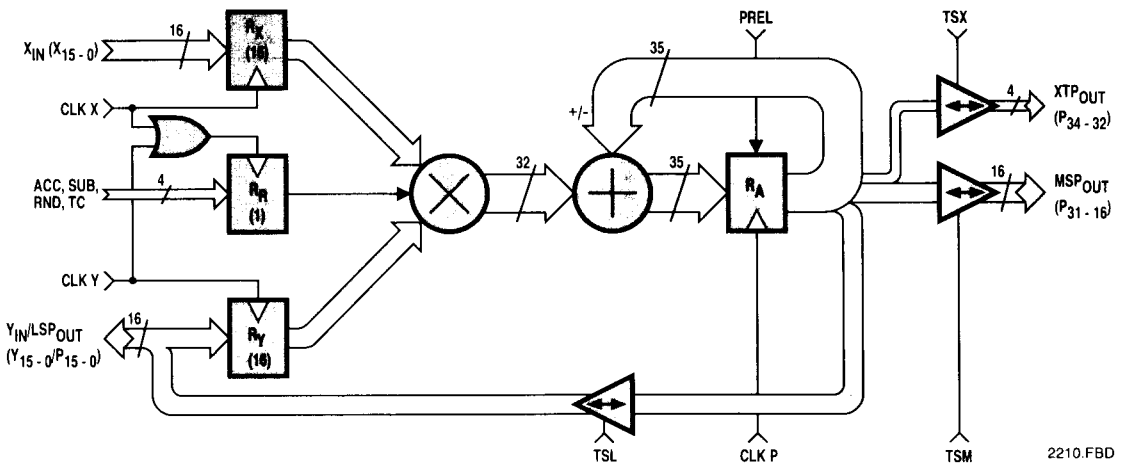
- 65, 80 or 95 ns multiply-accumulate time
- 16 x 16 parallel multiplication with accumulation to 35-bit result
- Selectable accumulation, subtraction, rounding, and accumulator preload
- Two's complement or unsigned magnitude operation
- All inputs and outputs are registered and TTL compatible
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 64-pin ceramic or plastic DIP, 68-pin grid array and 68-lead plastic J-leaded chip carrier

Applications

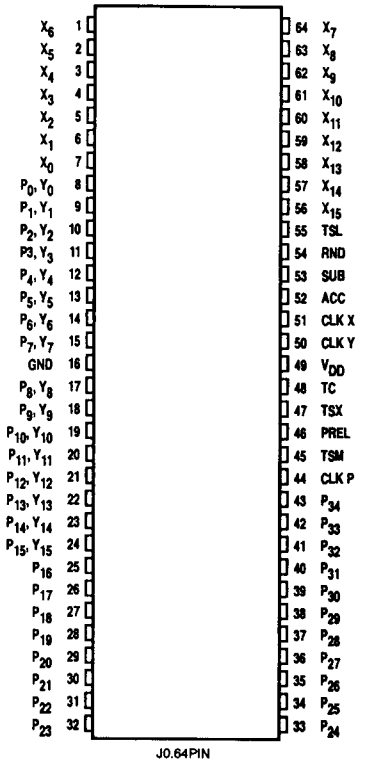
- Array processors
- Video processors
- Radar signal processors
- FFT processors
- General purpose digital signal processors
- Microcomputer/minicomputer accelerators

Fixed-Point

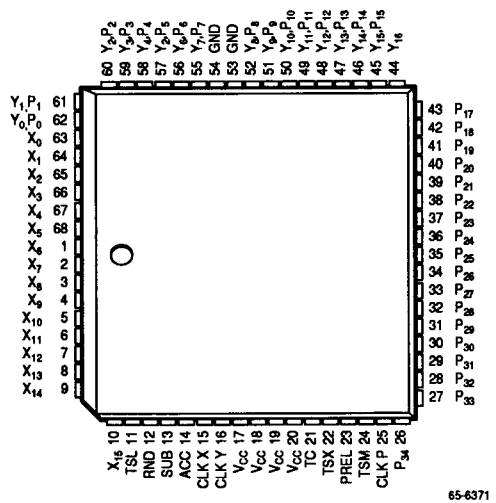
Functional Block Diagram



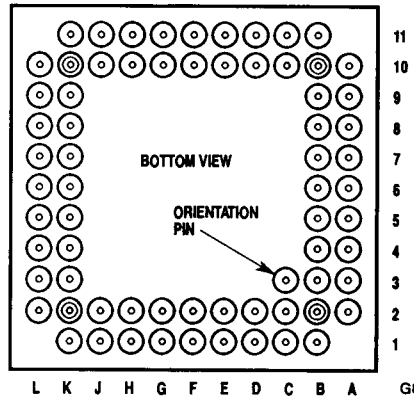
Pin Assignments



64 Pin Hermetic Ceramic DIP – J0, N0 Package



68-Lead Plastic J-Leaded chip Carrier — R1 Package



G8.69PIN/H8.69PIN

68 Pin Ceramic (G8) or Plastic (H8) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	X_{12}	F10	V_{DD}	K4	P_{20}
A3	P_0, Y_0	B10	X_{14}	F11	CLK Y	K5	P_{22}
A4	X_1	B11	NC	G1	P_{11}, Y_{11}	K6	P_{24}
A5	X_3	C1	P_4, Y_4	G2	P_{10}, Y_{10}	K7	P_{26}
A6	X_5	C2	P_3, Y_3	G10	TSX	K8	P_{28}
A7	X_7	C10	TSL	G11	TC	K9	P_{30}
A8	X_9	C11	X_{15}	H1	P_{13}, Y_{13}	K10	P_{32}
A9	X_{11}	D1	P_6, Y_6	H2	P_{12}, Y_{12}	K11	P_{33}
A10	X_{13}	D2	P_5, Y_5	H10	TSM	L2	P_{17}
B1	P_2, Y_2	D10	SUB	H11	PREL	L3	P_{19}
B2	P_1, Y_1	D11	RND	J1	P_{15}, Y_{15}	L4	P_{21}
B3	X_0	E1	GND	J2	P_{14}, Y_{14}	L5	P_{23}
B4	X_2	E2	P_7, Y_7	J10	P_{34}	L6	P_{25}
B5	X_4	E10	CLK X	J11	CLK P	L7	P_{27}
B6	X_6	E11	ACC	K1	NC	L8	P_{29}
B7	X_8	F1	P_9, Y_9	K2	P_{16}	L9	P_{31}
B8	X_{10}	F2	P_8, Y_8	K3	P_{18}	L10	NC

Functional Description

General Information

The TMC2210 consists of four functional sections: input registers, an asynchronous multiplier array, an adder and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array uses a modified Booth's algorithm and has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the MSP, the LSP and the XTP. Three-state output drivers permit the TMC2210 to be used on a bus or allow the outputs to be multiplexed over the same 16-bit output lines. The LSP is multiplexed with the Y input.

The TMC2210 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. The Round (RND), Two's Complement (TC), Accumulate (ACC) and Subtract (SUB) inputs are registered and all four bits are clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Signal Definitions

Power

V_{DD}, GND — The TMC2210 operates from a single +5V supply. All power and ground lines must be connected.

Data Inputs

X_{15-0}, Y_{15-0} — There are two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information when two's complement notation is used. The remaining bits are denoted X_{14-0} and Y_{14-0} (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers on the rising edge of the appropriate clock.

Data Outputs

P_{34-0} — There is a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the MSP and LSP, and one 3-bit output word, the XTP. The MSB of the XTP is the sign bit if two's complement notation is used.

Clocks

CLK X, CLK Y, CLK P — CLK X is the clock input for the X_{15-0} data register. CLK Y is the clock input for the Y_{15-0} data register. CLK P is the clock input for the product register.

Controls

TSX, TSM, TSL — TSX, TSM and TSL are three-state enable lines for the XTP, the MSP and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM or TSL is HIGH and enabled when the appropriate control is LOW.

PREL — PREL (Preload) is an active HIGH control which has several effects when active. First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL) and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RND — RND (Round) controls the addition of a one to the MSB of the LSP for rounding. When RND is HIGH, a one is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating.

Controls (cont.)

TC — TC (Two's Complement) controls how the device interprets data on the X and Y inputs. When TC is HIGH, both inputs are two's complement inputs. When TC is LOW, both inputs are unsigned magnitude only inputs. The necessary sign extension for negative two's complement numbers is provided internally.

ACC — When ACC (Accumulate) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers on the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated will be stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

SUB — The SUB (Subtract) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated, and the difference is stored back into the output register. When ACC is HIGH and SUB is LOW, the content of the output register is added to the next product generated and the sum is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

No Connects

NC — The pin grid array version of the TMC2210 has four pins which are not connected internally.

Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins	J0, N0 Package Pins	R1 Package Pins
Power	V_{DD}	Supply Voltage	F10	49	17, 18, 19, 20
	GND	Ground	E1	16	53, 54
Data Inputs	X_{15-0}	X Input Word	C11, B10, A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3	56-64, 1-7	1-10, 63-68
	Y_{15-0}	Y Input Word	J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3	24-17, 15-8	45-52, 55-62
Data Outputs	P_{34-0}	Product Output	J10, K11, K10, L9, K9, L8, K8, L7, K7, L6, K6, L5, K5, L4, K4, L3, K3, L2, K2, J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3	43-17, 15-8	26-52, 55-62
Clocks	CLK X	X Register Clock	E10	51	15
	CLK Y	Y Register Clock	F11	50	16
	CLK P	P Regsiter Clock	J11	44	25
Controls	TSX	XTP Three-State	G10	47	22
	TSM	MSP Three-State	H10	45	24
	TSL	LSP Three-State	C10	55	11
	PREL	Preload	H11	46	23
	RND	Round	D11	54	12
	TC	Two's Complement	G11	48	21
	ACC	Accumulate	E11	52	14
	SUB	Subtract	D10	53	13
No Connects	NC	No Connection	K1, L10, B11, A2	–	–

Figure 1. Fractional Two's Complement Notation

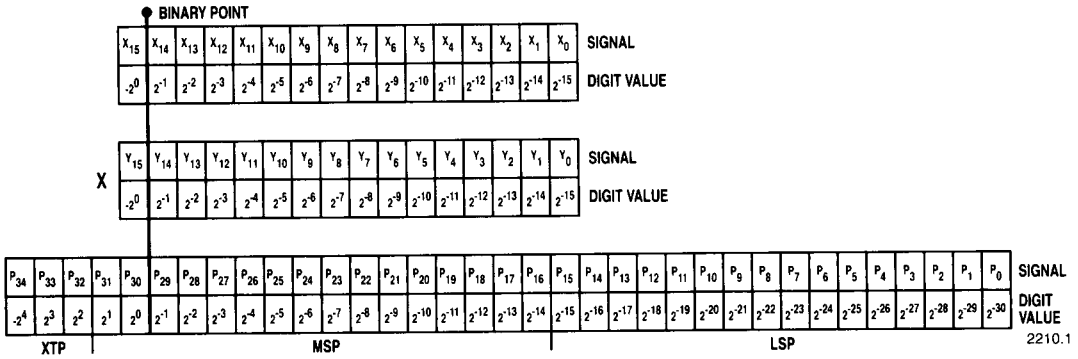


Figure 2. Fractional Unsigned Magnitude Notation

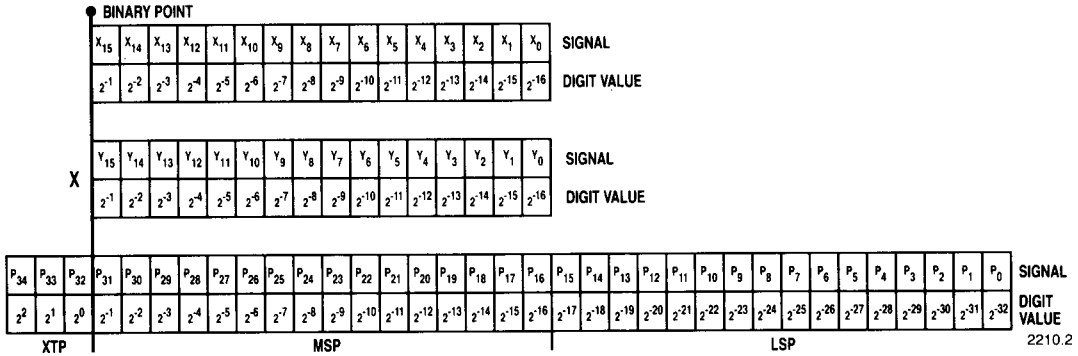


Figure 3. Integer Two's Complement Notation

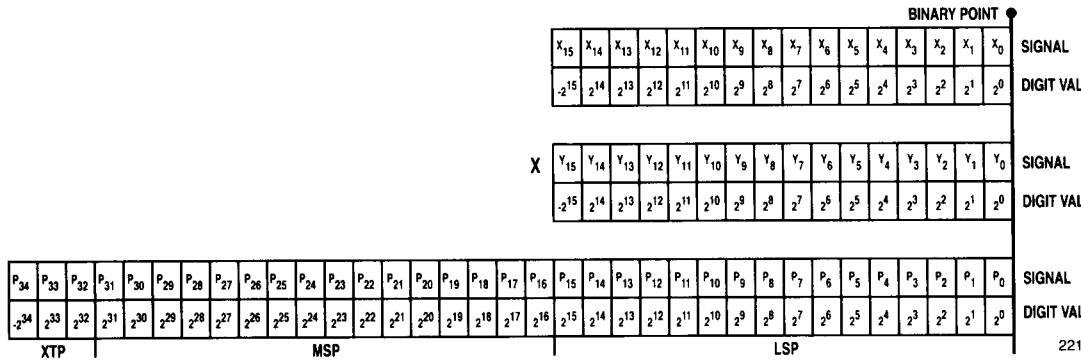


Figure 4. Integer Unsigned Magnitude Notation

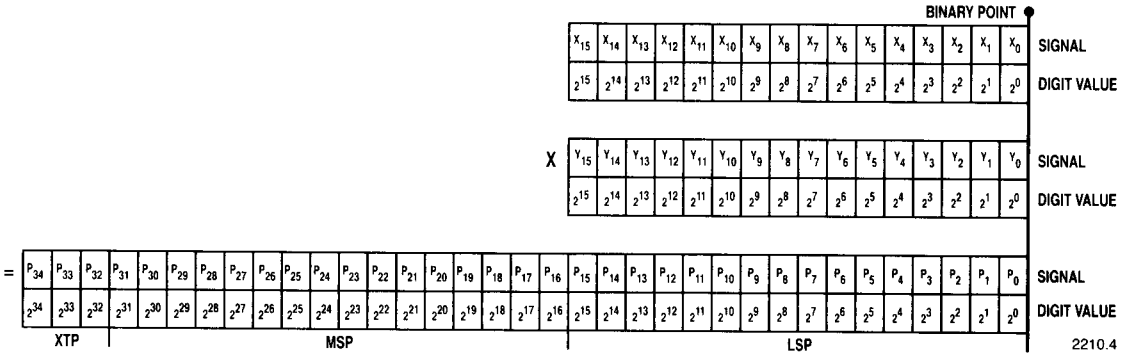


Figure 5. Timing Diagram

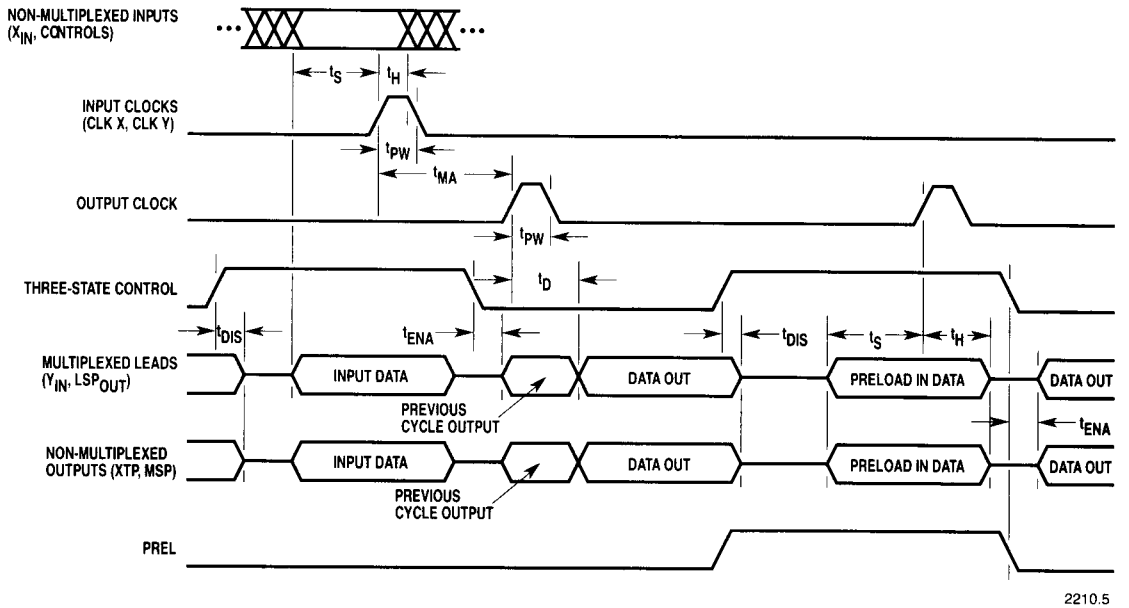


Figure 6. Equivalent Input Circuit

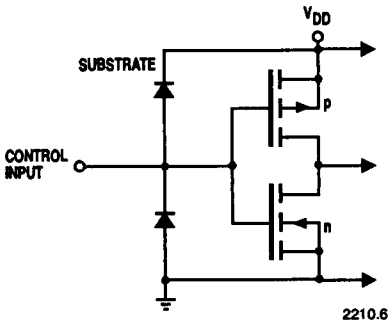


Figure 7. Equivalent Output Circuit

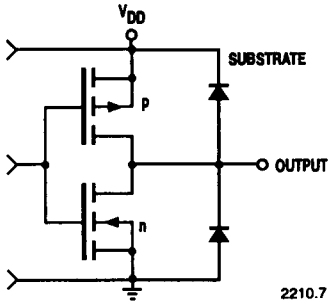
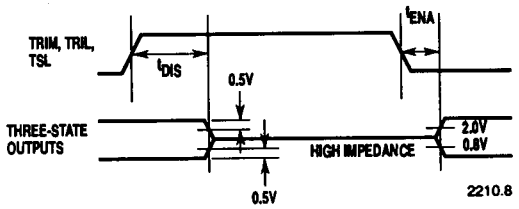


Figure 8. Threshold Levels for Three-State Measurements



Preload Truth Table

PREL[1, 2]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
0	0	0	0	Register → Output Pin	Register → Output Pin	Register → Output Pin
0	0	0	1	Register → Output Pin	Register → Output Pin	Hi-Z
0	0	1	0	Register → Output Pin	Hi-Z	Register → Output Pin
0	0	1	1	Register → Output Pin	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Register → Output Pin	Register → Output Pin
0	1	0	1	Hi-Z	Register → Output Pin	Hi-Z
0	1	1	0	Hi-Z	Hi-Z	Register → Output Pin
0	1	1	1	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	0	0	1	Hi-Z	Hi-Z	Hi-Z Preload
1	0	1	0	Hi-Z	Hi-Z Preload	Hi-Z
1	0	1	1	Hi-Z	Hi-Z Preload	Hi-Z Preload
1	1	0	0	Hi-Z Preload	Hi-Z	Hi-Z
1	1	0	1	Hi-Z Preload	Hi-Z	Hi-Z Preload
1	1	1	0	Hi-Z Preload	Hi-Z Preload	Hi-Z
1	1	1	1	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes: 1. PREL, TSX, TSM, and TSL are not registered.
2. When PREL is HIGH, any change of output register (for those outputs in which the three-state control is LOW) is inhibited.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Outputs	
Applied voltage	−0.5 to (V_{DD} + 0.5)V [2]
Forced current	−1.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range						
		Commercial			Military			
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V					
		All Except		5		10	mA
		TMC2210-45, -55, Outputs Open		0.5		0.5	mA
I_{DDO}	Supply Current, Unloaded [1]	V_{DD} = Max, TSL, TSM, TSX = 5V					
		f = 15MHz		75		75	mA
		f = 10MHz		50		50	mA
		f = 6.2MHz		30		30	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V					
		X_{15-0}, Controls, Clocks		−10		−10	mA
		P_{15-0}, Y_{15-0}		−40		−40	mA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}					
		X_{15-0}, Controls, Clocks		10		10	mA
		P_{15-0}, Y_{15-0}		40		40	mA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = +4.0mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −400μA	2.6		2.6		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		−40		−40	μA
C_I	Input Capacitance	f = 1.0MHz, T_A = 25°C		10		10	pF
C_O	Output Capacitance	f = 1.0MHz, T_A = 25°C		10		10	pF
$C_{I/O}$	I/O Capacitance	f = 1.0MHz, T_A = 25°C		15		15	pF

Note: 1. Supply current is proportional to f_{CLK}, typically 5mA per MHz.

AC characteristics within specified operating conditions [1]

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	TMC2210-95		95		95	ns
		TMC2210-80		80		80	ns
		TMC2210-65		65		65	ns
t_{PWL}	Clock Pulse Width, LOW	TMC2210-95	15		15		ns
		TMC2210-80	15		15		ns
		TMC2210-65	15		25		ns
t_{PWH}	Clcok PUlse Width, HIGH	TMC2210-95	15		15		ns
		TMC2210-80	15		15		ns
		TMC2210-65	15		25		ns

Notes: 1. All transitions are measured at a 1.5V level except t_{ENA} and t_{DIS} which are measured as shown in Figure 8.
2. V_{DD} = Min.

Fixed-Point

AC characteristics within specified operating conditions [1] (cont.)

Parameter		Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
t_S	Input Setup Time	Data, ACC, SUB, RND, TC					
		TMC2210-95	20		20		ns
		TMC2210-80	20		20		ns
		TMC2210-65	15		25		ns
		PREL, TSL, TSM, TSX					
		TMC2210-95	30		30		ns
		TMC2210-80	30		30		ns
		TMC2210-65	30		25		ns
t_H	Input Hold Time	Data, ACC, SUB, RND, TC					
		TMC2210-95	0		0		ns
		TMC2210-80	0		0		ns
		TMC2210-65	0		3		ns
		PREL, TSL, TSM, TSX					
		TMC2210-95	3		3		ns
		TMC2210-80	3		3		ns
		TMC2210-65	3		3		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		40		40	ns
		TMC2210-80		35		35	ns
		TMC2210-65		35		35	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		40		40	ns
		TMC2210-80		30		35	ns
		TMC2210-65		30		30[2]	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40 pf					
		TMC2210-95		35		35	ns
		TMC2210-80		30		30	ns
		TMC2210-65		30		30[2]	ns

Notes: 1. All transitions are measured at a 1.5V level except t_{ENA} and t_{DIS} which are measured as shown in Figure 8.

2. V_{DD} = Min.

Application Discussion

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, there is no difference between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

Ordering Information

Product Number	Multiply/ Accumulate Time (ns)	Temperature	Screening	Package	Package Marking
TMC2210G8C65	65	STD: T_A = 0 to 70°C	Commercial	68-pin Ceramic Pin Grid Array	2210G8C65
TMC2210G8C80	80	STD: T_A = 0 to 70°C	Commercial	68-pin Ceramic Pin Grid Array	2210G8C80
TMC2210G8V65	65	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V65
TMC2210G8V80	80	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V80
TMC2210G8V95	95	EXT: T_C = -55 to 125°C	MIL-STD-883C	68-pin Ceramic Pin Grid Array	2210G8V95
TMC2210H8C65	65	STD: T_A = 0 to 70°C	Commercial	68-pin Plastic Pin Grid Array	2210H8C65
TMC2210H8C80	80	STD: T_A = 0 to 70°C	Commercial	68-pin Plastic Pin Grid Array	2210H8C80
TMC2210J0V80	80	EXT: T_C = -55 to 125°C	MIL-STD-883C	64-pin Hermetic Ceramic DIP	2210J0V80
TMC2210J0V95	95	EXT: T_C = -55 to 125°C	MIL-STD-883C	64-pin Hermetic Ceramic DIP	2210J0V95
TMC2210N0C65	65	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C65
TMC2210N0C80	80	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C80
TMC2210N0C95	95	STD: T_A = 0 to 70°C	Commercial	64-pin Plastic DIP	2210N0C95
TMC2210R1C65	65	STD: T_A = 0 to 70°C	Commercial	68-Lead Plastic J-Leaded Chip Carrier	2210R1C65
TMC2210R1C80	80	STD: T_A = 0 to 70°C	Commercial	68-Lead Plastic J-Leaded Chip Carrier	2210R1C65

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