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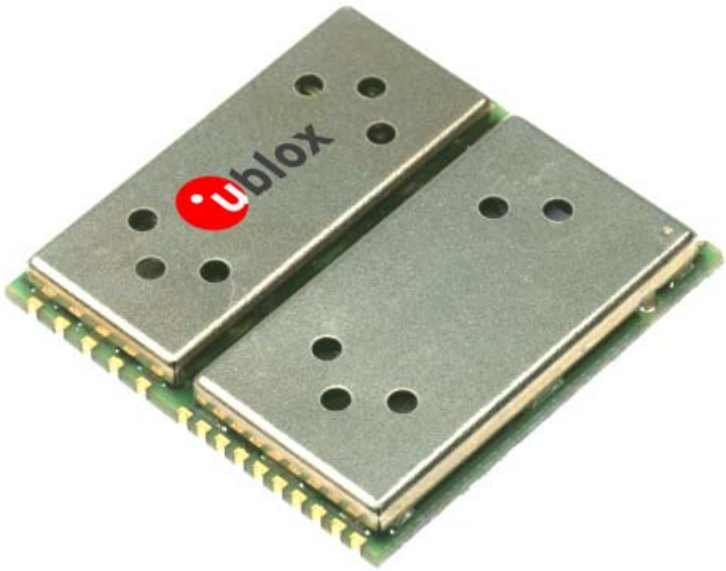
TIM-LL
GPS Receiver Module

Data Sheet



Abstract

This document describes the features and specifications of the TIM-LL module suitable for passive and active antennas. Based on the ANTARIS® GPS technology, it offers best GPS performance at very low power consumption.

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Data Sheet

Title	TIM-LL
Subtitle	GPS Receiver Module
Doc Type	Data Sheet
Doc Id	GPS.G3-MS3-04035-B

Revision Index	Date	Name	Status / Comments
P1	6. Aug. 04	GzB	Preliminary release
Initial Release	15. Sep. 04	GzB	Modified section 1.7, 1.8 and ordering information (introduced product variant 8)
A	17. June 05	GzB	Ordering information: Added TIM-LL-7
B	02. Feb. 06	GzB	Modified section 1.8, table 7 (RESET_N)

For most recent documents, please visit www.u-blox.com

Data Sheet Revisions	Identification of applicable hardware	Comments
P1, Initial Release	TIM-LL-0, all data codes TIM-LL-8, all data codes, TIM-LL-9, all data codes	TIM-LL-0: Standard GPS functionality TIM-LL-8: 8 Mbit SST Flash (SCKit users) TIM-LL-9: 8 Mbit AMD Flash (SCKit users)
A, B	TIM-LL-0, all data codes TIM-LL-7, all data codes, TIM-LL-8, all data codes, TIM-LL-9, all data codes	TIM-LL-0: Standard GPS functionality TIM-LL-7: 8 Mbit Atmel Flash (SCKit users) TIM-LL-8: 8 Mbit SST Flash (SCKit users) TIM-LL-9: 8 Mbit AMD Flash (SCKit users)

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Contents

1 Functional Description

1.1 Overview

The TIM-LL is an ultra-low power OEM GPS module suitable for passive and active antennas. It provides two 3V (5V TTL input compatible) serial ports, SPI and configurable 1.8V I/O ports. The TIM-LL provides system resources for user application software. The combination of high performance, maximum flexibility, and innovative packaging technology makes the TIM-LL suitable for high-volume applications requiring cost-effective and tight system integration.

The leading ANTARIS® GPS Engine, jointly developed by Atmel and u-blox, provides excellent navigation performance under dynamic conditions in areas with limited sky view like urban canyons, high sensitivity for weak signal operation without compromising accuracy, and support of DGPS and multiple SBAS systems like WAAS and EGNOS. The 16 parallel channels and 8192 search bins provide fast start-up times. The aiding functionality accelerates start-up times even further. The low power consumption and FixNow™ power saving mode make this product suitable for handheld and battery-operated devices.

Innovative packaging technologies enable high integration of a GPS receiver in a small module measuring just 25.4 x 25.4 mm and allowing straightforward integration in particularly small end products and opportunities in new application fields. The small form factor and the SMT pads allow a fully automatic assembly process with standard pick-and-place equipment and reflow soldering, enabling cost-efficient high-volume production.

1.2 Block Diagram

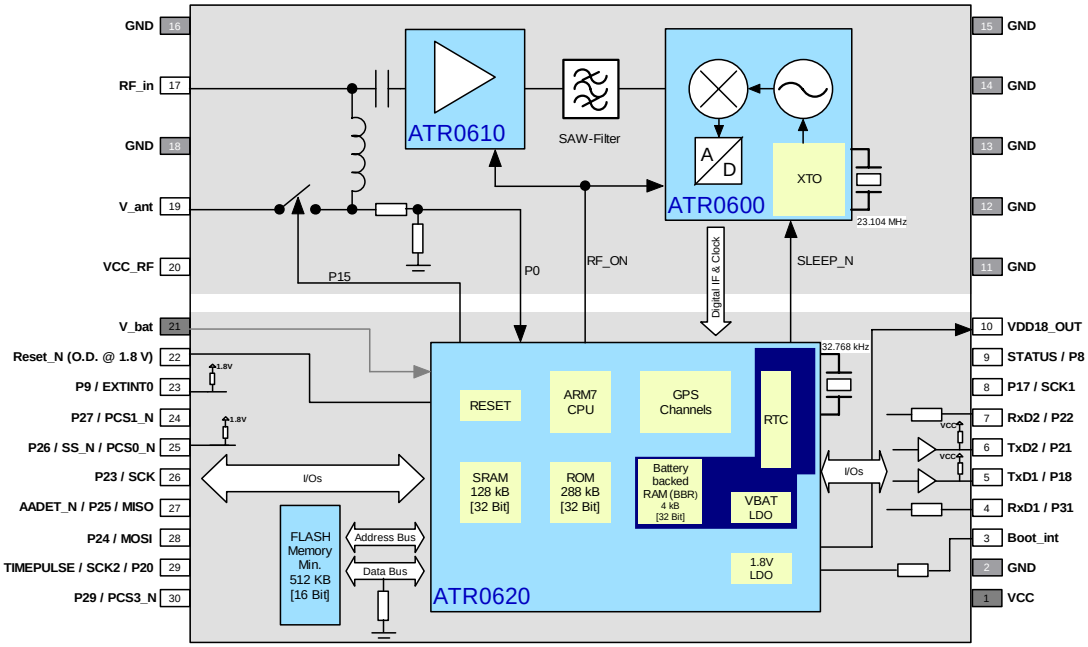

Figure 1: Block Diagram

1.3 Benefits

- High acquisition and tracking sensitivity
- Ultra-low power consumption
- Excellent GPS performance
  - Excellent navigation accuracy, even at low signal levels
  - Active multipath detection and removal
  - Fast Time-To-First-Fix (TTFF)
  - Accelerated TTFF with aiding functionality
- Highly integrated GPS module
  - Automatic pick and place assembly
  - Reflow solderable
- Maximum flexibility
  - Extensively configurable
  - Integration of user application software
- Fully EMI shielded
- Passive and Active antenna support

1.4 Features

- 16 channel GPS receiver
- 8192 simultaneous time-frequency search bins
- 4 Hz position update rate
- ANTARIS Positioning Engine
  - ATR0600 RF front-end IC
  - ATR0620 Baseband IC with ARM7TDMI inside
  - ATR0610 Low noise amplifier IC
- FLASH memory
- DGPS and SBAS (WAAS, EGNOS) support
- FixNOW™ power saving mode
- Operating voltage 2.7 to 3.3 V
- Battery supply pin for internal backup memory and real time clock
- Industrial operating temperature range –40 to 85°C
- Small size
  - Size 25.4mm x 25.4mm
  - Height 3mm
  - Weight 3g

1.5 Operating Modes

The ANTARIS GPS Technology defines the following Operating Modes:

Operating Modes	Description
Continuous Tracking Mode (CTM)	The Continuous Tracking Mode is configured for optimal position accuracy. This mode is optimized for power consumption based on the ANTARIS Autonomous Power Management (APM) saving as parts of the receiver are switched off when they are not required; also the CPU clock speed is reduced when the CPU is not loaded. There is no need for a user to configure this mode as it is built into the architecture of the module.
Power Saving Modes	
FixNOW™ (FXN)	FixNOW™ Mode allows an application a navigation solution on request. It includes additional Power Saving Functions and is the best mode for any Mobile, Tracking Unit application where low power consumption requirements are primary consideration. This mode can be configured to meet application requirements.

Table 1: Operating Modes

For more information see the *ANTARIS System Integration Manual* [1].

1.6 Protocols

The TIM-LL supports different serial protocols. These can be assigned to any serial interface port.

Protocol	Type	Runs on
NMEA	Input/output, ASCII, 0183, 2.3 (compatible to 3.0)	All Serial ports
UBX	Input/output, binary, u-blox proprietary	All Serial ports
RTCM	Input, message 1,2,3,9	All Serial ports

Table 2: Available Protocols

For specification of the various protocols see the *Protocol Specification* [2].

1.7 Available Resources

The product variants TIM-LL**-7**, **-8** and **-9** (see see section 6.2 for ordering information) are available for use with customized software created with the ANTARIS SCKit (Software Customization Kit).

Resources		Characteristics
Processor	ARM7TDMI running at 23 MHz	3.75 - 9 MIPS [1] @ 1 Hz navigation update rate
Memory	Flash EPROM SRAM	1 MB (physical memory size for all code) 8 kB
Interfaces	USARTs, synchronous and asynchronous operation SPI (Master and slave operation)	2 interfaces, 3 V levels 3 chip-select signals, 1.8 V levels
Digital I/Os	7 GPIOs 1 GPIO, interrupt-capable	1.8 V levels 1.8 V levels (Pin EXTINT0 / P9)

Table 3: Available Resources

[1] "VAX MIPS", calculated using Dhrystone, available for user code

1.8 Antenna

This GPS receiver is designed for use with passive and active antennas. An antenna supervisor is provided. If activated, the GPS receiver is capable of detecting short circuits to the active antenna by checking the bias voltage level and can shut down the voltage bias immediately. A series resistor is needed in front of the **V_ANT** input. UBX and NMEA messages are provided to report the condition of the antenna supply. Open circuit detection can also be supported with an additional external circuit. For details, please refer to the *ANTARIS System Integration Manual* [1].

Parameter	Specification	
Antenna Type		Passive and active antenna
Active Antenna Recommendations	Minimum gain	10 - 15 dB (to compensate signal loss in RF cable)
	Maximum noise figure	1.5 dB
	Maximum gain	45 dB
Built-in LNA		Atmel ATR0610
Antenna Supply		Using **VCC_RF**
		or external
Antenna Supervisor	Short circuit detection	Built-in
	Open circuit detection	Enabled with external circuit

Table 4: Antenna Specification

2 Performance Specification

Parameter	Specification			
Receiver Type		L1 frequency, C/A Code, 16-Channels 8192 search bins		
Max Update Rate		4 Hz		
Accuracy (Selective Availability off)	Position	2.5 m CEP[3]	5.0 m SEP[4]	
	Position DGPS / SBAS[2]	2.0 m CEP	3.0 m SEP	
Acquisition[5]		Fast Acquisition Mode	Normal Mode	High Sensitivity Mode
	Cold Start[6]	34 s	36 s	41 s
	Warm Start	33 s		
	Hot Start	<3.5 s		
	Aided Start[7]	5 s		
Signal Reacquisition		<1 s		
Sensitivity[8]		Fast Acquisition Mode	Normal Mode	High Sensitivity Mode
	Acquisition	-134 dBm	-138 dBm	-140 dBm
	Tracking	-143 dBm	-146 dBm	-149 dBm
Timepulse Accuracy	RMS	50 ns		
	99%	<100 ns		
	Granularity	43 ns		
Dynamics		≤ 4 g		
Operational Limits		COCOM restrictions		

Table 5: Performance Specification

[2] Depends on accuracy of correction data of DGPS or SBAS service
[3] CEP = Circular Error Probability: The radius of a horizontal circle, centered at the antenna's true position, containing 50% of the fixes.
[4] SEP = Spherical Error Probability. The radius of the sphere, centered at the true position, contains 50% of the fixes.
[5] The different start-up modes like cold, warm and hot start are described in the System Integration Manual [1]
[6] Measured with good visibility and -125 dBm signal strength
[7] Time synch. signal from aiding source must be supplied to **EXTINT0** pin, having accuracy of better than 200 µs
[8] Demonstrated with a good active antenna

3 Mechanical Specification

3.1 Dimensions

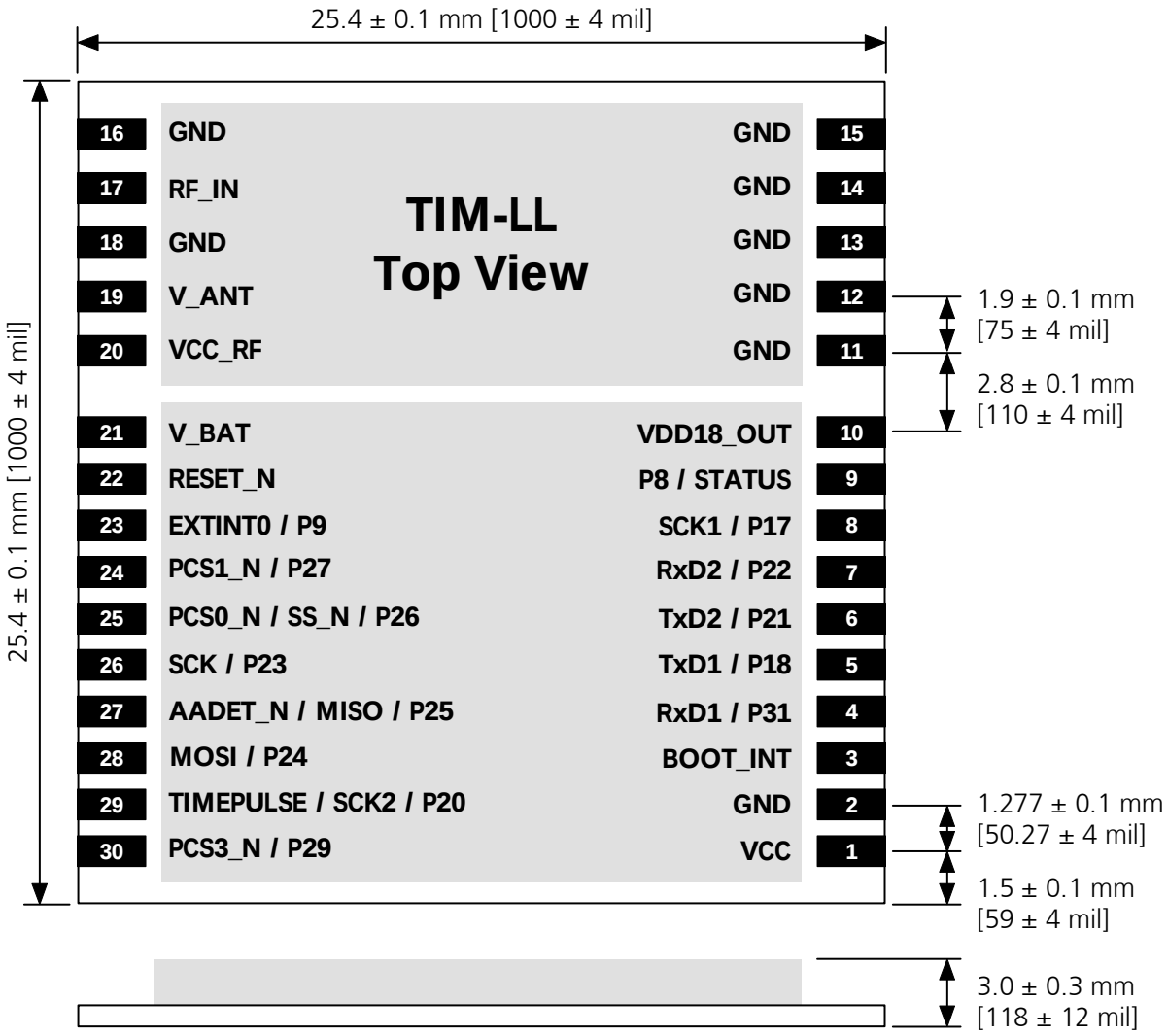

Figure 2: TIM-LL Dimensions

3.2 Specification

Parameter	Specification	Tolerance	Unit
Length	25.4	±0.1	mm
Width	25.4	±0.1	mm
Thickness	3.0	±0.3	mm
Pitch RF pins	1.9	±0.1	mm
Pitch Digital pins	1.277	±0.1	mm
Weight	3		g

Table 6: Mechanical Specification

3.3 Pinout

Standard Function				Alternate Functions[9]			Remarks
Pin	Name	I/O	Description	Name	I/O	Description	
1	VCC	I	Supply voltage				
2	GND	I	Ground				
3	BOOT_INT	I	Boot mode				Leave open if not used (normal operation)
4	RxD1	I	Serial Port 1				Pull up if not used
5	TxD1	O	Serial Port 1				Leave open if not used
6	TxD2	O	Serial Port 2				Leave open if not used
7	RxD2	I	Serial Port 2				Pull up if not used
8	P17	I/O	GPIO	SCK1	I/O	synch. serial port 1 clock	Default config. to output, leave open if not used
9	STATUS	O	GPS Status				Leave open if not used
10	VDD18_Out	O	1.8V supply output				Suitable as reference for external level shifter
11 – 16	GND	I	Ground				
17	RF_IN	I	GPS signal input				Apply no DC through this pin
18	GND	I	Ground				
19	V_ANT	I	Antenna Bias voltage				Connect to GND if not used
20	VCC_RF	O	Output Voltage RF section				May be connected to V_ANT
21	V_BAT	I	Backup voltage supply				Connect to GND if not used
22	RESET_N	I/O	Reset (Active low)				Concerning use of RESET_N signal, please refer to the ANTARIS System Integration Manual [1]
23	EXTINT0	I	External Interrupt Pin	P9	I/O	GPIO	Internal pull-up, Leave open if not used
24	P27	I/O	GPIO	PCS1_N	O	SPI Chip Select 1	Default config. to output, leave open if not used
25	P26	I/O	GPIO	SS_N PCS0_N	I O	SPI Slave Select SPI Chip Select 0	Internal pull-up, Leave open if not used
26	P23	I/O	GPIO	SCK	I/O	SPI clock	Default config. to output, leave open if not used
27	AADET_N [10]	I	Active Antenna Detect	P25 MISO	I/O I/O	GPIO SPI MISO	Default config. to output (!), leave open if not used
28	P24	I/O	GPIO	MOSI	I/O	SPI MOSI	Default config. to output, leave open if not used
29	TIMEPULSE	O	Timepulse signal				Leave open if not used
30	P29	I/O	GPIO[11]	PCS3_N	O	SPI Chip Select 3	Default config. to output, leave open if not used

Shaded pins operate with 1.8V signal levels

Table 7: Signals and Module Interface

[9] ANTARIS™ Software Customization Kit needed to explore alternate functions
[10] AADET_N will only be operated as input pin if "Open Circuit Detection" for active antennas is activated or configured. Otherwise, it will operate as an output pin unless custom software configures this pin otherwise.
[11] Standard software allows this pin to be connected to GND externally

4 Electrical Specification

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply (VCC and V_BAT)				
Power supply voltage	Vcc	-0.3	3.6	V
Input Pins				
Input pin voltage (1.8V inputs, RESET_N)	Vio	-0.3	1.95	V
Input pin voltage (RxD1, RxD2)	Vrxd	-0.3	8	V
BOOT_INT pin	Vboot	-0.3	3.3	V
Voltage Supply output for Active Antenna and RF Section				
VCC_RF output current	Iccrf		50	mA
RF Input				
Antenna bias voltage (applied via V_ANT)	Vant	0	8	V
Antenna bias current (applied via V_ANT)	Iant		100	mA
Input power at RF_IN (source impedance 50Ω, continuous wave)	Prfin		-17	dBm
Environment				
Storage temperature	Tstg	-40	125	°C

Table 8: Absolute Maximum Ratings

! Warning Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

4.2 Operating Conditions

Parameter[12]	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Power supply voltage	Vcc		2.7		3.3	V
Power supply voltage ripple	Vcc_PP				50	mV
Sustained supply current [13]	Icc	Vcc = 3.0 V		54		mA
Peak supply current [14]	Iccp	Vcc = 3.3 V			125	mA
Sleep mode current	Iccs	Vcc = 3.0 V		100		µA
Backup battery voltage	Vbat		1.95		3.6	V
Backup battery current	Ibat	Vbat = 3.3 V		15	40 (prelim.)	µA
1.8V output voltage (VDD18_Out pin)	Vdd18out		1.65	1.8	1.95	V
1.8V output current (VDD18_Out pin)	Idd18out				20	mA

Table 9: Operating Conditions

[12] All specification are at an ambient temperature of 25°C.
[13] Average current drawn during Continuous Tracking Mode with 1 Hz update rate, using 6 satellites for tracking and navigation. Use this figure to determine required battery capacity
[14] Peak current drawn during initial acquisition phase. Use this figure to dimension maximum current capability of power supply

Parameter[15]	Symbol	Condition	Min	Typ	Max	Units
1.8V Digital I/Os and RESET_N						
Input pin voltage range	Vin18		0V		Vdd18out	V
Input pin low voltage	Vin_low18				0.45	V
Input pin high voltage	Vin_high18		1.4			V
Output pin voltage range	Vout18		0V		Vdd18out	V
Output pin low voltage	Vout_low18	Iout < 0.3 mA (sink)			0.1	V
Output pin high voltage	Vout_high18	Iout < 0.3 mA (source)	1.55			V
Output pin current at low voltage	Iout_low18	Vout_low18 = 0.28 V			2	mA
Output pin current at high voltage	Iout_high18	Vout_high18 = 1.35 V			2	mA
Input leakage current	Iin_leak18				1	µA
TxD1 and TxD2 Pins						
Output pin voltage range	VoutT		0V		Vcc	V
Output pin low voltage	Vout_lowT	Iout < 100µA (sink)			0.1	V
	Vout_lowT	Iout < 16mA (sink)			0.4	V
Output pin high voltage	Vout_highT	Iout < 10µA (source)	Vcc - 0.2			V
	Vout_highT	Iout < 40µA (source)	Vcc - 0.5			V
Output pin current at low voltage	Iout_lowT	Vout_lowT = 0.24 V			4	mA
Output pin current at high voltage	Iout_highT	Vout_highT = Vcc-0.5 V			40	µA
RxD1 and RxD2 Pins						
Input pin voltage range	VinR		0		5.5	V
Input pin low voltage	Vin_lowR				0.4	V
Input pin high voltage	Vin_highR		1.5	Vcc		V
BOOT_INT Pin						
Input pin voltage range	VinB		0		Vcc	V
Input pin low voltage	Vin_lowB				0.4	V
Input pin high voltage	Vin_highB		2.7	Vcc		V
RF input						
Input power	Prfin				-61	dBm
V_ANT antenna bias voltage (must connect to ground if not used)	Vant		1.8		8	V
Antenna bias voltage drop	Vant_drop	Iant=10mA			50	mV
VCC_RF voltage	Vccrf			Vcc – 0.1		V
Environment						
Operating temperature	Topr		-40		85	°C

Table 9: Operating Conditions (continued)

Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability. The technical data apply to products where standard ANTARIS firmware is running.

[15] All specification are at an ambient temperature of 25°C.

5 Environmental Specification

Detailed description of the test series:

Test		Standard
Visual inspection		IPC-A-610 "Acceptability of electronic assemblies" I.T.R.I. Publication No. 700 IPC-SM-840B Class 2.
Thermal shock	-40°C...+125°C, 100 cycles	IEC 68-2-14
Function at various temperatures	-40°C/2 hours; RT/2 hours; +85°C/2 hours; function tests at stable temperature	IEC 68-2-1 and IEC 68-2-2
Lifespan test	+85°C/1000 hours, in function	IEC 68-2-2
Damp heat, cyclic	+25°C...+55°C; >90% rH	IEC 68-2-30
Vibration Shock	10-500 Hz; 2 hours/axis; 5g 30g/11ms (halfsine); 3 Shock/axis; no function	IEC 68-2-6 IEC 68-2-27
Metallographic investigations		IPC-QE-650

Note: This specification is preliminary and yet subject to confirmation.

Table 10: Environmental Specification

6 Product Lineup

6.1 Default Settings

Interface	Settings
Serial Port 1 Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, ZDA, TXT** Additional messages can be activated with appropriate input messages.
Serial Port 1 Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA, RTCM** The GPS receiver supports interleaved UBX and NMEA messages.
Serial Port 2 Output	57600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following UBX and no NMEA messages have been activated at start-up: **NAV-POSLLH, NAV-SOL, NAV-SVINFO, NAV-STATUS** MON-IO, MON-SCHD, MON-TXBUF, INF-Warning, INF-Error, INF-Notice Additional messages can be activated with appropriate input messages.
Serial Port 2 Input	57600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA, RTCM** The GPS receiver supports interleaved UBX and NMEA messages.
TIMEPULSE	1 pulse per second, synchronized at rising edge, pulse length 100ms

Table 11: Available Protocols

6.2 Ordering Information

Ordering No.	Product
TIM-LL-0-000-0	TIM-LL GPS Receiver Module Delivery Packing **0** = Single samples **1** = Tape on reel (100 pieces) **5** = Tape on reel (500 pieces) Flash EPROM Configuration **0** = Standard GPS functionality. Not for ANTARIS SCKit users For ANTARIS SCKit users only: **7** = 8 Mbit (Flash EPROM: Atmel AT49SV802A) **8** = 8 Mbit (Flash EPROM: SST SST39WF800A) **9** = 8 Mbit (Flash EPROM: AMD AM29SL800DT) Availability of these two variants varies depending on availability of the corresponding Flash EPROMs. Custom software shall support both Flash EPROMs.

Table 12: Ordering Information

Parts of this product are patent protected.

Related Documents

[1] ANTARIS TIM-Lx GPS Modules, System Integration Manual, Docu. No GPS.G3-MS3-01001

[2] ANTARIS GPS Technology - Protocol Specification, Docu. No GPS.G3-X-03002

All these documents are available on our homepage (http://www.u-blox.com).

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