mosaic

Mosaic Semiconductor Inc.

256K x 1 CMOS SRAM

MSM1256-45/55

Issue 2.0 : FEBRUARY 1993

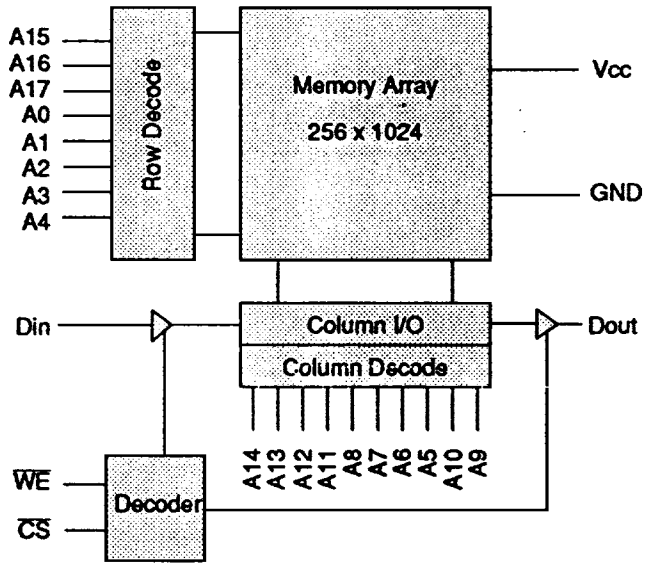
PRELIMINARY

262,144 x 1 CMOS High Speed Static RAM

Features

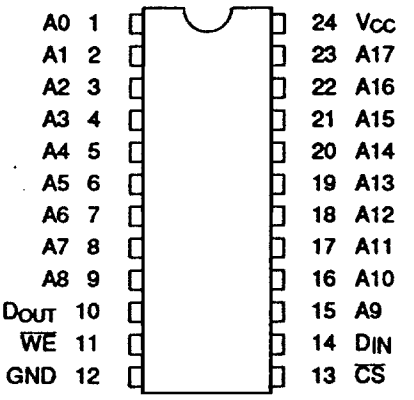
Very Fast Access Times of 45/55 ns
Standard 24 pin Dual-in-Line Package
High Density 24 Pin VIL and 28 Pad LCC
Low Power Operation 300 mW (typ)
Low Power Standby 30 µW (typ)-L Version
Completely Static Operation.
Equal Access and Cycle Times.
Directly TTL Compatible
Common Data Inputs & Outputs
May be Processed to MIL-STD-883 (suffix MB)

Block Diagram

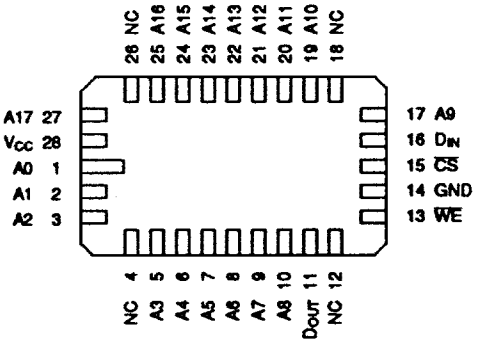


Pin Definitions

Package Type: 'T', 'V'



Package Type: 'W'



Pin Functions

A0-A17	Address inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power(+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
24	0.3" Dual-in-Line (DIP)	T	Ceramic	JEDEC
24	0.1" Vertical-in-Line (VIL)	V	Ceramic	JEDEC
28	Ceramic Leadless Chip Carrier(LCC)	W	Ceramic	JEDEC

Package details and dimensions on page 5.

VIL is a trademark of Mosaic Semiconductor Inc., US patent number D316251.

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_{IN} min = -2.5V for pusle width ≤ 10ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.5(1)	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (suffix I)
	T_{AM}	-55	-	125	°C (suffix M, MB)

Note: (1) V_{IL} min = -2.0V for pusle width ≤ 10ns.

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	-	-	10	µA
Operating Supply Current	I_{CC1}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	60	100	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min. Cycle	-	15	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	20	2000	µA
- Low Power	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	6	100	µA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}= -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

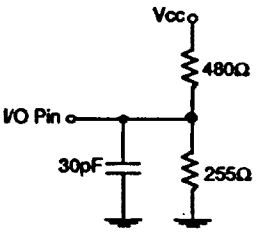
Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$ = 0V	-	10	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions Output Load

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%



Electrical Characteristics & Recommended AC Operating Conditions

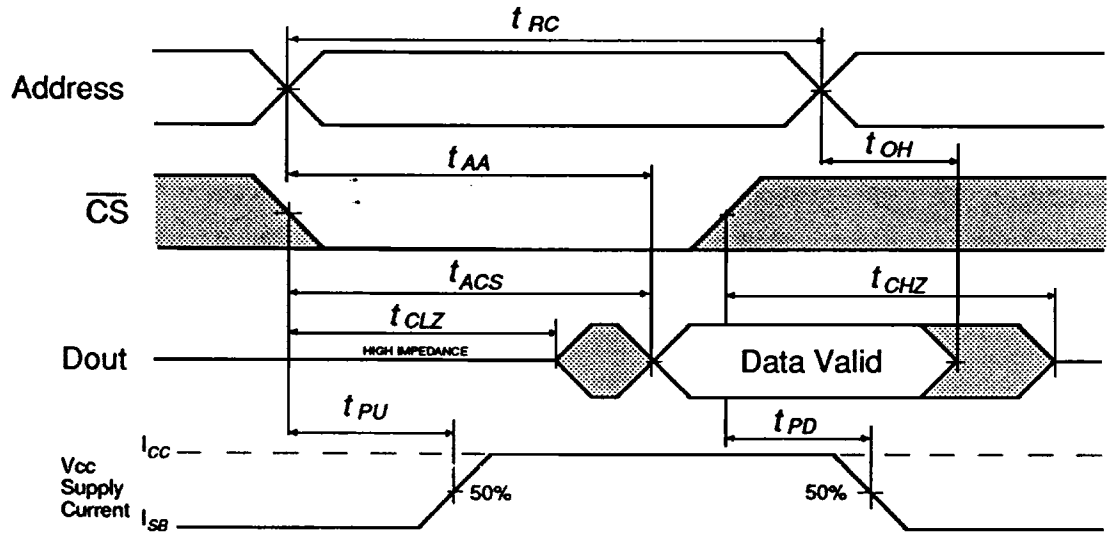
Read Cycle (1)

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	Unit
Read Cycle Time	t_{RC}	45	-	55	-	ns
Address Access Time	t_{AA}	-	45	-	55	ns
Chip Select Access Time	t_{ACS}	-	45	-	55	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Chip Select to Output in Low Z (2)	t_{CLZ}	5	-	5	-	ns
Chip Deselection to O/P in High Z (2)	t_{CHZ}	0	30	0	35	ns
Chip Select to Power up Time	t_{PU}	0	-	0	-	ns
Chip Disable to Power Down	t_{PD}	-	40	-	45	ns

Notes: (1) $\overline{WE}$ is High for Read Cycle.

(2) t_{CHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

Read Cycle Timing Waveform



Write Cycle

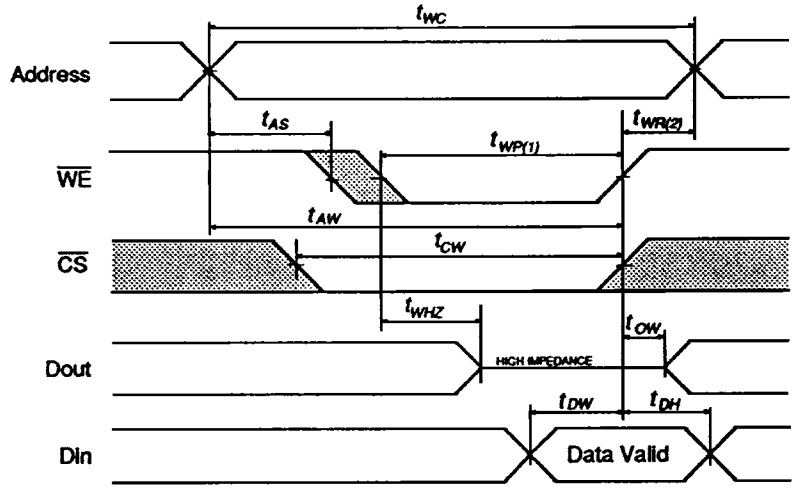
Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	Unit
Write Cycle Time	t_{WC}	45	-	55	-	ns
Chip Selection to End of Write	t_{CW}	40	-	45	-	ns
Address Valid to End of Write	t_{AW}	40	-	45	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	40	-	ns
Write Recovery Time	t_{WR}	3	-	3	-	ns
Write to Output in High Z (3)	t_{WHZ}	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}	0	-	0	-	ns

Notes: (1) A Write occurs during the overlap of $\overline{CS}$ and $\overline{WE}$.

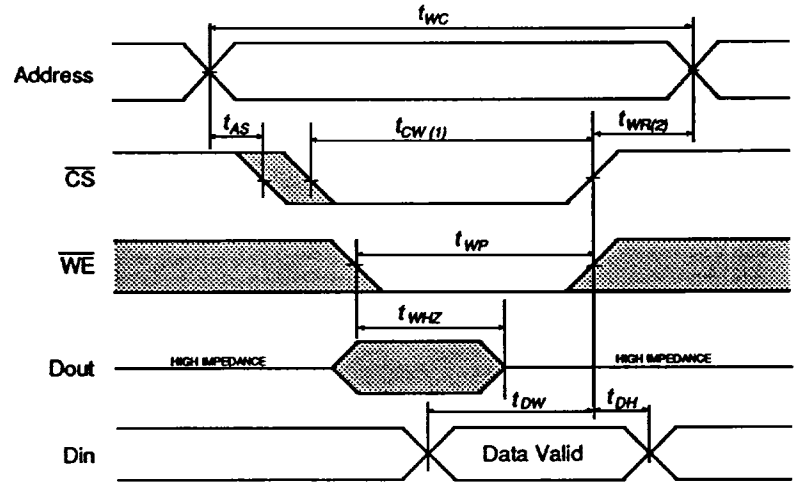
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of Write Cycle.

(3) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Write Cycle 1 Timing Waveform ($\overline{WE}$ Controlled)



Write Cycle 2 Timing Waveform ($\overline{CS}$ Controlled)

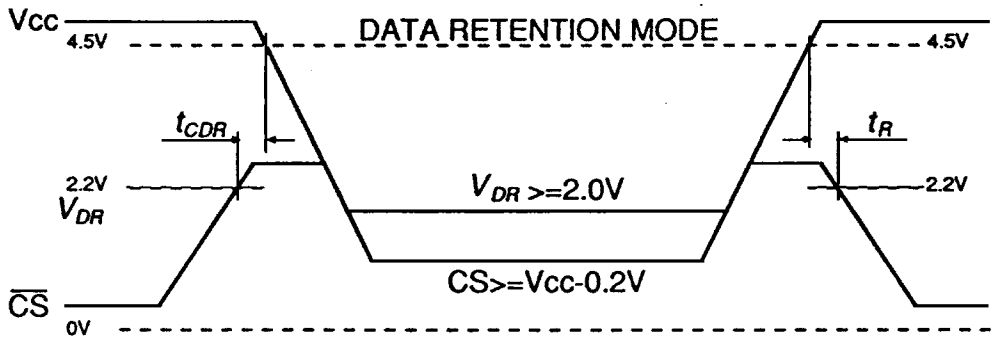


Low V_{cc} Data Retention Characteristics - L Version Only (T_A= -55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2	-	1	50	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} (1)	-	-	ns

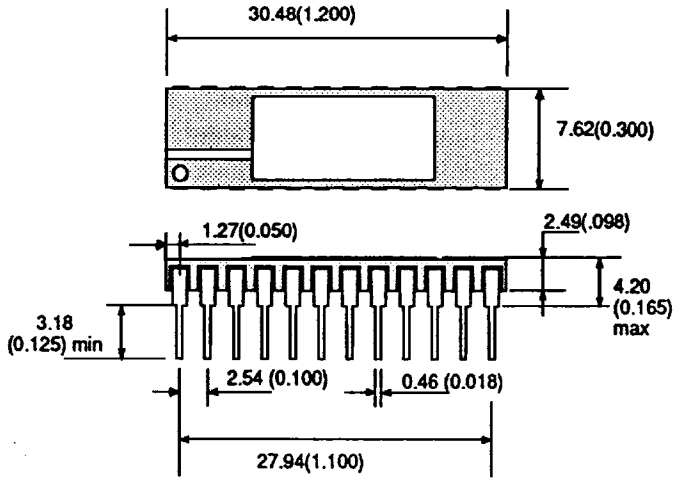
Notes: (1) t_{RC}=Read Cycle Time

Low V_{CC} Data Retention Timing Waveform

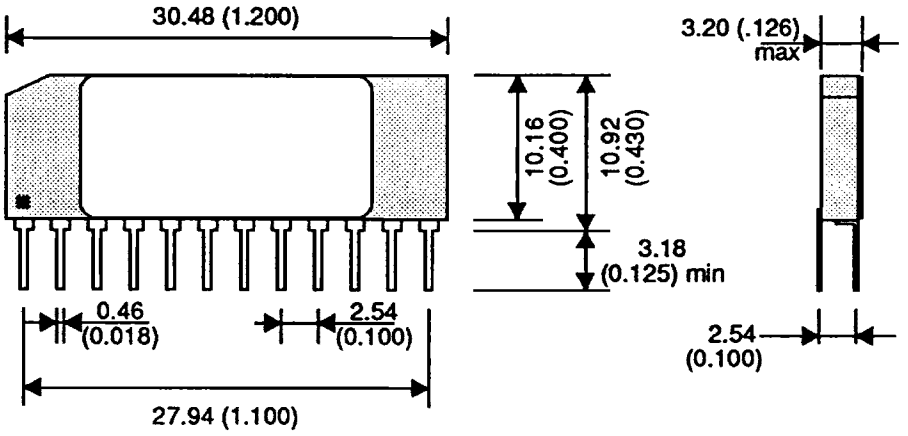


Package Details Dimensions in mm (inches). Tolerance on all dimensions ±0.254(0.010).

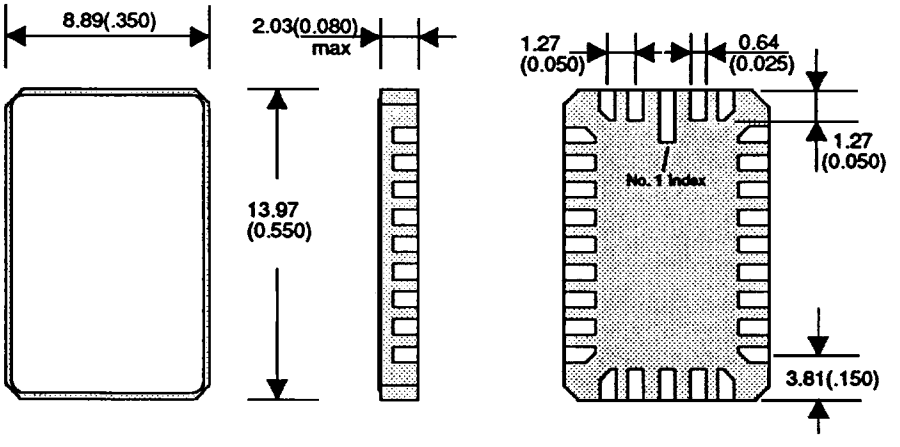
24 Pin DIL ('T' Package)



24 Pin Vertical- In- line (VIL™) 'V' Package



28 Pad Leadless Chip Carrier (LCC) 'W' Package



Ordering Information

MSM1256VLMB-45

Speed	45	= 45ns
	55	= 55ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
Power	Blank	= Standard Power
	L	= Low Power
Package	T	= 24 Pin 300 mil DIP
	V	= 24 Pin 100 mil VIL™
	W	= 28 Pad LCC

Note: For more information regarding screening flows, contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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