

Digital Step Attenuator

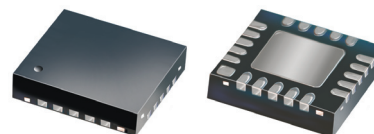
75Ω DC-2000 MHz

15.5 dB, 0.5 dB Step

5 Bit, Serial Control Interface, Single Positive Supply Voltage, +3V

Product Features

- Single positive supply voltage, +3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Serial control interface
- Low Insertion Loss
- High IP3, +52 dBm typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm



DAT-15575-SP+
DAT-15575-SP

CASE STYLE: DG983-1

PRICE: \$3.55 ea. QTY. (10-24)

Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

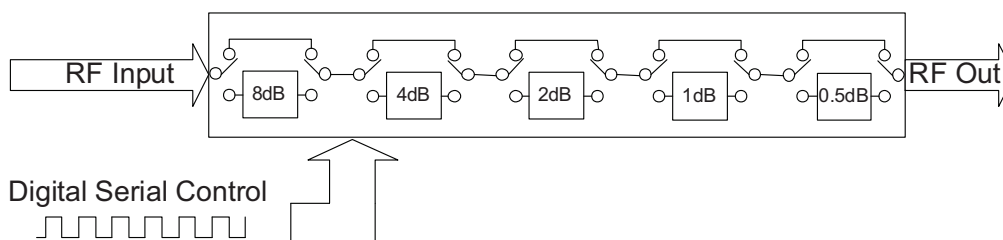
*+ RoHS compliant in accordance
with EU Directive (2002/95/EC)*

The +Suffix identifies RoHS Compliance. See our web site for
RoHS Compliance methodologies and qualifications.

General Description

The DAT-15575-SP is a 75Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit serial interface, operating on a single +3 volt supply. The DAT-15575-SP is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



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REV. E
M125066
DAT-15575-SP
100207
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Digital Step Attenuator

DAT-15575-SP+
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RF Electrical Specifications, DC-2000 MHz, $T_{AMB}=25^{\circ}\text{C}$, $V_{DD}=+3\text{V}$

| Parameter | Freq. Range (GHz) | Min. | Typ. | Max. | Units |
|--|-------------------|------|------|------|-------|
| Accuracy @ 0.5 dB Attenuation Setting | DC-1.2 | — | 0.03 | 0.17 | dB |
| | 1.2-2.0 | — | 0.05 | 0.18 | dB |
| Accuracy @ 1 dB Attenuation Setting | DC-1.2 | — | 0.03 | 0.19 | dB |
| | 1.2-2.0 | — | 0.1 | 0.2 | dB |
| Accuracy @ 2 dB Attenuation Setting | DC-1.2 | — | 0.07 | 0.23 | dB |
| | 1.2-2.0 | — | 0.15 | 0.25 | dB |
| Accuracy @ 4 dB Attenuation Setting | DC-1.2 | — | 0.05 | 0.25 | dB |
| | 1.2-2.0 | — | 0.15 | 0.35 | dB |
| Accuracy @ 8 dB Attenuation Setting | DC-1.2 | — | 0.1 | 0.25 | dB |
| | 1.2-2.0 | — | 0.24 | 0.55 | dB |
| Insertion Loss ^(note1) @ all attenuator set to 0dB | DC-1.2 | — | 1.2 | 1.8 | dB |
| | 1.2-2.0 | — | 1.6 | 2.1 | dB |
| Input IP3 ^(note 2) (at Min. and Max. Attenuation) | DC-2.0 | — | +52 | — | dBm |
| Input Power @ 0.2dB Compression ^(note 2) (at Min. and Max. Attenuation) | DC-2.0 | — | +24 | — | dBm |
| VSWR | DC-1.2 | — | 1.6 | 2.0 | — |
| | 1.2-2.0 | — | 1.7 | 2.0 | — |

Notes:

1. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.40dB @1200MHz, 0.55dB @2000MHz, 0.75dB @4000MHz)
2. Input IP3 and 1dB compression degrades below 1 MHz

DC Electrical Specifications

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------|---------------------|------|---------------------|---------------|
| V_{DD} , Supply Voltage | 2.7 | 3 | 3.3 | V |
| I_{DD} , Supply Current | — | — | 100 | μA |
| Control Input Low | — | — | $0.3 \times V_{DD}$ | V |
| Control Input High | $0.7 \times V_{DD}$ | — | — | V |
| Control Current | — | — | 1 | μA |

Switching Specifications

| Parameter | Min. | Typ. | Max. | Units |
|--|------|------|------|-----------------|
| Switching Speed, 50% Control to 0.5dB of Attenuation Value | — | 1.0 | — | μSec |
| Switching Control Frequency | — | — | 25 | KHz |

Absolute Maximum Ratings

| Parameter | Ratings |
|-----------------------|---------------------------------------|
| Operating Temperature | -40°C to 85°C |
| Storage Temperature | -55°C to 100°C |
| V_{DD} | -0.3V Min., 4V Max. |
| Voltage on any input | -0.3V Min., $V_{DD}+0.3\text{V}$ Max. |
| ESD, HBM | 500V |
| ESD, MM | 100V |
| Input Power | +24dBm |

Permanent damage may occur if any of these limits are exceeded.



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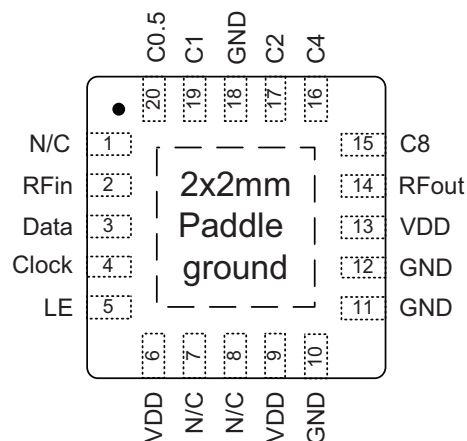
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Pin Description

| Function | Pin Number | Description |
|-----------------|------------|--|
| N/C | 1 | Not connected (Note 5) |
| RF in | 2 | RF in port (Note 1) |
| Data | 3 | Serial Interface data input (Note 3) |
| Clock | 4 | Serial Interface clock input |
| LE | 5 | Latch Enable Input (Note 2) |
| V _{DD} | 6 | Power Supply |
| N/C | 7 | Not connected |
| N/C | 8 | Not connected |
| V _{DD} | 9 | Power Supply |
| GND | 10 | Ground connection |
| GND | 11 | Ground connection |
| GND | 12 | Ground connection |
| V _{DD} | 13 | Power Supply |
| RF out | 14 | RF out port (Note 1) |
| C8 | 15 | Control for attenuation bit, 8 dB (Note 4) |
| C4 | 16 | Control for attenuation bit, 4 dB (Note 4) |
| C2 | 17 | Control for attenuation bit, 2 dB (Note 4) |
| GND | 18 | Ground Connection |
| C1 | 19 | Control for attenuation bit, 1 dB (Note 4) |
| C0.5 | 20 | Control for attenuation bit, 0.5 dB (Note 4) |
| GND | Paddle | Paddle ground (Note 6) |

Pin Configuration (Top View)



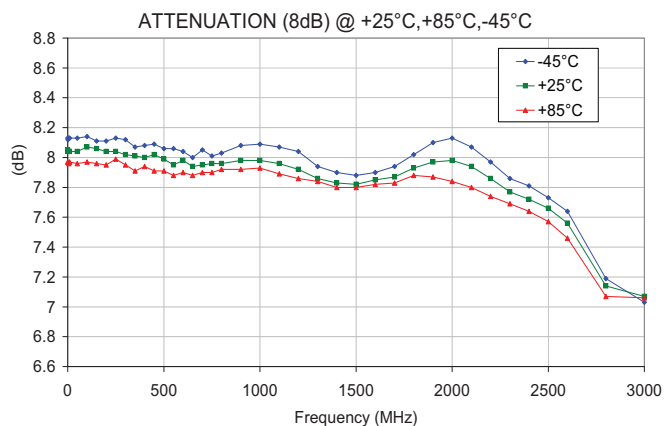
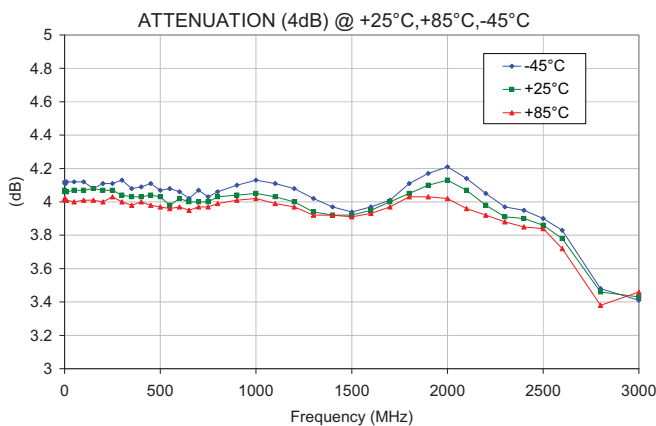
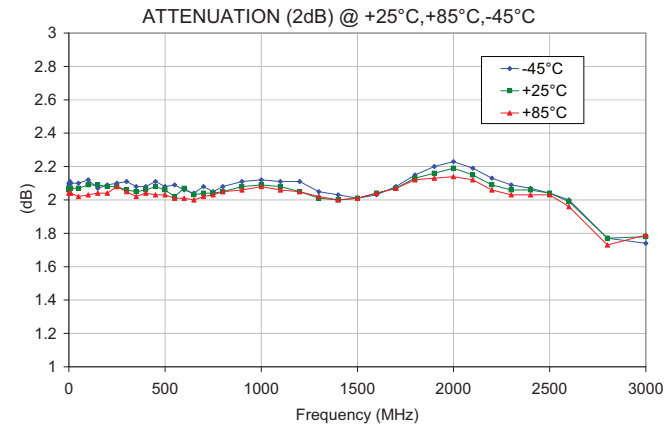
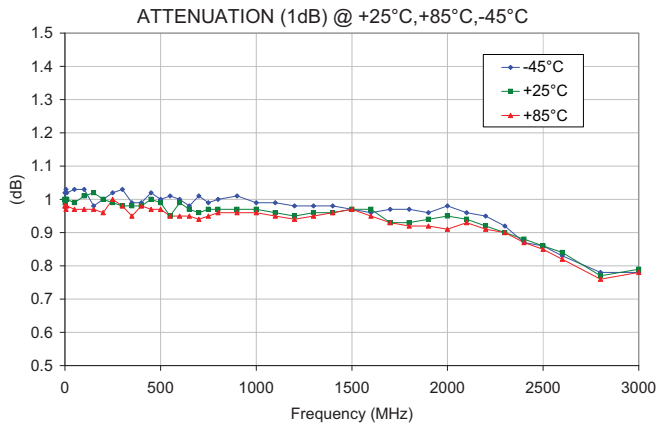
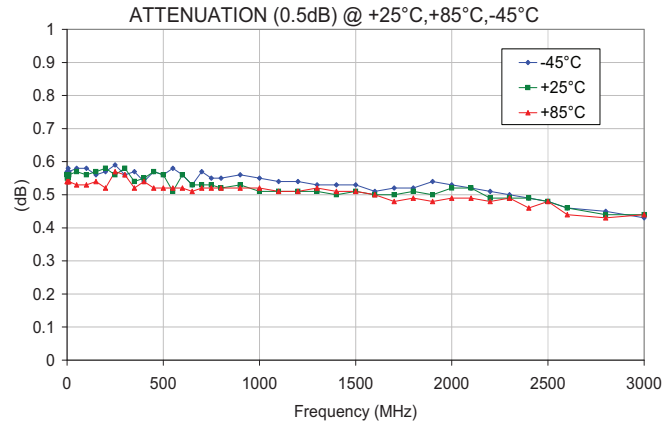
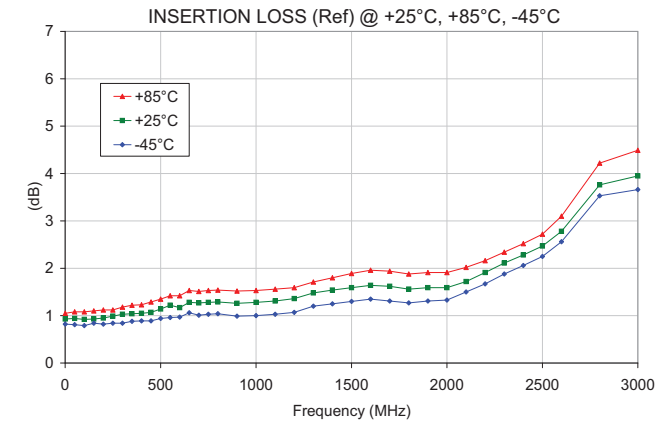
Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
- Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
- Refer to Power-up Control Settings.
- Place a shunt 10KΩ resistor to GND.
- The exposed solder pad on the bottom of the package (see Pin configuration) must be grounded for proper device operation.

Digital Step Attenuator

DAT-15575-SP+
DAT-15575-SP

Typical Performance Curves



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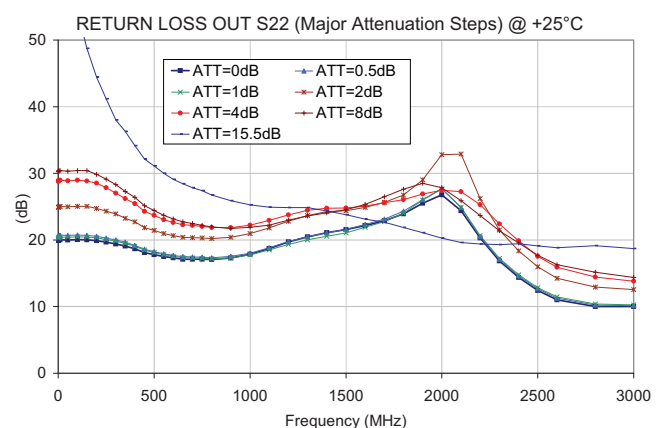
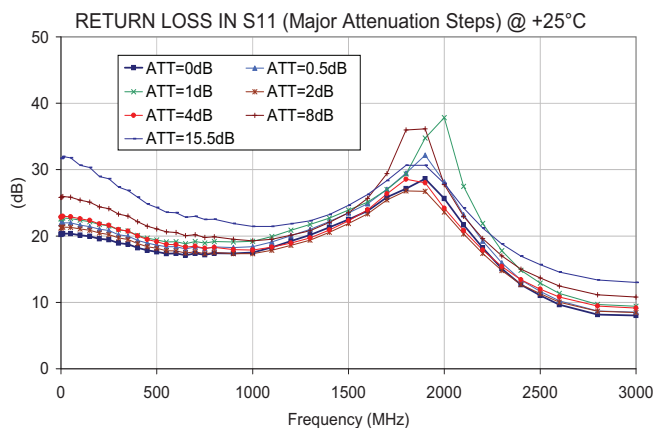
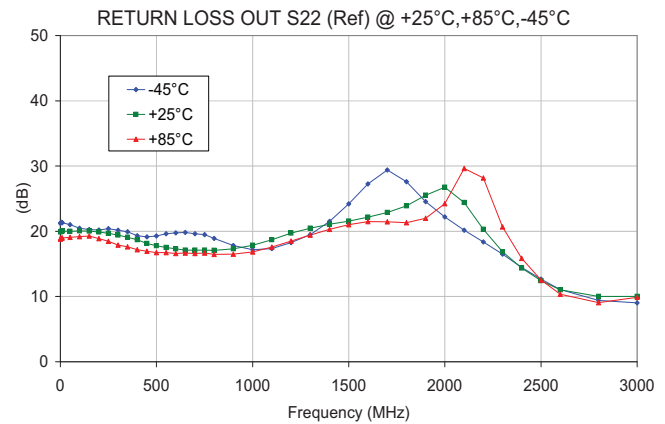
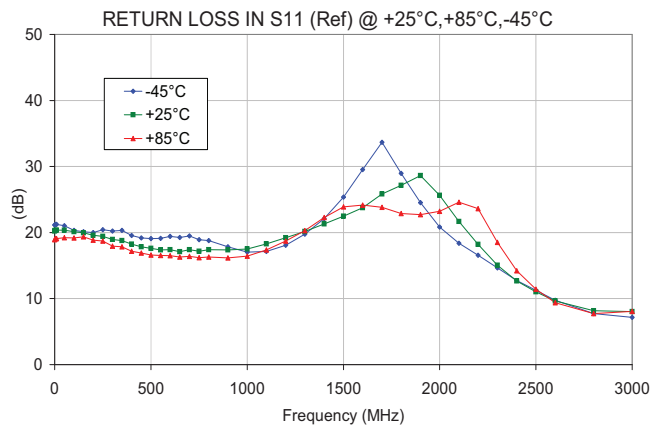
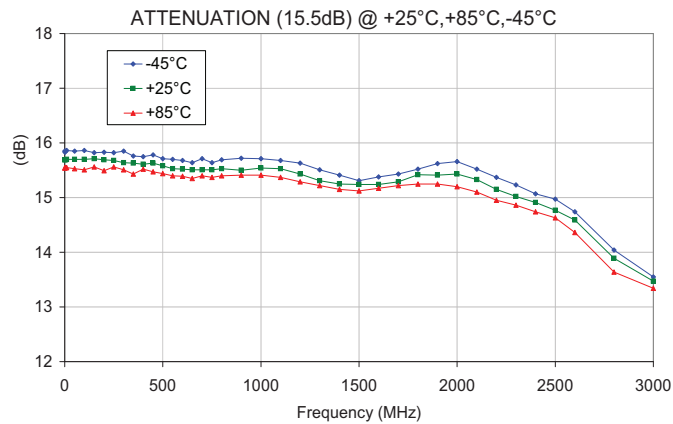
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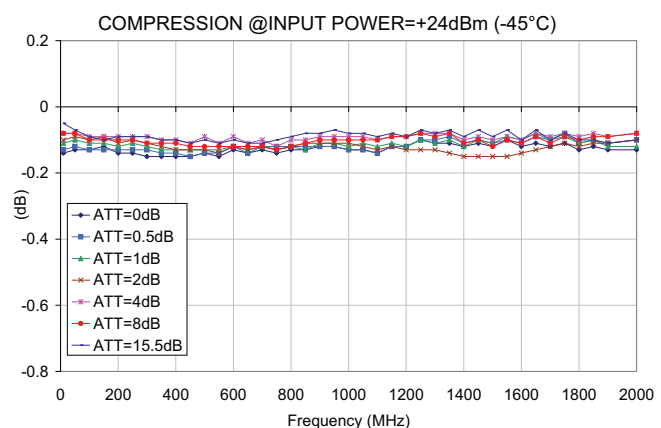
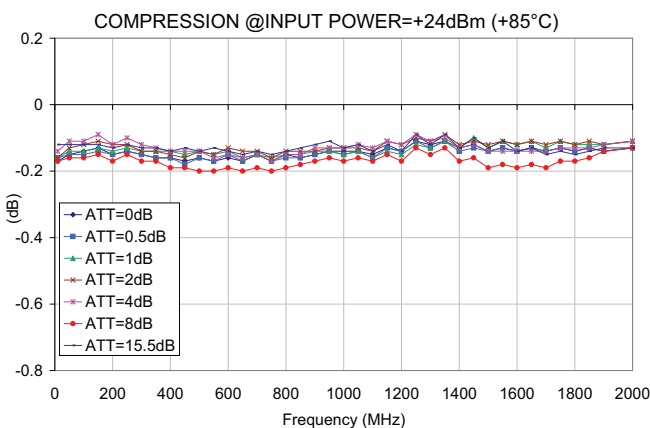
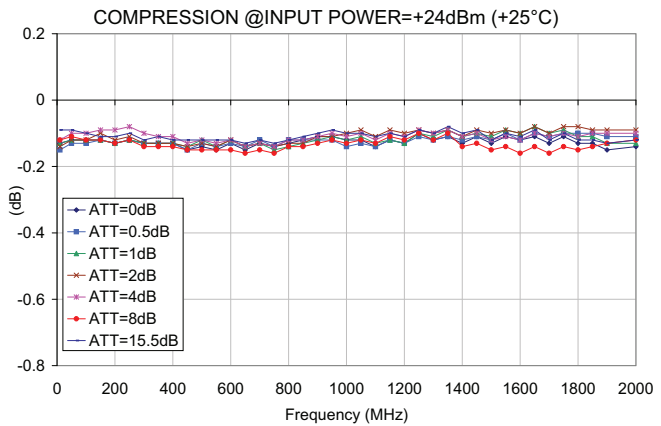
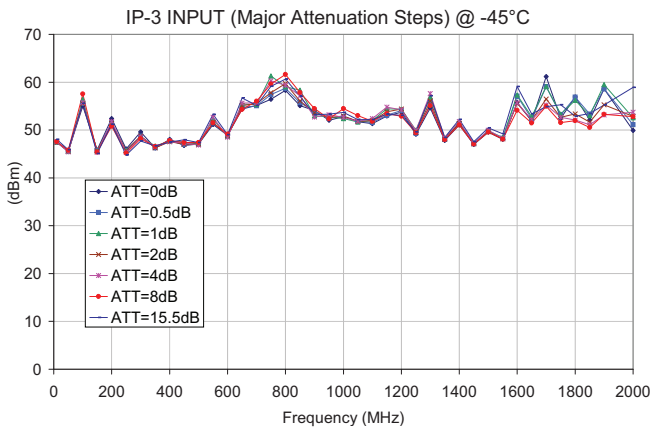
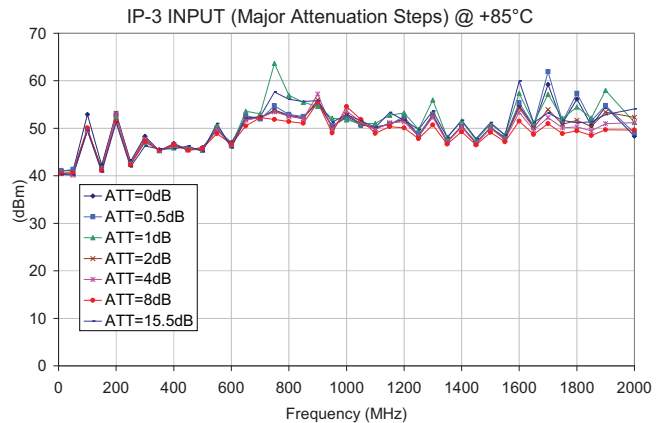
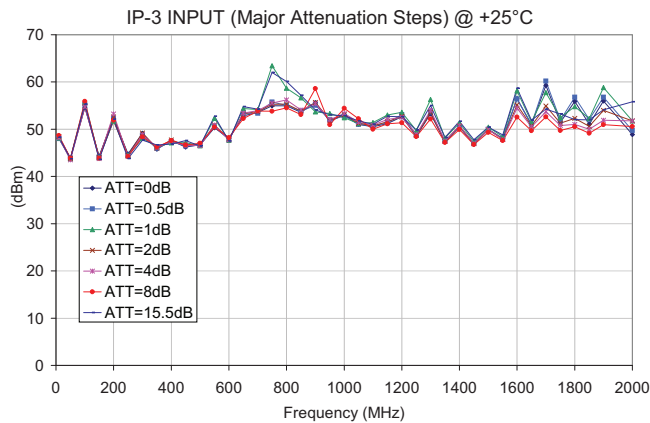
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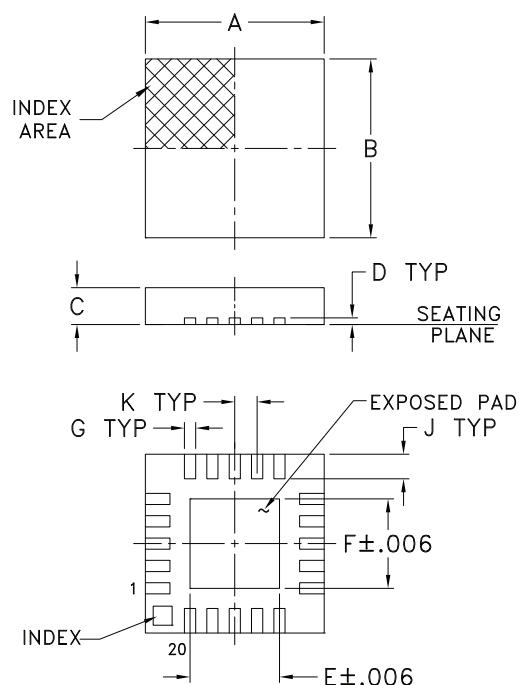
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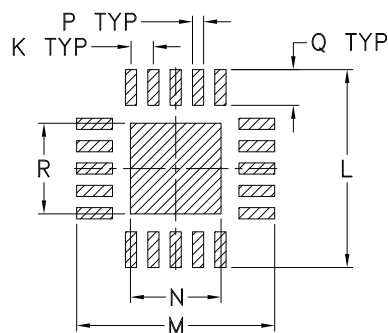
Digital Step Attenuator

DAT-15575-SP+
DAT-15575-SP

Outline Drawing (DG983-1)

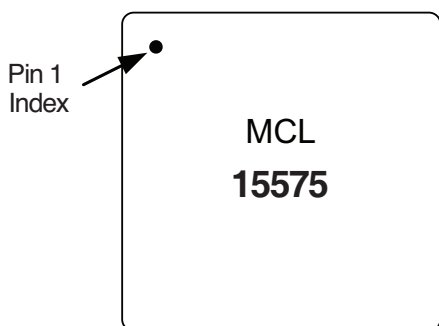


PCB Land Pattern



Suggested Layout,
Tolerance to be within $\pm.002$

Device Marking



Outline Dimensions (inch/mm)

| A | B | C | D | E | F | G | H | J | K | L | M | N | P | Q | R | WT. GRAMS |
|------|------|------|------|------|------|------|---|------|------|------|------|------|------|------|------|-----------|
| .157 | .157 | .035 | .008 | .081 | .081 | .010 | — | .022 | .020 | .177 | .177 | .081 | .010 | .032 | .081 | .04 |
| 4.00 | 4.00 | 0.90 | 0.20 | 2.06 | 2.06 | 0.25 | — | 0.56 | 0.50 | 4.50 | 4.50 | 2.06 | 0.25 | 0.81 | 2.06 | |

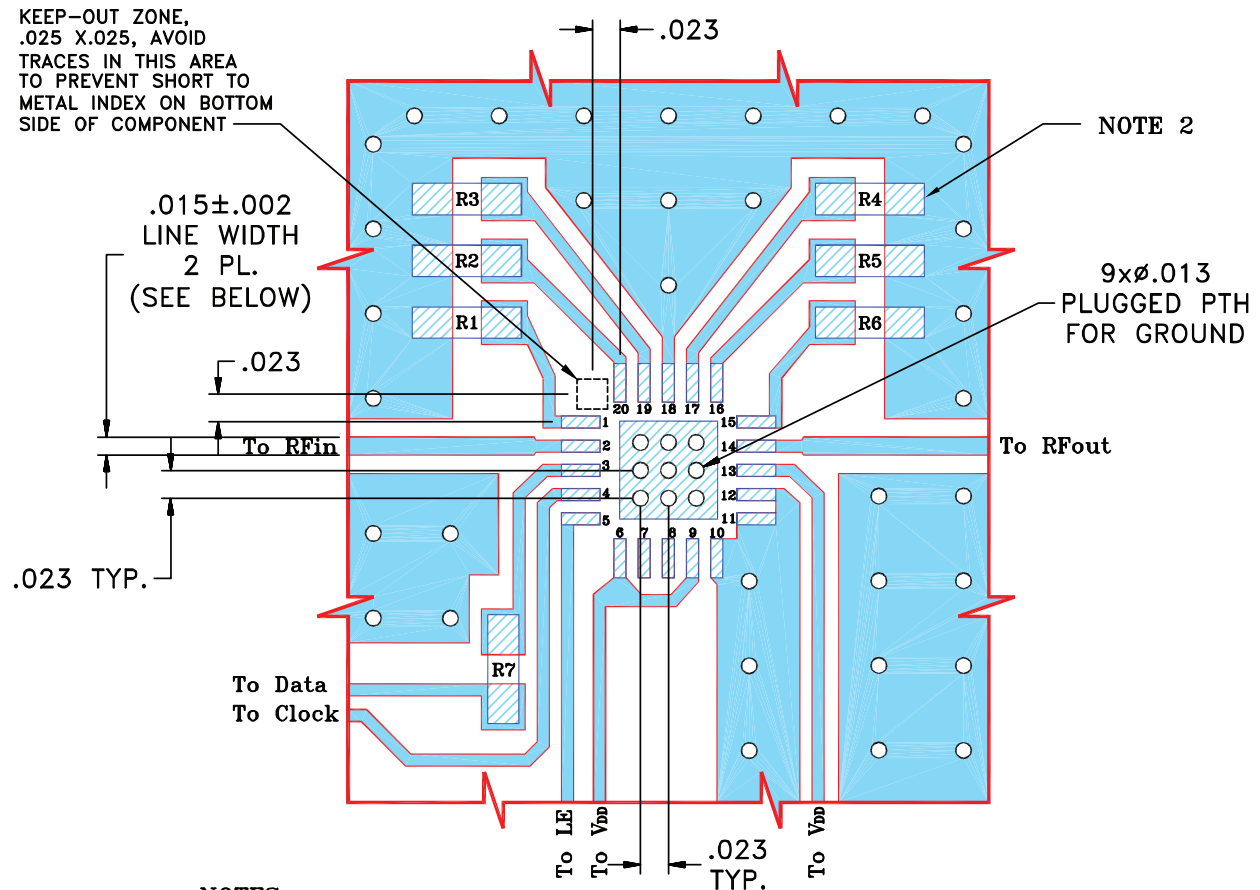
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Suggested Layout for PCB Design (PL-203)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1-R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



NOTES:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603 SIZE CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.



DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

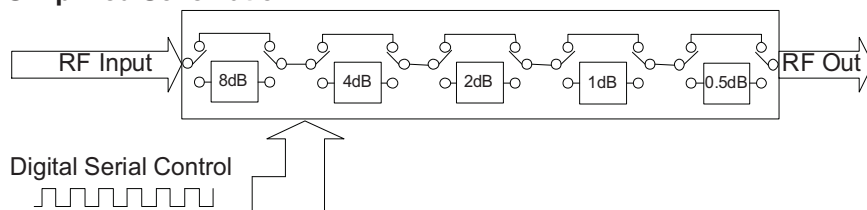


DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Digital Step Attenuator

DAT-15575-SP+
DAT-15575-SP

Simplified Schematic



The DAT-15575-SP Serial interface consists of 5 control bits that select the desired attenuation state, as shown in **Table 1**: Truth Table

| Table 1. Truth Table | | | | | |
|----------------------|----|----|----|----|------|
| Attenuation State | C8 | C4 | C2 | C1 | C0.5 |
| Reference | 0 | 0 | 0 | 0 | 0 |
| 0.5 (dB) | 0 | 0 | 0 | 0 | 1 |
| 1 (dB) | 0 | 0 | 0 | 1 | 0 |
| 2 (dB) | 0 | 0 | 1 | 0 | 0 |
| 4 (dB) | 0 | 1 | 0 | 0 | 0 |
| 8 (dB) | 1 | 0 | 0 | 0 | 0 |
| 15.5 (dB) | 1 | 1 | 1 | 1 | 1 |

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

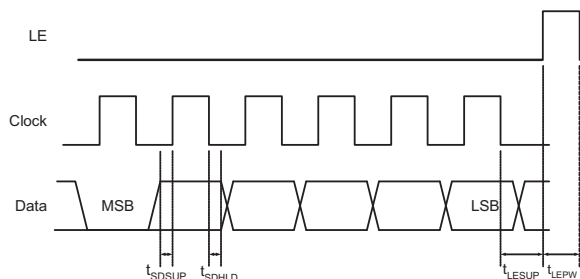
The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch.

It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by **Figure 1** (Serial Interface Timing Diagram) and **Table 2** (Serial Interface AC Characteristics).

Figure 1: Serial Interface Timing Diagram



| Table 2. Serial Interface AC Characteristics | | | | |
|--|--|------|------|-------|
| Symbol | Parameter | Min. | Max. | Units |
| f_{Clk} | Serial data clock frequency (Note 1) | | 10 | MHz |
| t_{ClkH} | Serial clock HIGH time | 30 | | ns |
| t_{ClkL} | Serial clock LOW time | 30 | | ns |
| t_{LESUP} | LE set-up time after last clock falling edge | 10 | | ns |
| t_{LEPW} | LE minimum pulse width | 30 | | ns |
| t_{SDSUP} | Serial data set-up time before clock rising edge | 10 | | ns |
| t_{SDHLD} | Serial data hold time after clock falling edge | 10 | | ns |

Note 1. Fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify Fclk specification.

Digital Step Attenuator

DAT-15575-SP+
DAT-15575-SP

The DAT-15575-SP, uses a common 5-bit serial word format, as shown in **Table 3**: 5-Bit attenuator Serial Programming Register Map.

Bit B4 corresponds to the 8-dB Step and the last bit, the LSB, corresponds to the 0.5 dB step.

| Table 3. 5-Bit attenuator Serial Programming Register Map | | | | | |
|---|----|----|----|----|------|
| B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | C8 | C4 | C2 | C1 | C0.5 |

↑ MSB (first in) Note: The start bit (B5) must always be low to prevent the attenuator from entering an unknown state. ↑ LSB (last in)

Power-up Control Settings

The DAT-15575-SP always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

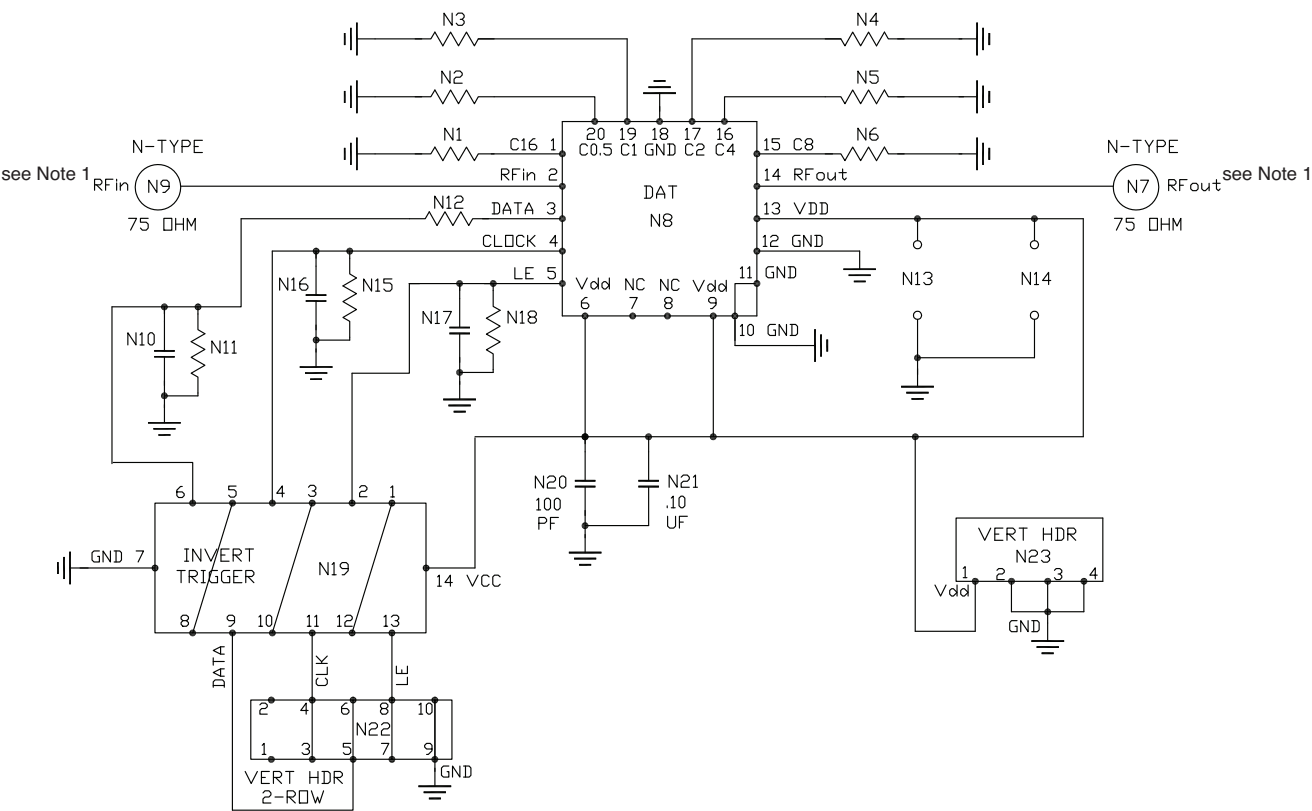
When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C0.5 to C8).

This allows any one of the 32 attenuation settings to be specified as the power-up state.

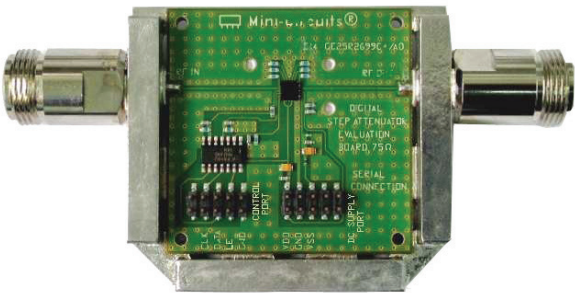
Digital Step Attenuator

DAT-15575-SP+
DAT-15575-SP

TB-344 Evaluation Board Schematic Diagram



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.



TB-344

| Bill of Materials | |
|---------------------------|---------------------------------------|
| N1-N6, N11, N12, N15, N18 | Resistor 0603 10 KOhm +/- 1% |
| N10, N16, N17, N20 | NPO Capacitor 0603 100pF +/- 5% |
| N21 | Tantalum Capacitor 0805 100nF +/- 10% |
| N19 | Hex Invert Schmitt Trigger MSL1 |

Table T&R

Ordering Information

| Model No. | Description | Packaging Designation Letter (See Table T&R) | Quantity Min. No. of Units | Price \$ Ea. |
|------------------|--|---|-------------------------------|--------------|
| DAT-15575-SP (+) | Serial Interface, Single Positive Voltage | E | 10 | \$3.55 |
| TB-344 | Test Board Only | Not Applicable | 1 | \$79.95 |

Example: 3000 pieces of DAT-15575-SP+

3K DAT-15575-SP+ T&R=T

Quantity Model No. T&R designation letter (see Table T&R)