P29FCT520AT/BT/CT — P29FCT521AT/BT/CT PIPELINE REGISTERS

FEATURES

- Function, Pinout and Drive Compatible with the FCT, F Logic and AM29520/521
- FCT-C speed at 6.0ns max. (Com'l) FCT-B speed at 7.5ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- Single and Dual Pipeline Operation Modes
- Multiplexed Data Inputs and Outputs
- Manufactured in 0.7 micron PACE Technology™

DESCRIPTION

The P29FCT520T and P29FCT521T are multi-level 8-bit wide pipeline registers. Each device consists of 4 registers A1, A2, B1 and B2 which are configured by the instruction inputs I_0, I_1 as a single 4-level pipeline or as two 2-level pipelines. The contents of any register may be read at the multiplexed output at any time by using the mux-selection controls S_0 and S_1.

The pipeline registers are positive edge triggered and data is shifted by the rising edge of the clock input. Instruction I = 0 selects the 4-level pipeline mode. Instruction I = 1 selects the 2-level B pipeline while I = 2 selects the 2-level A pipeline. I = 3 is the HOLD instruction; no shifting is performed by the clock in this mode.

The P29FCT520T and P29FCT521T differ only in the 2-level operation mode. For the P29FCT520T, data is shifted from level 1 to level 2 and new data is loaded into level 1. In the P29FCT521T, new data is overwritten into level 1. To shift data from level 1 to level 2 in the P29FCT521T, the 4-level pipeline mode must be used. Note that new data will also be clocked into both A1 and B1 during this 4-level shift operation.

The P29FCT520T and P29FCT521T are available in standard 24-pin 300 mil DIP, SOIC, and 28-pad square LCC package.

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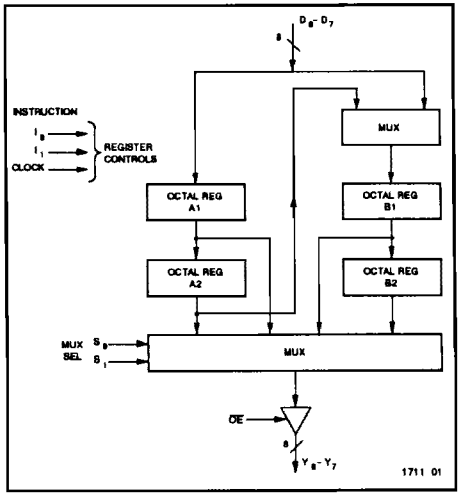
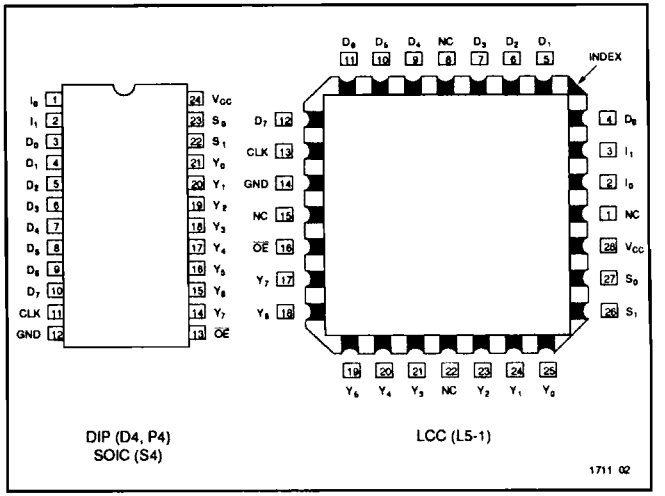
LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, Outputs Open, f_1 = 0, V_{IN} = 3.4V
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

OUTPUT SELECTION MUX TABLE

S_1	S_0	Output
1	1	A1
1	0	A2
0	1	B1
0	0	B2

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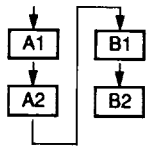
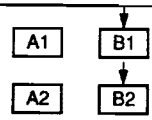
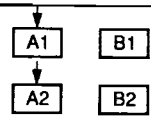
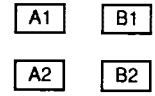
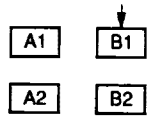
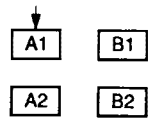
PIPELINE INSTRUCTION TABLE

	I = 0	I = 1	I = 2	I = 3
	$I_1 = 0$, $I_0 = 0$	$I_1 = 0$, $I_0 = 1$	$I_1 = 1$, $I_0 = 0$	$I_1 = 1$, $I_0 = 1$
P29FCT520T				
P29FCT521T				
	Single 4-level	Dual 2-level		Hold

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AC CHARACTERISTICS (P29FCT520AT/521AT)

Symbol	Parameter	P29FCT520AT/521AT				Units	Fig. No.
		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Clock to Data Output	2.0	16.0	2.0	14.0	ns	5
t_{PLH} t_{PHL}	S0, S1 To Data Output	2.0	15.0	2.0	13.0	ns	5
t_S	Setup Time Input Data to Clock	6.0	—	5.0	—	ns	
t_H	Hold Time Input Data to Clock	2.0	—	2.0	—	ns	
t_S	Setup Time Instruction (Reg. Enable) to Clock	6.0	—	5.0	—	ns	
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0	—	2.0	—	ns	
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	13.0	1.5	12.0	ns	8, 7
t_{PZH} t_{PZL}	Output Enable Time	1.5	16.0	1.5	15.0	ns	8, 7
t_W (H) t_W (L)	Clock Pulse Width, High or Low	8.0	—	7.0	—	ns	5

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AC CHARACTERISTICS (P29FCT520BT/521BT—P29FCT520CT/521CT)

Symbol	Parameter	P29FCT520BT/521BT				P29FCT520CT/521CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Clock to Data Output	2.0	8.0	2.0	7.5	2.0	7.0	2.0	6.0	ns	5
t_{PLH} t_{PHL}	S0, S1 To Data Output	2.0	8.0	2.0	7.5	2.0	7.0	2.0	6.0	ns	5
t_S	Setup Time Input Data to Clock	2.8	—	2.5	—	2.8	—	2.5	—	ns	
t_H	Hold Time Input Data to Clock	2.0	—	2.0	—	2.0	—	2.0	—	ns	
t_S	Setup Time Instruction (Reg. Enable) to Clock	4.5	—	4.0	—	4.5	—	4.0	—	ns	
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0	—	2.0	—	2.0	—	2.0	—	ns	
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	6.0	1.5	6.0	ns	8, 7
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.0	1.5	7.5	1.5	7.0	1.5	6.0	ns	8, 7
t_W (H) t_W (L)	Clock Pulse Width, High or Low	6.0	—	5.5	—	6.0	—	5.5	—	ns	5

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Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

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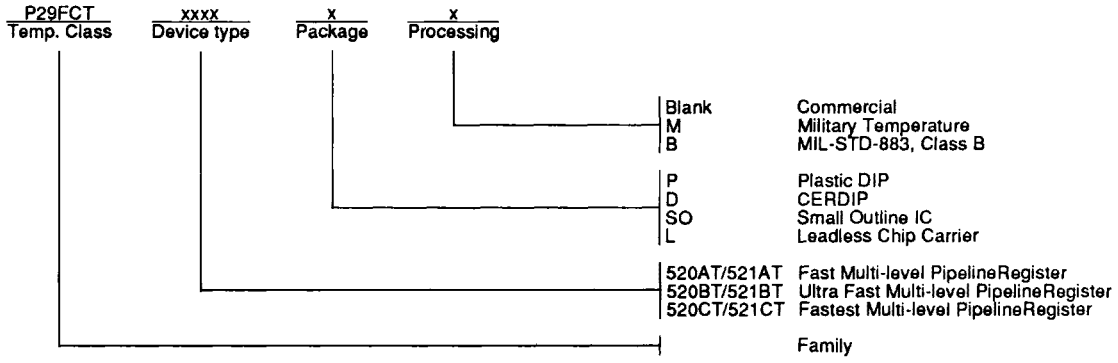
ORDERING INFORMATION



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