



SPECIFICATION

General Description

The EM39LV800 is an 8M bits Flash memory organized as 512K x 16 bits. The EM39LV800 uses 2.7-3.6V power supply for Program and Erase. Featuring high performance Flash memory technology, the EM39LV800 provides a typical Word-Program time of 14 μ sec and a typical Sector/Block-Erase time of 18 ms. The device uses Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent write, the device has on-chip hardware and software data protection schemes. The device offers typical 100,000 cycles endurance and a greater than 10 years data retention. The EM39LV800 conforms with the JEDEC standard pin outs for x16 memories. The EM39LV800 is offered in package types of 48-ball FBGA, 48-pin TSOP, and known good dice (KGD). For KGD, please contact ELAN Microelectronics or its representatives for detailed information (see Appendix at the bottom of this specification for Ordering Information).

The EM39LV800 devices are developed for applications that require memories with convenient and economical updating of program, data or configuration, e.g., DVD player, DVD R/W, WLAN, Router, Set-Top Box, etc.

Features

- **Single Power Supply**
Full voltage range from 2.7 to 3.6 volts for both read and write operations
- **Sector-Erase Capability**
Uniform 2Kword sectors
- **Block-Erase Capability**
Uniform 32Kword blocks
- **Read Access Time**
Access time: 55, 70 and 90 ns
- **Power Consumption**
Active current: 20 mA (Typical)
Standby current: 2 μ A (Typical)
- **Erase/Program Features**
Sector-Erase Time: 18 ms (Typical)
Block-Erase Time: 18 ms (Typical)
Chip-Erase Time: 45 ms (Typical)
Word-Program Time: 14 μ s (Typical)
Chip Rewrite Time: 8 seconds (Typical)
- **Automatic Write Timing**
Internal V_{PP} Generation
- **End-of-Program or End-of-Erase Detection**
Data# Polling
Toggle Bit
- **CMOS I/O Compatibility**
- **JEDEC Standard**
Pin-out and software command sets compatible with single-power supply Flash memory
- **High Reliability**
Endurance cycles: 100K (Typical)
Data retention: 10 years
- **Package Option**
48-pin TSOP
48-pin FBGA



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Functional Block Diagram

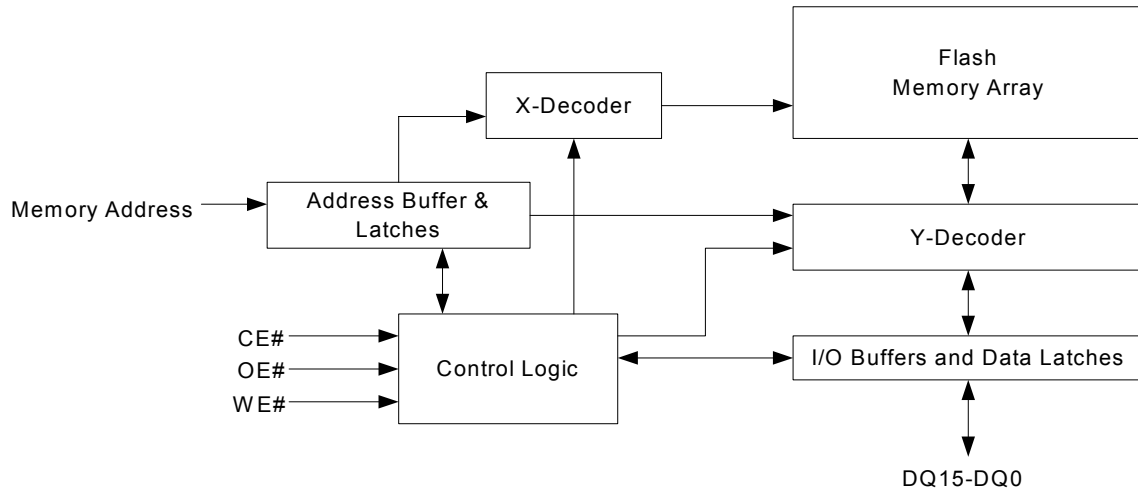


Figure 0a: Functional Block Diagram

Pin Assignments

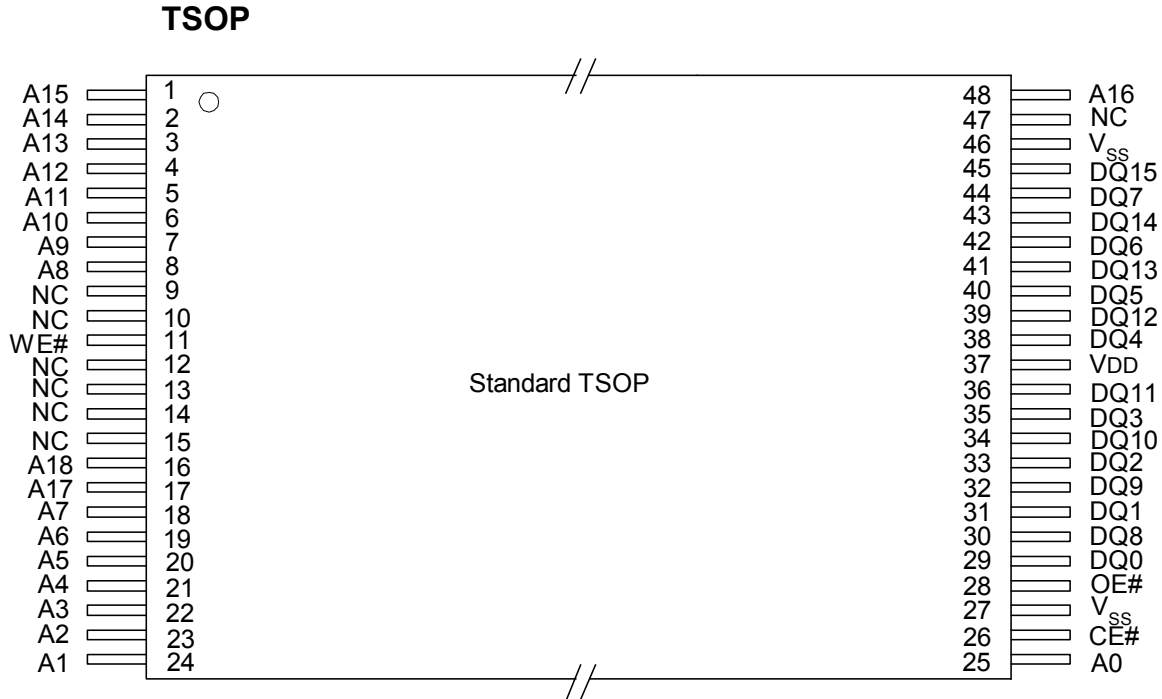


Figure 0b: TSOP Pin Assignments

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FBGA

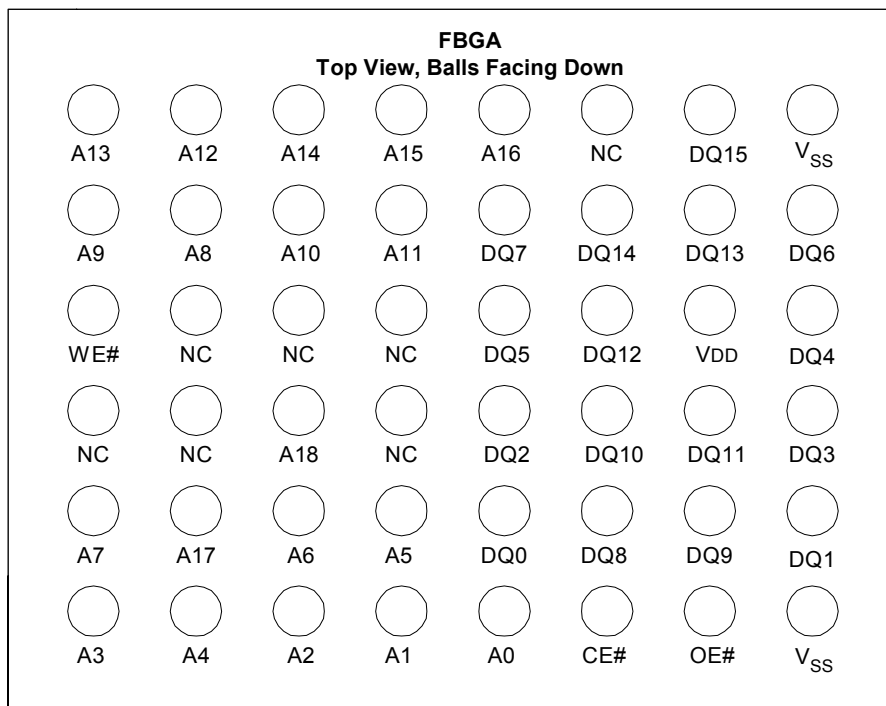


Figure 0c: FBGA Pin Assignments

Pin Description

| Pin Name | Function |
|----------|------------------------------------|
| A0–A18 | 19 addresses |
| DQ15–DQ0 | Data inputs/outputs |
| CE# | Chip enable |
| OE# | Output enable |
| WE# | Write enable |
| VDD | 2.7 ~ 3.6 volt single power supply |
| VSS | Device ground |
| NC | Pin not connected internally |

Table 1: Pin Description



Device Operation

The EM39LV800 uses Commands to initiate the memory operation functions. The Commands are written to the device by asserting WE# Low while keeping CE# Low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the EM39LV800 is controlled by CE# and OE#. Both have to be Low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read Cycle Timing Diagram in Figure 1 for further details.

Word Program

The EM39LV800 is programmed on a word-by-word basis. Before programming, the sector where the word is located must be erased completely. The Program operation is accomplished in three steps:

- The first step is a three-byte load sequence for Software Data Protection.
- The second step is to load word address and word data. During the Word Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last; and the data is latched on the rising edge of either CE# or WE#, whichever occurs first.
- The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 μ s. See Figures 2 and 3 for WE# and CE# controlled Program operation timing diagrams respectively and Figure 15 for flowchart.

During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any command issued during the internal Program operation is ignored.



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EM39LV800 Device Operation

| Operation | CE# | OE# | WE# | DQ | Address |
|------------------------|-----------------|-----------------|-----------------|-------------------------|---|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} | A _{IN} |
| Program | V _{IL} | V _{IH} | V _{IL} | D _{IN} | A _{IN} |
| Erase | V _{IL} | V _{IH} | V _{IL} | X* | Sector or Block address, XXH for Chip-Erase |
| Standby | V _{IH} | X | X | High Z | X |
| Write Inhibit | X | V _{IL} | X | High Z/D _{OUT} | X |
| Write Inhibit | X | X | V _{IH} | High Z/D _{OUT} | X |
| Software Mode | V _{IL} | V _{IL} | V _{IH} | | See Table 3 |
| Product Identification | | | | | |

*X can be V_{IL} or V_{IH}, but no other value.

Table 2: EM39LV800 Device Operation

Write Command/Command Sequence

The EM39LV800 provides two software methods to detect the completion of a Program or Erase cycle in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the write operation is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent such spurious rejection, when an erroneous result occurs, the software routine should include an additional two times loop to read the accessed location. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Chip Erase

The EM39LV800 provides Chip-Erase feature, which allows the entire memory array to be erased to logic "1" state. The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid reads are Toggle Bit and Data# Polling. See Table 3 for the command sequence, Figure 6 for timing diagram, and Figure 17 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.



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Sector/Block Erase

The EM39LV800 offers both Sector-Erase and Block-Erase modes. The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The sector architecture is based on uniform sector size of 2 KWord. The Block architecture is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined by using either Data# Polling or Toggle Bit method. See Figures 7 and 8 for timing waveforms. Any commands issued during the Sector or Block Erase operation are ignored.

Data# Polling (DQ7)

When the EM39LV800 is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce the true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Program operation, the remaining data outputs may still be invalid (valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 μ s). During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase, Block-Erase, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 4 for Data# Polling timing diagram and Figure 14 for a flowchart.

Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase, Block-Erase or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 5 for Toggle Bit timing diagram and Figure 14 for a flowchart.

Data Protection

The EM39LV800 provides both hardware and software features to protect the data from inadvertent write.



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Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# Low, CE# High, or WE# High will inhibit the Write operation. This prevents inadvertent write during power-up or power-down.

Software Data Protection (SDP)

The EM39LV800 provides the JEDEC approved Software Data Protection (SDP) scheme for Program and Erase operations. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, especially during the system power-up or power-down transition. Any Erase operation requires the inclusion of six-byte sequence. See Table 3 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Common Flash Memory Interface (CFI)

The EM39LV800 contains the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as Software ID Entry command, with 98H (CFI Query command) to address 5555H in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 4 through 6. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.



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Software Command Sequence

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---------------------|-------------------|---------------------|-------------------|---------------------|-------------------|---------------------|-------------------|---------------------|-------------------|------------------------------|-------------------|
| | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² |
| Word Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | WA ³ | Data | | | | |
| Sector Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | SA _X ⁴ | 30H |
| Block Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | BA _X ⁴ | 50H |
| Chip Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Software ID Entry ^{5,6} | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0000H | 0007F | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0003H | 0007F | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0040H | 0001F | | | | |
| Device ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0001H | 0020H | | | | |
| CFI Query Entry ⁵ | 5555H | AAH | 2AAAH | 55H | 5555H | 98H | | | | | | |
| Software ID Exit ⁷ /CFI Exit | XXH | F0H | | | | | | | | | | |
| Software ID Exit ⁷ /CFI Exit | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | | | | | | |

Notes:

1. Address format A14-A0 (Hex), Addresses A18-A15 can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
3. WA = Program word address.
4. SA_X for Sector-Erase; uses A18-A11 address lines.
BA_X for Block-Erase; uses A18-A15 address lines.
5. The device does not remain in Software Product ID mode if powered down.
6. Both Software ID Exit operations are equivalent.
7. Refer to Figure 9 for more information.

Table 3: Software Command Sequence



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CFI Query Identification String*

| Address | Data | Data |
|---------|-------|--|
| 10H | 0051H | Query Unique ASCII string "QRY" |
| 11H | 0052H | |
| 12H | 0059H | |
| 13H | 0001H | Primary OEM command set |
| 14H | 0007H | |
| 15H | 0000H | Address for Primary Extend Table |
| 16H | 0000H | |
| 17H | 0000H | Alternate OEM command set (00H=none exists) |
| 18H | 0000H | |
| 19H | 0000H | Address for Alternate OEM extended Table (00H=none exists) |
| 1AH | 0000H | |

* Refer to CFI publication 100 for more details.

Table 4: CFI Query Identification String1

System Interface

| Address | Data | Data |
|---------|-------|--|
| 1BH | 0027H | V _{DD} Min (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts |
| 1CH | 0036H | V _{DD} Max (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts |
| 1DH | 0000H | V _{PP} min (00H=no V _{PP} pin) |
| 1EH | 0000H | V _{PP} max (00H=no V _{PP} pin) |
| 1FH | 0004H | Typical time out for Word-Program 2 ^N μs (2 ⁴ =16μs) |
| 20H | 0000H | Typical time out for min size buffer program 2 ^N μs (00H=not supported) |
| 21H | 0004H | Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ =16ms) |
| 22H | 0006H | Typical time out for Chip-Erase 2 ^N ms (2 ⁶ =64ms) |
| 23H | 0001H | Maximum time out for Word-Program 2 ^N times typical (2 ¹ x2 ⁴ =32μs) |
| 24H | 0000H | Maximum time out for buffer Program 2 ^N times typical |
| 25H | 0001H | Maximum time out for individual Sector/Block-Erase 2 ^N times typical (2 ¹ x2 ⁴ =32ms) |
| 26H | 0001H | Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x2 ⁶ =128ms) |

Table 5: System Interface



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Device Geometry Information

| Address | Data | Data |
|--------------------------|----------------------------------|--|
| 27H | 0014H | Device size=2 ^N Byte (14H=20; 2 ²⁰ =1MByte) |
| 28H 29H | 0001H 0000H | Flash Device Interface description; 0001H=x16-only asynchronous interface |
| 2AH 2BH | 0000H 0000H | Maximum number of byte in multi-byte write=2 ^N (00H=not supported) |
| 2CH | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH 2EH 2FH 30H | 00FFH 0000H 0010H 0000H | Sector Information (y+1=Number of sectors; z x 256B=sector size) y=255+1=256 sectors (00FFH=255) z=16 x 256 Bytes=4Kbyte/sector (0010H=16) |
| 31H 32H 33H 34H | 000FH 0000H 0000H 0001H | Block Information (y+1=Number of blocks; z x 256B=block size) y=15+1=16 blocks (000FH=15) z=256 x 256 Bytes=64 Kbyte/block (0100H=256) |

Table 6: Device Geometry Information

Absolute Maximum Ratings

NOTE

Applied conditions greater than those listed under these ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this specification, are not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

- Temperature Under Bias -55°C to 125°C
- Storage Temperature -65°C to 150°C
- D.C. Voltage on Any Pin to Ground Potential -0.5 V to V_{DD}+0.5V
- Transient Voltage (<20ns) on Any Pin to Ground Potential -2.0V to V_{DD} +2.0V
- Voltage on A9 Pin to Ground Potential -0.5 V to 13.2V
- Package Power Dissipation Capability (Ta=25°C)..... 1.0W
- Surface Mount Lead Soldering Temperature (3 Seconds)..... 240°C
- Output Short Circuit Current * 50mA

* Output shorted for no more than one second.
No more than one output shorted at a time.



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Operating Range

| Model Name | Ambient Temperature | V _{DD} |
|------------|---------------------|-----------------|
| EM39LV800 | 0°C to +70°C | 2.7~3.6V |

Table 7: Operating Range

AC Conditions of Test

Input Rise/Fall Time 5ns
 Output Load CL=30pF for 55Rns
 Output Load CL=100pF for 70ns/90ns
 See Figures 14 and 15

DC CHARACTERISTICS (CMOS Compatible)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|------------------|---------------------------------|--|----------------------|-----|------|
| I _{DD} | Power Supply Current | Address Input =V _{IL} /V _{IH} , at f=1/T _{RC} Min, V _{DD} =V _{DD} Max | | | |
| | Read | CE#=OE#=V _{IL} , WE#=V _{IH} , all I/Os open | | 30 | mA |
| | Program and Erase | CE#=WE#=V _{IL} , OE#=V _{IH} , | | 30 | mA |
| I _{SB} | Standby V _{DD} Current | CE#=V _{IHC} , V _{DD} =V _{DD} Max | | 20 | μA |
| I _{LI} | Input Leakage Current | V _{IN} =GND to V _{DD} , V _{DD} =V _{DD} Max | | 1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} =GND to V _{DD} , V _{DD} =V _{DD} Max | | 10 | μA |
| V _{IL} | Input Low Voltage | V _{DD} =V _{DD} Min | | 0.8 | V |
| V _{IH} | Input High Voltage | V _{DD} =V _{DD} Max | 0.7 V _{DD} | | V |
| V _{IHC} | Input High Voltage (CMOS) | V _{DD} =V _{DD} Max | V _{DD} -0.3 | | V |
| V _{OL} | Output Low Voltage | I _{OL} =100μA, V _{DD} =V _{DD} Min | | 0.2 | V |
| V _{OH} | Output High Voltage | I _{OH} =-100μA, V _{DD} =V _{DD} Min | V _{DD} -0.2 | | V |

Table 8: DC Characteristics (Cmos Compatible)

Recommended System Power-up Timing

| Parameter | Description | Min | Unit |
|-------------------------|-------------------------------------|-----|------|
| T _{PU-READ} * | Power-up to Read Operation | 100 | μs |
| T _{PU-WRITE} * | Power-up to Program/Erase Operation | 100 | μs |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 9: Recommended System Power-up Timing

**SPECIFICATION****Capacitance (Ta=25°C, f=1Mhz, other pins open)**

| Parameter | Description | Test Conditons | Max |
|--------------------|---------------------|----------------------|------|
| C _{I/O} * | I/O Pin Capacitance | V _{I/O} =0V | 12pF |
| C _{IN} * | Input Capacitance | V _{IN} =0V | 6pF |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Capacitance (Ta=25°C, f=1Mhz, Other Pins Open)

Reliability Characteristics

| Symbol | Parameter | Min Specification | Unit | Test Method |
|--------------------|----------------|---------------------|--------|---------------------|
| N _{END} * | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T _{DR} * | Data Retention | 10 | Years | JEDEC Standard A103 |
| I _{LTH} * | Latch Up | 100+I _{DD} | mA | JEDEC Standard 78 |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 11: Reliability Characteristics

AC Characteristics**Read Cycle Timing Parameters**

| Symbol | Parameter | 55REC | | 70REC | | 90REC | | Unit |
|--------------------|---------------------------------|-------|-----|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| T _{RC} | Read Cycle Time | 55 | | 70 | | 90 | | ns |
| T _{CE} | Chip Enable Access Time | | 55 | | 70 | | 90 | ns |
| T _{AA} | Address Access Time | | 55 | | 70 | | 90 | ns |
| T _{OE} | Output Enable Access Time | | 30 | | 35 | | 45 | ns |
| T _{CLZ} * | CE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| T _{OLZ} * | OE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| T _{CHZ} * | CE# High to High-Z Output | | 15 | | 20 | | 30 | ns |
| T _{OHZ} * | OE# High to High-Z Output | | 15 | | 20 | | 30 | ns |
| T _{OH} * | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 12a: Read Cycle Timing Parameters



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| Symbol | Parameter | 55EC | | 70EC | | 90EC | | Unit |
|--------------------|---------------------------------|------|-----|------|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| T _{RC} | Read Cycle Time | 55 | | 70 | | 90 | | ns |
| T _{CE} | Chip Enable Access Time | | 55 | | 70 | | 90 | ns |
| T _{AA} | Address Access Time | | 55 | | 70 | | 90 | ns |
| T _{OE} | Output Enable Access Time | | 30 | | 35 | | 45 | ns |
| T _{CLZ} * | CE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| T _{OLZ} * | OE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| T _{CHZ} * | CE# High to High-Z Output | | 15 | | 20 | | 30 | ns |
| T _{OHZ} * | OE# High to High-Z Output | | 15 | | 20 | | 30 | ns |
| T _{OH} * | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 12b: Read Cycle Timing Parameters

Program/Erase Cycle Timing Parameter

| Symbol | Parameter | Min | Max | Unit |
|--------------------|----------------------------------|-----|-----|------|
| T _{BP} | Word-Program Time | | 20 | μs |
| T _{AS} | Address Setup Time | 0 | | ns |
| T _{AH} | Address Hold Time | 30 | | ns |
| T _{CS} | WE# and CE# Setup Time | 0 | | ns |
| T _{CH} | WE# and CE# Hold Time | 0 | | ns |
| T _{OES} | OE# High Setup Time | 0 | | ns |
| T _{OEH} | OE# High Hold Time | 10 | | ns |
| T _{CP} | CE# Pulse Width | 45 | | ns |
| T _{WP} | WE# Pulse Width | 45 | | ns |
| T _{WPH} * | WE# Pulse Width High | 30 | | ns |
| T _{CPH} * | CE# Pulse Width High | 30 | | ns |
| T _{DS} | Data Setup Time | 45 | | ns |
| T _{DH} * | Data Hold Time | 0 | | ns |
| T _{IDA} * | Software ID Access and Exit Time | | 150 | ns |
| T _{SE} | Sector Erase | | 30 | ms |
| T _{BE} | Block Erase | | 30 | ms |
| T _{SCE} | Chip Erase | | 60 | ms |

* This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 13: Program/Erase Cycle Timing Parameter

Timing Diagrams

Read Cycle Timing Diagram

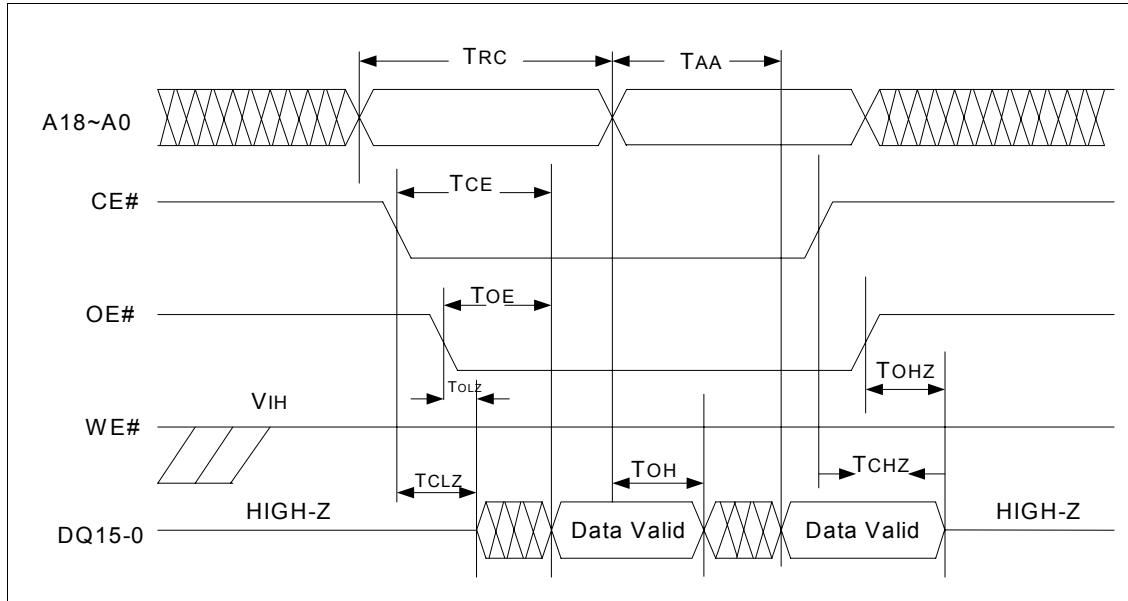


Figure 1: Read Cycle Timing Diagram

WE# Controlled Program Cycle Timing Diagram

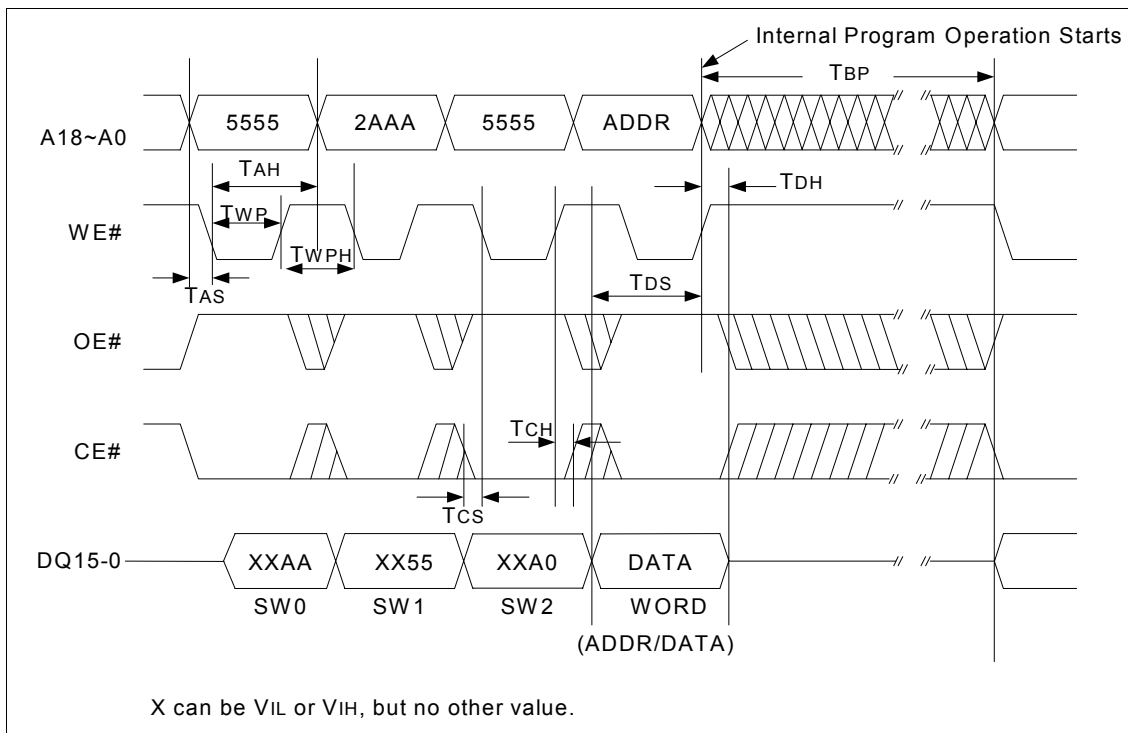


Figure 2: WE# Controlled Program Cycle Timing Diagram

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CE# Controlled Program Cycle Timing Diagram

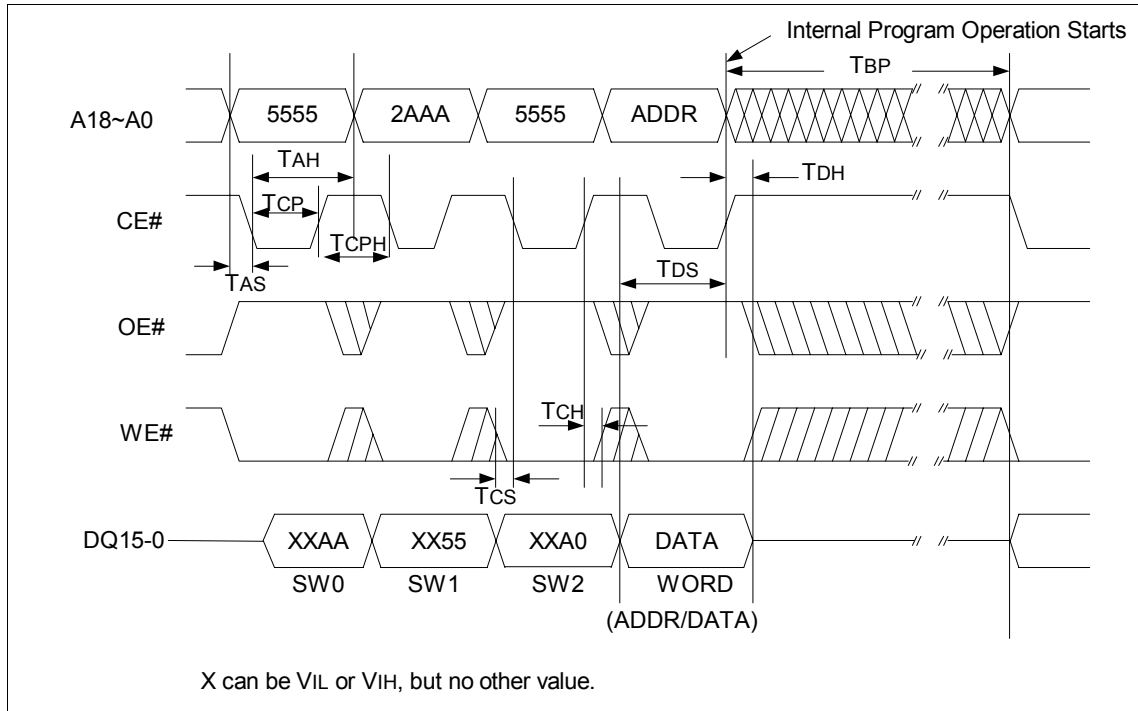


Figure 3: CE# Controlled Program Cycle Timing Diagram

Data# Polling Timing Diagram

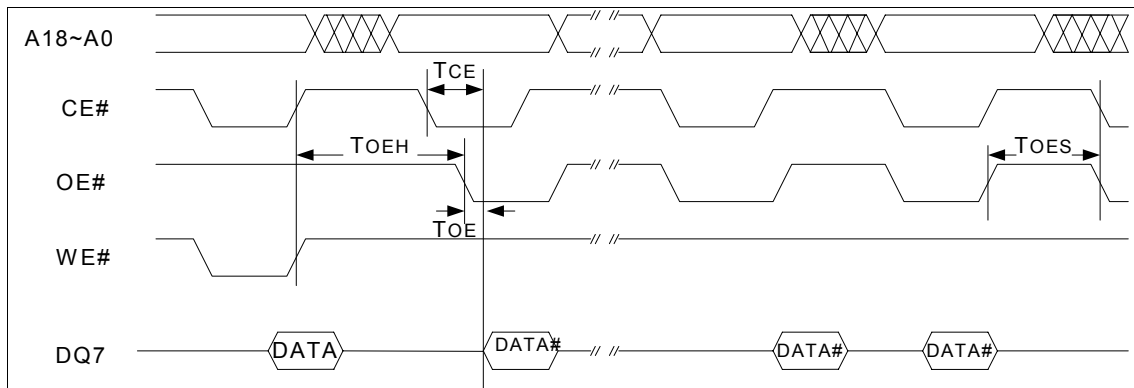


Figure 4: Data# Polling Timing Diagram

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Toggle Bit Timing Diagram

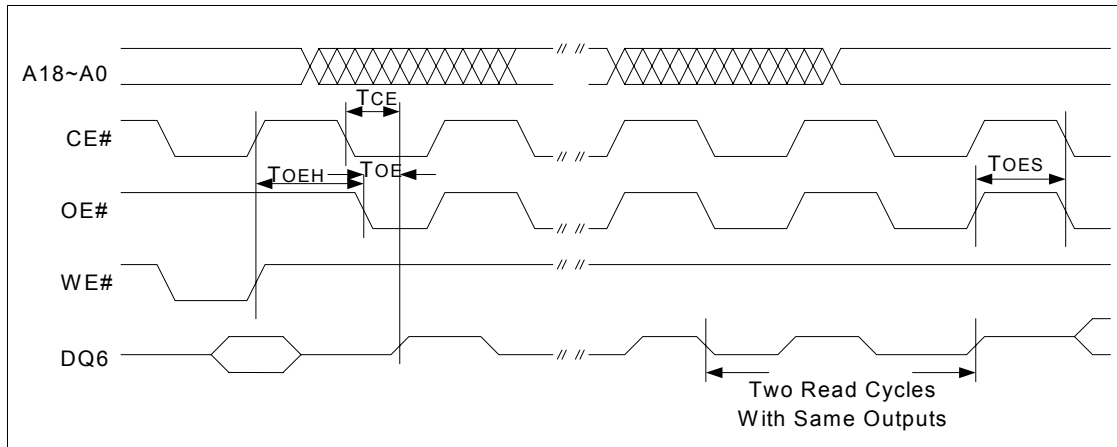


Figure 5: Toggle Bit Timing Diagram

WE# Controlled Chip-Erase Timing Diagram

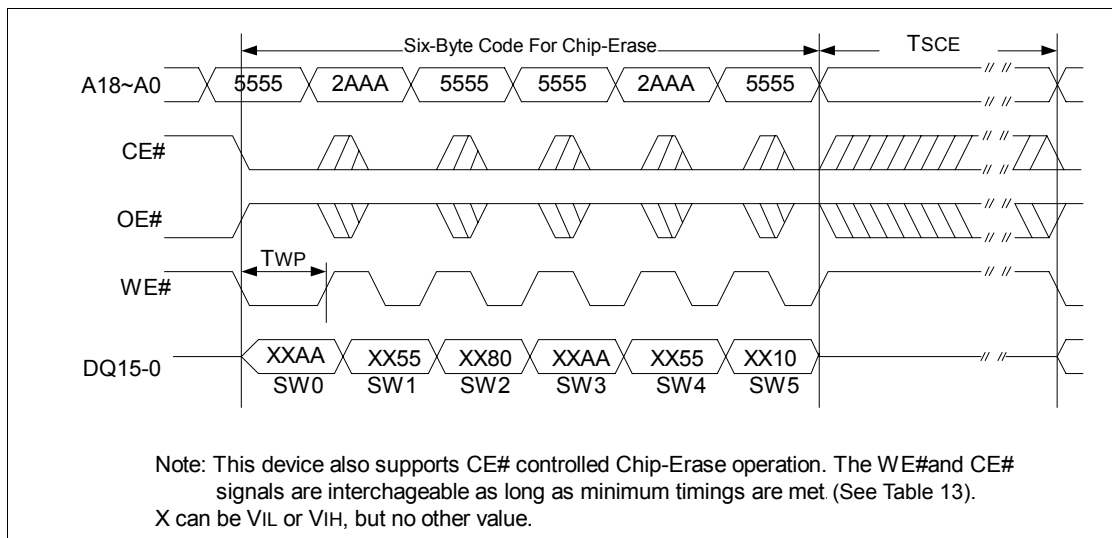


Figure 6: WE# Controlled Chip-Erase Timing Diagram



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WE# Controlled Block-Erase Timing Diagram

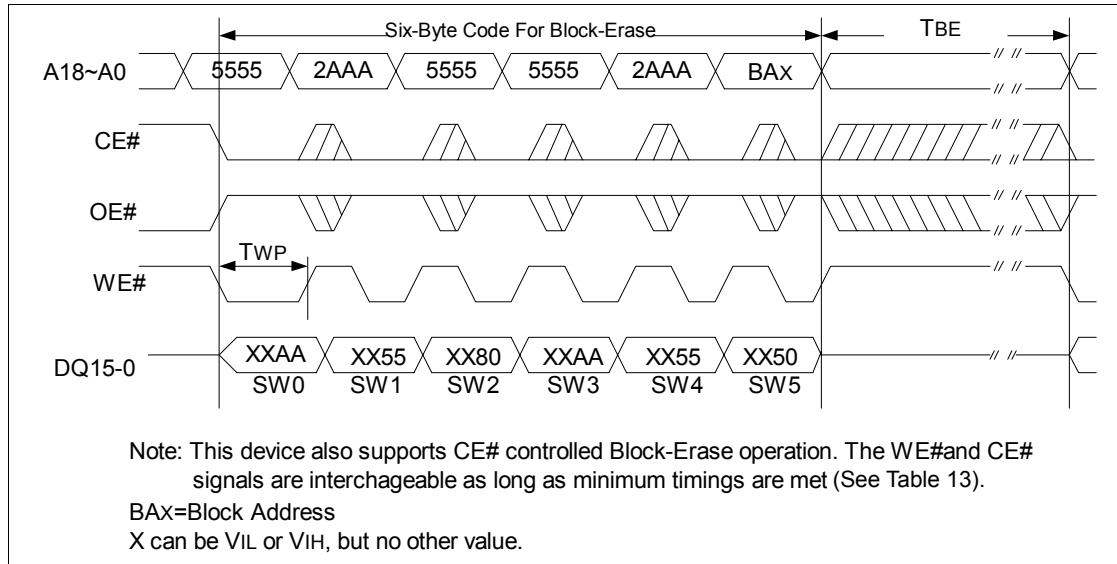


Figure 7: WE# Controlled Block-Erase Timing Diagram

WE# Controlled Sector-Erase Timing Diagram

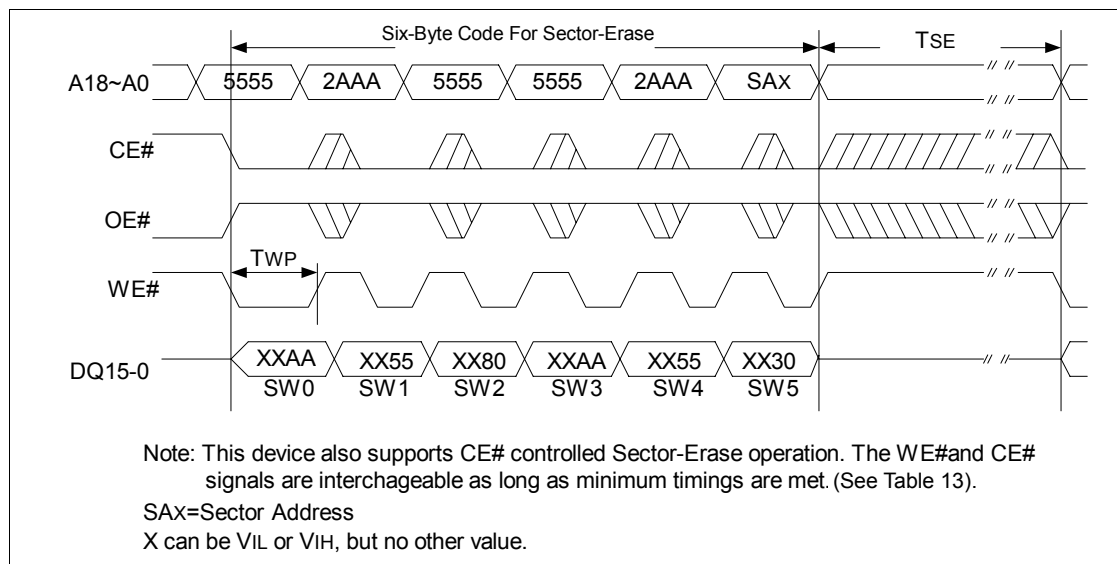


Figure 8: WE# Controlled Sector-Erase Timing Diagram

SPECIFICATION

Software ID Entry and Read

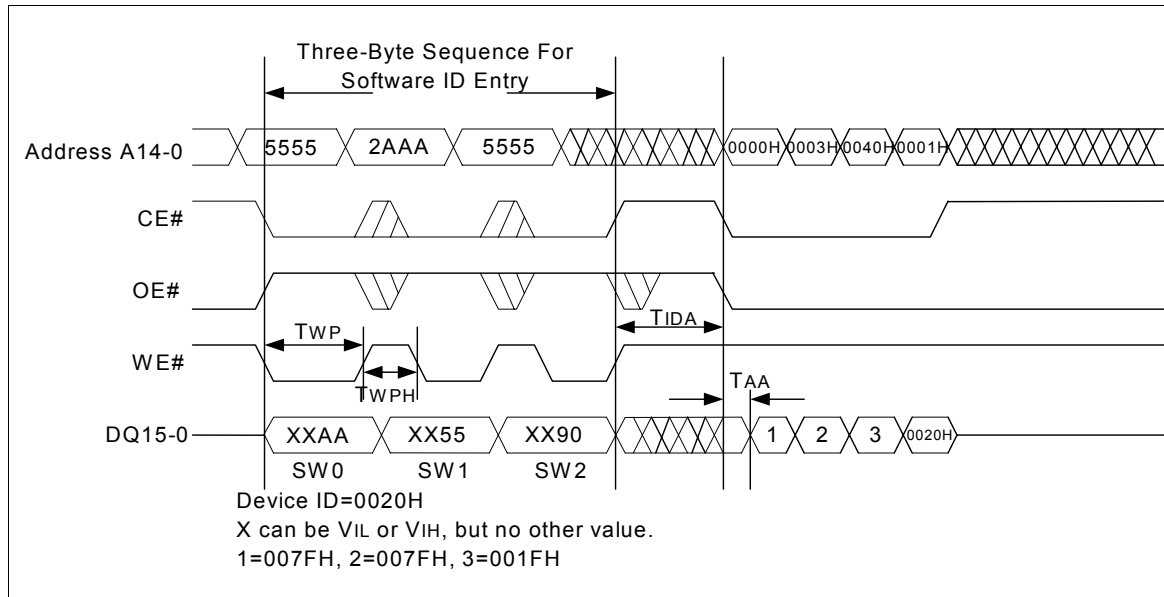


Figure 9: Software ID Entry and Read

CFI Query Entry and Read

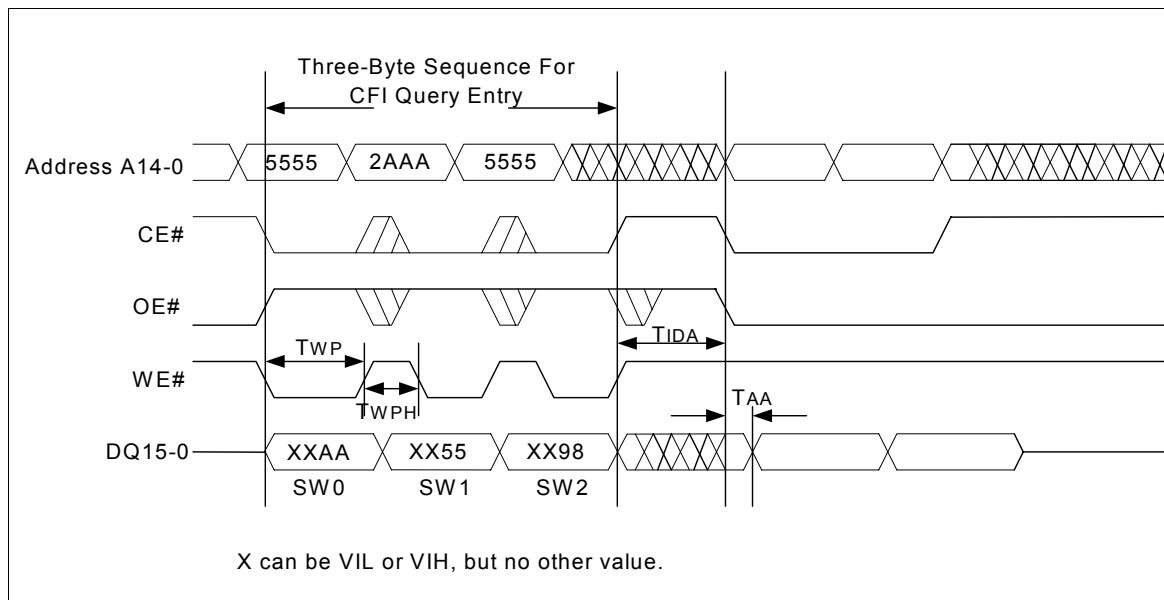


Figure 10: CFI Query Entry and Read

Software ID Exit/CFI Exit

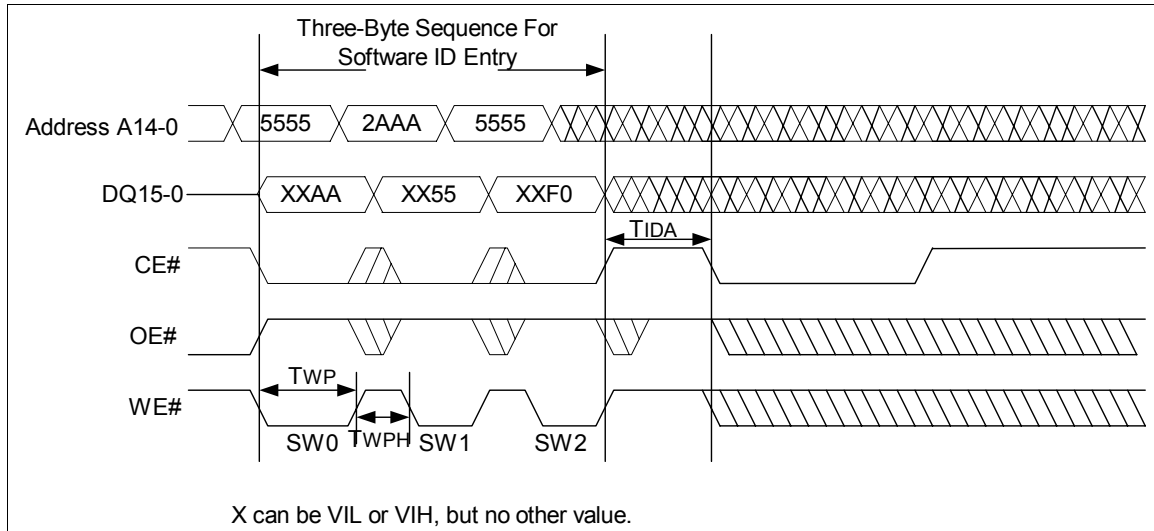


Figure 11: Software ID Exit/CFI Exit

AC Input/Output Reference Waveforms

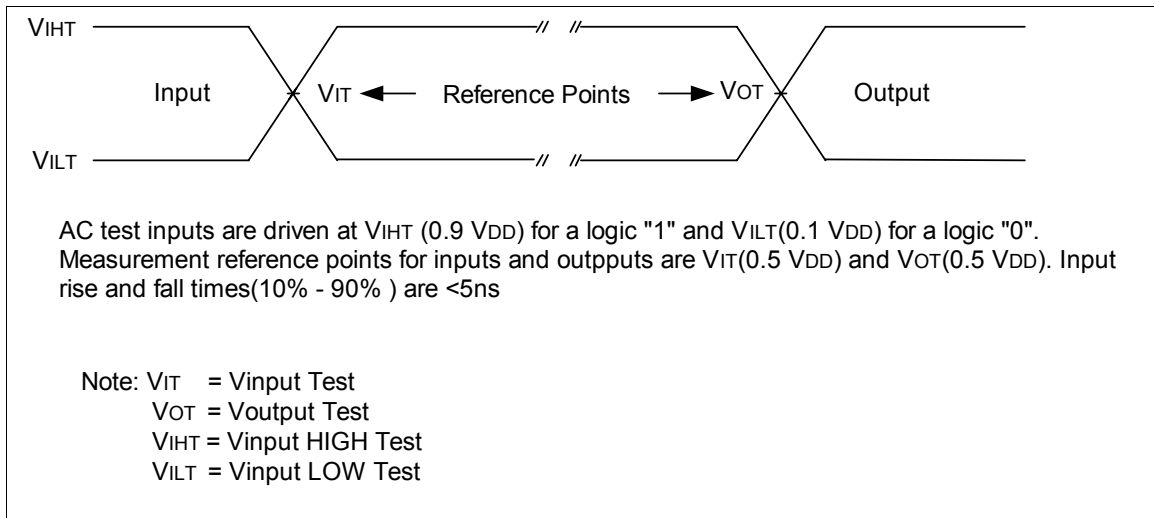


Figure 12: AC Input/Output Reference Waveforms

A Test Load Example

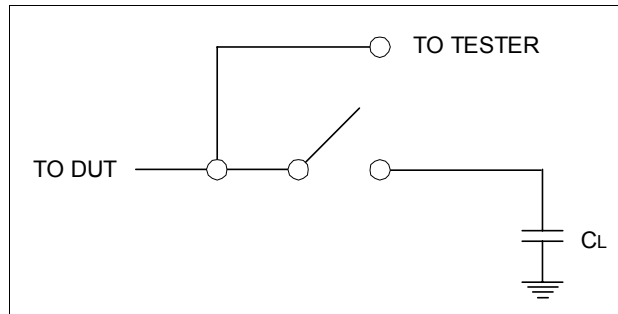


Figure 13: A Test Load Example

Flow Charts

Wait Options

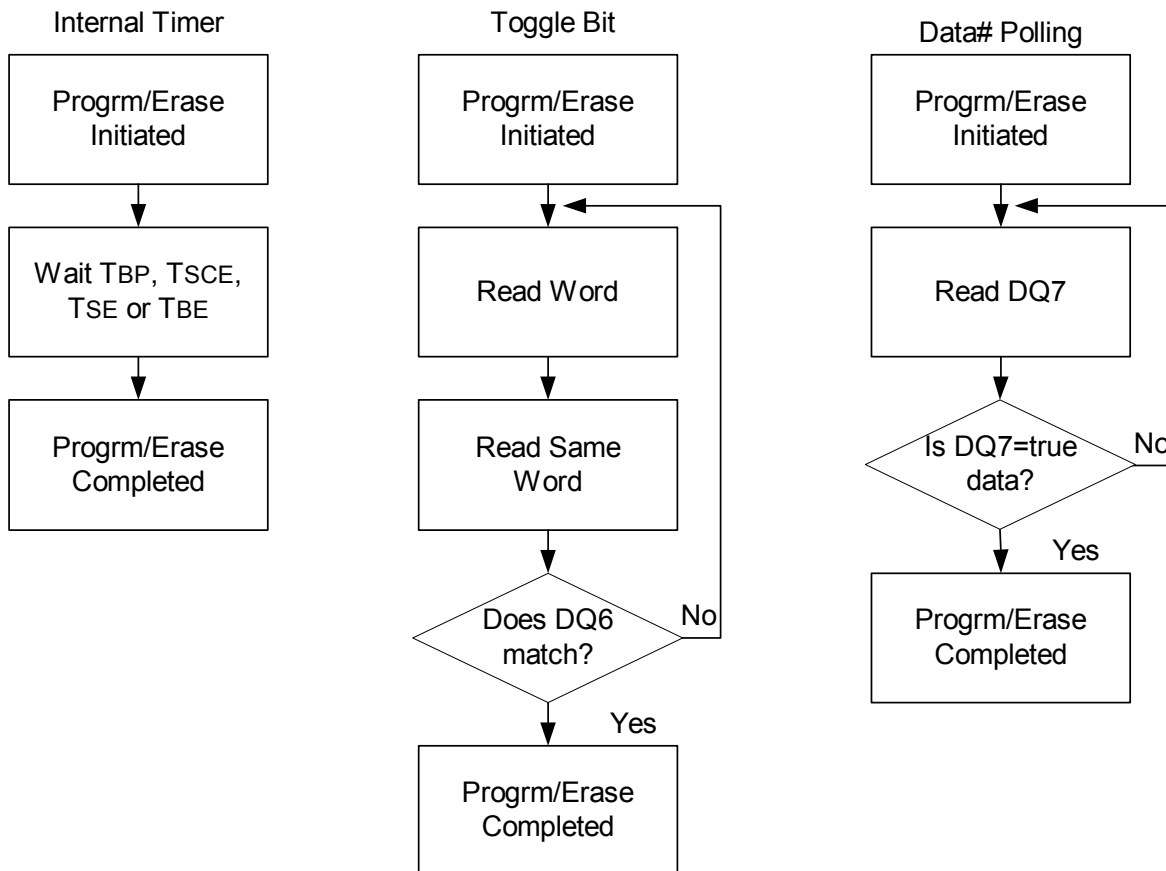
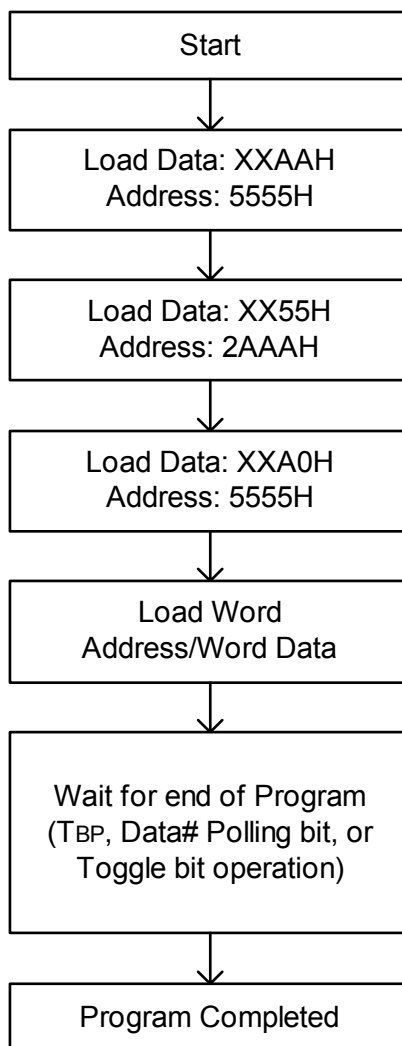


Figure 14: Wait Options

SPECIFICATION

Word-Program Algorithm



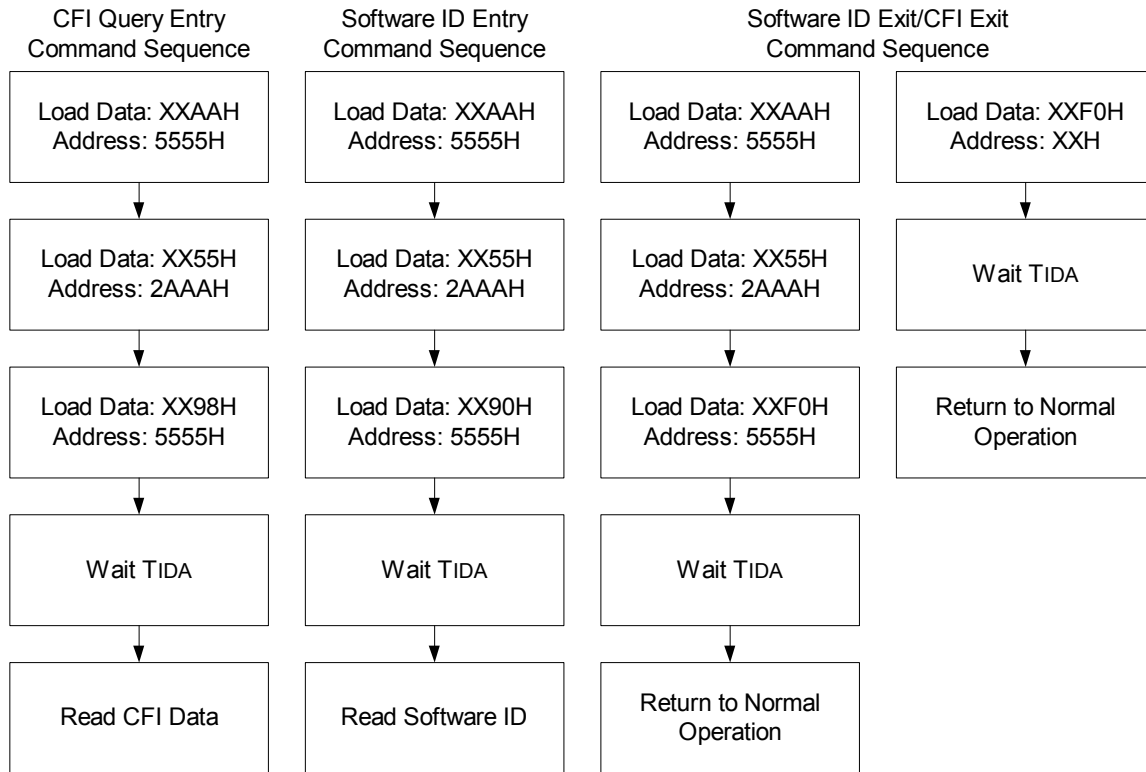
X can be VIL or VIH, but no other value.

Figure 15: Word-Program Algorithm



SPECIFICATION

Software ID/CFI Command Flowcharts



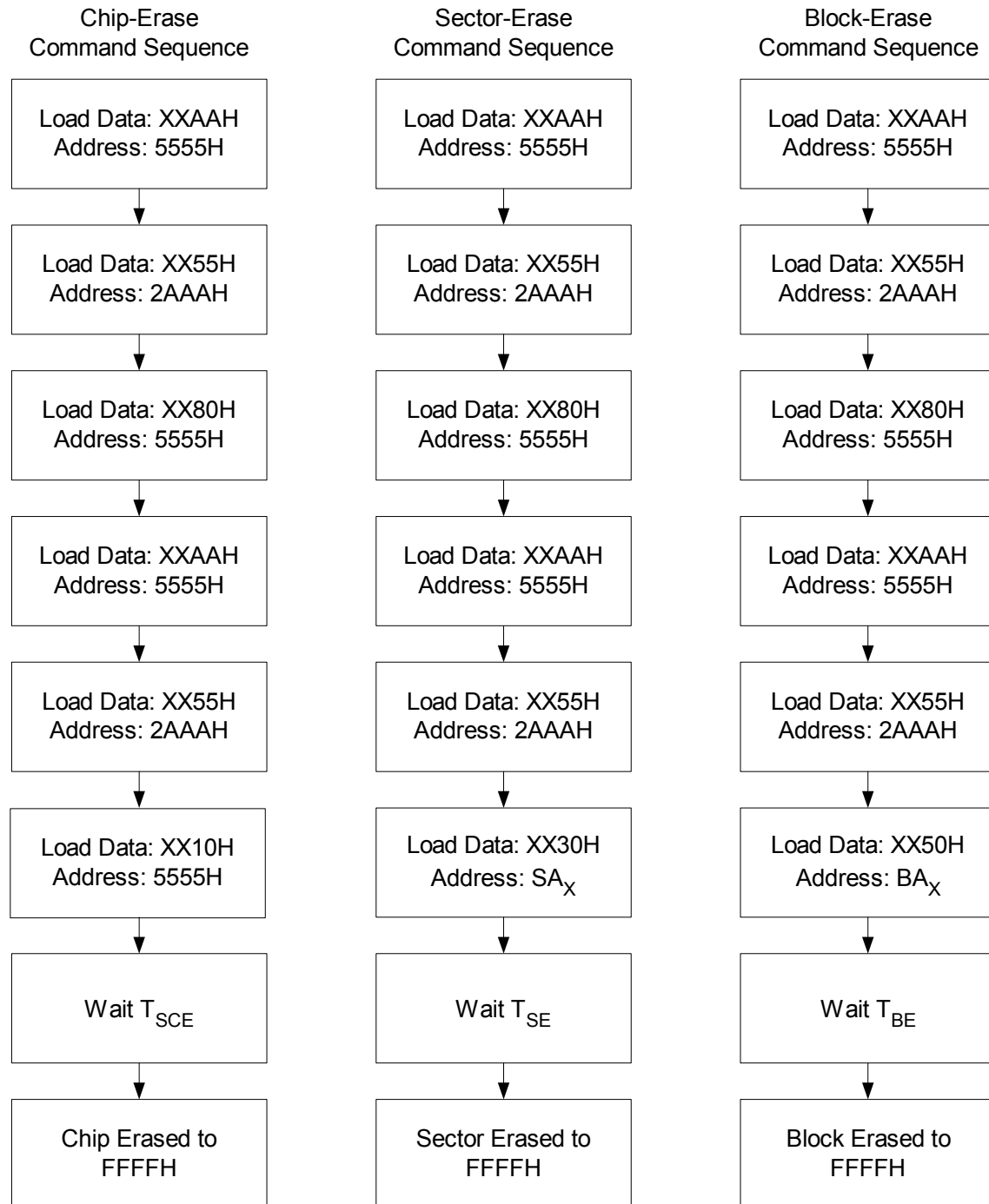
X can be VIL or VIH, but no other value.

Figure 16: Software ID/CFI Command Flowcharts



SPECIFICATION

Erase Command Sequence



X can be VIL or VIH, but no other value.

Figure 17: Erase Command Sequence

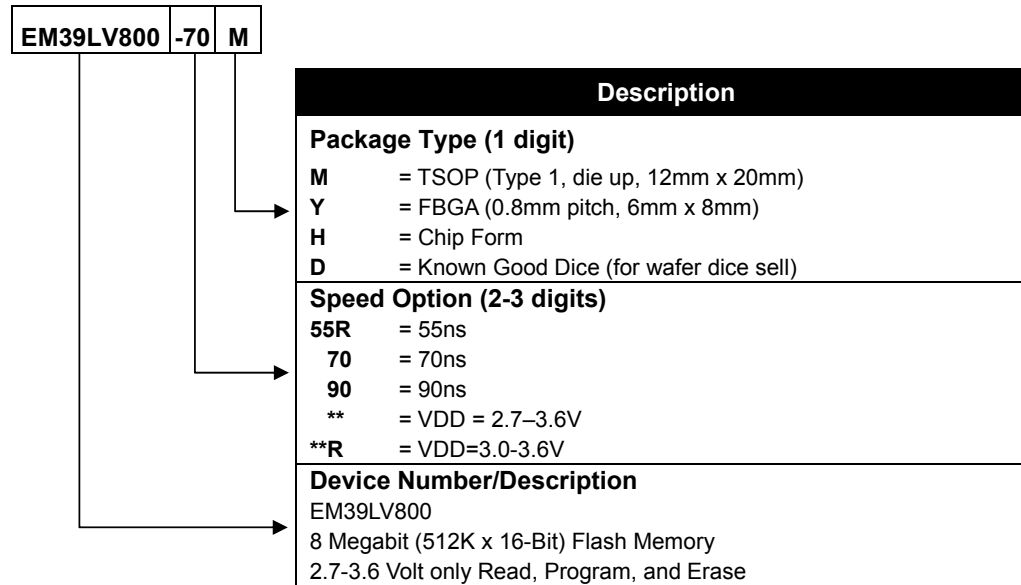


SPECIFICATION

Appendix

ORDERING INFORMATION (Standard Products)

The order number is defined by a combination of the following elements.





SPECIFICATION

ORDERING INFORMATION (Non-Standard Products)

For Know Good Dice (KGD), please contact ELAN Microelectronics at the following contact information or its representatives.

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Fax: +852 2723-7780
elanhk@emc.com.hk

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Fax: +86 021 5080-4600