Preliminary Product Information
November 1998 *(1 of 5)*

1.85 to 1.91 GHz 3.0V, 30 dBm, PCS/PCN Plastic SOIC-8 Power Amplifier

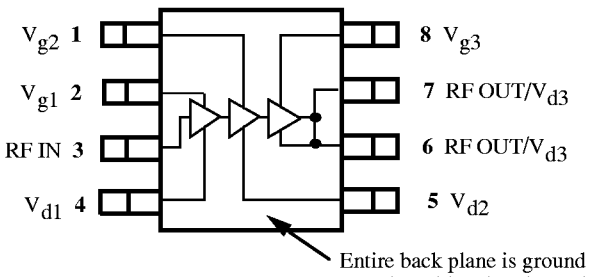
Features

- ❑ Operation as Low as 3.0V
- ❑ 38% Linear Power Added Efficiency
- ❑ +30 dBm Output Power (IS-136 TDMA Mode)
- ❑ +28.5 dBm Output Power (IS-98 CDMA Mode)
- ❑ 31 dB Gain at Operating Output
- ❑ Tested Under Digital Modulation
- ❑ New Low-Cost, Thermally Enhanced, SOIC-8 Plastic Package
- ❑ PHEMT Material Technology

Applications

- ❑ PCS Handsets
- ❑ PCS Base Stations
- ❑ Wireless Local Loop Subscriber Units
- ❑ CDMAone Handsets

Functional Block Diagram



Entire back plane is ground and must be soldered to thermally conductive ground plane.

Description

The CMM1530-RJ is a linear power amplifier intended for use in PCS handsets and wireless local loop subscriber units. The amplifier can be biased to meet the requirements of PCS-1900, IS-136 (TDMA), IS-98 (CDMA) or DCS-1800 systems. It is a member of Celeritek's new ***Triniti DX Pro***™ family of 3V power amplifier MMICs.

The CMM1530-RJ is packaged in a low-cost, space efficient, SOIC-8 plastic package that provides excellent electrical stability and low thermal resistance. The part requires minimal external circuitry for bias and matching to reduce space and cost.

This device is unconditionally stable under all source and load impedances.

Absolute Maximum Ratings

Parameter	Rating	Parameter	Rating	Parameter	Rating
Drain Voltage (+V_d)	+5.5 V*	Power Dissipation	5 W	Operating Temperature	-40°C to +90°C
Drain Current (I_d)	1.8 A	Thermal Resistance	20°C/W	Channel Temperature	150°C
RF Input Power	10 dBm*	Storage Temperature	-65°C to +150°C	Soldering Temperature	260°C for 5 Sec.
DC Gate Voltage (-V_g)	-3.0 V*				

* Max (+V_d) and (-V_g) under linear operation. Max potential difference across the device at 1dB gain compression point ($2V_d$ + |-V_g|) not to exceed the minimum breakdown voltage (V_{br}) of +12V.

Recommended Operating Conditions

Parameter	Typ	Units	Parameter	Typ	Units
Drain Voltage (+V_d)	3.0 to 4.2	Volts	Operating Temperature (PC Board)	-30 to +80	°C

Application Information

The CMM1530-RJ is a three stage amplifier that requires a positive and a negative supply voltages for proper operation. It is essential when turning on the device that the negative supply be applied before the positive supply. When turning the device off, the positive supply should be removed before the negative supply is removed.

The CMM1530-RJ can be operated over a range of supply voltages and bias points. It is important that the maximum power dissipation of the package be observed at all times and that the maximum voltage across the device is not exceeded.

Circuit Design Considerations

Biasing Negative gate voltages are necessary to set the bias currents of the three FET stages in the CMM1530-RJ. The first stage gate bias voltage is applied to Vg1 (Pin 2). The second stage gate bias voltage is applied to Vg2 (Pin 1), while the third stage FET gate bias is applied to Vg3 (Pin 8). It is desirable to use one or more DACs (digital to analog converters) along with appropriate divider networks, when necessary, in order to adjust the quiescent currents to within 10 mA of the target values. As an example, for CDMA applications the target quiescent current of the third FET is 90 mA, while those for the second and the first FETs are 35 and 15 mA, respectively. The total quiescent is 140 mA. It is also recommend that the quiescent currents be set in the following sequence: the third stage FET is set first, followed by the second stage FET, followed by the first stage FET. The negative supply voltages control the quiescent currents through each of the FETs and, therefore, control the output power, adjacent channel power ratios, and the currents at the full output power.

The positive supply voltages are applied to Pins 4, 5, 6 and 7.

– Continued on Page 2 –

Electrical Characteristics

Unless otherwise specified, the following specifications are guaranteed at room temperature with drain voltage ($+V_d$) = 3.5 V in Celeritek test fixture.

Parameter	Condition	Min	Typ	Max	Units
Frequency Range		1.85		1.91	GHz
Gain	@ Digital power output	28	31		dB
Gain Ripple*	1805-1880 MHz & 1850-1910 MHz			1.5	dB
Gain Variation	Over supply voltage		2		dB/V
	Over temperature		0.03		dB/°C
Power Output Control Range	Vdd = 0 V to +3.5 V		50		dB
Power Output	Meets IS-136 TDMA mask		+30.0		dBm
	Meets IS-98 CDMA mask		+28.5		dBm
Harmonics	2nd @ Digital power output, no output trapping, Po=+28.5 dBm		-30		dBc
	3rd @ Digital power output, no output trapping, Po=+28.5 dBm		-40		dBc
Noise Power in Receive Band	30 kHz bandwidth		-94		dBm
Linearity	CDMA modulation @ +28.5 dBm Pout, 1.25 MHz offset	-45			dBc/30KHz
	TDMA modulation @ +30 dBm Pout - Adjacent	-26			dBc
	TDMA modulation @ +30 dBm Pout - Alternate	-45			dBc
Spurious Signal	VSWR = 3:1 in-band, VSWR = 10:1 out-of-band			-80	dBc
Noise Figure			3.5		dB
Return Loss Input			10		dB
Return Loss Output			8		dB
Efficiency (Vdd = 3.0 V)	Pout = +30.0 dBm - TDMA	36	38		%
	Pout = +28.5 dBm - CDMA	32	34		%
Positive Supply Current (I_d)	Pout IS-136 TDMA		750		mA
	Pout IS-98 CDMA		595		mA
Quiescent Current (I_q)	No RF CDMA mode		140		mA
	No RF TDMA mode		200		mA
Negative Supply Current ($-I_g$)	Includes external resistor divider		1.1	2.0	mA
Negative Supply Voltage ($-V_g$)	Into external resistor divider	-0.5	-0.8	-1.4	V

* Specifications guaranteed over the temperature range of -20°C to +80°C

– Continued from Page 1 –

It is very important to provide adequate de-coupling between the RF and DC signals in designing the DC bias circuit. Inadequate by-pass capacitance around the DC supply lines and inductance can compromise the adjacent channel power ratio (ACPR), or reduce power gain and/or create oscillations. The recommend DC by-pass capacitance and low-pass in-line inductance are shown in the evaluation board on Page 4.

Matching Circuits Output matching and input matching circuits are required to achieve the RF specifications in this data sheet. The recommend matching circuits are identical to the matching circuits for the evaluation board shown on Page 4. For output power matching, one shunt capacitor along the transmission line connected to Pins 6 and 7 as well as the bond wire inside the package from the output leads to the output FET are used to transform 50Ω impedance to the load line resistance of the output FET. The placement and the value of the capacitor are important in achieving the performance desired. Matching circuits for the frequencies other than the one shown can be achieved by changing the capacitor value and the placement position of the capacitor. The device can be designed to work from UHF to around 3 GHz.

Supply Ramping To obtain power ramping, gate supply control is recommend. Drain supply voltage ramping can also be used.

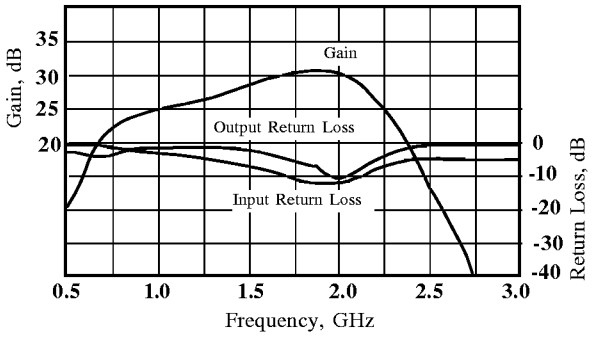
Modulation When biased as specified, the CMM1530-RJ will achieve the required adjacent channel response for the digital PCS system specified. Celeritek tests each product under digital modulation to ensure correlation to customer applications.

Thermal

1. The copper pad on the backside of the CMM1530-RJ must be soldered to the ground plane.
2. All 8 leads of the package must be soldered to the appropriate electrical connection.

Typical Performance

Wideband Gain & Return Loss vs Frequency @ 3.5 V, +25°C



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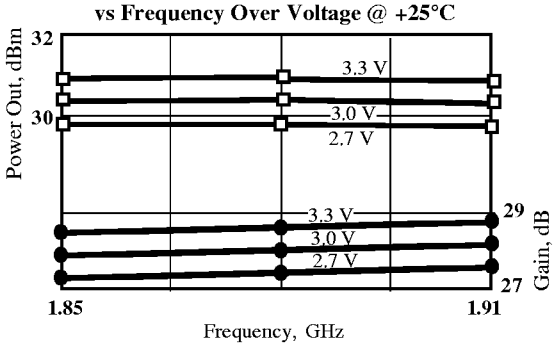
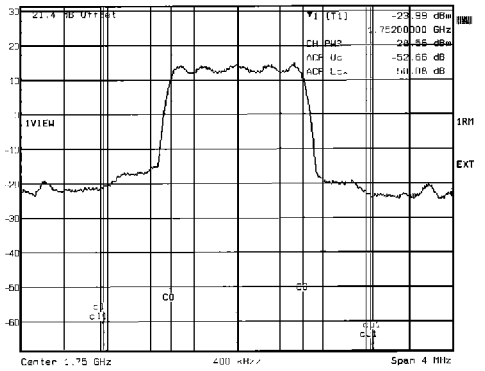
Typical Performance (Continued)

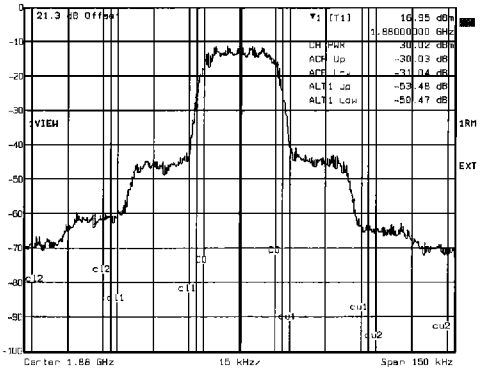
Gain & IS-136 TDMA Output Power vs Frequency Over Voltage @ +25°C



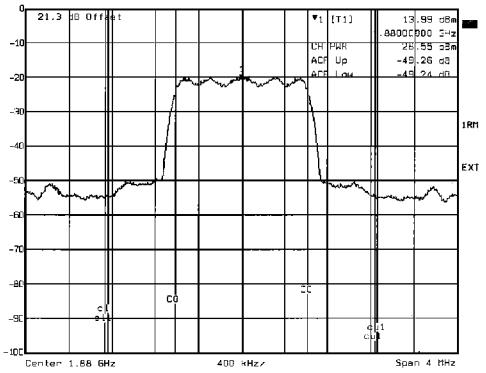
Korean CDMA Spectral Mask (Vdd=3.5V, 1,752 MHz, Po=+28.5 dBm)



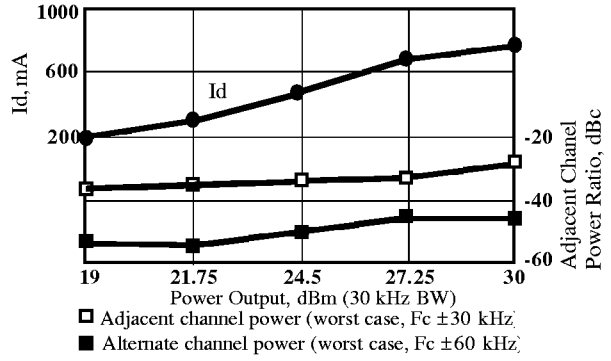
IS-136 TDMA Spectral Mask (Vdd=3.5V, 1,880 MHz, Po=+30 dBm)



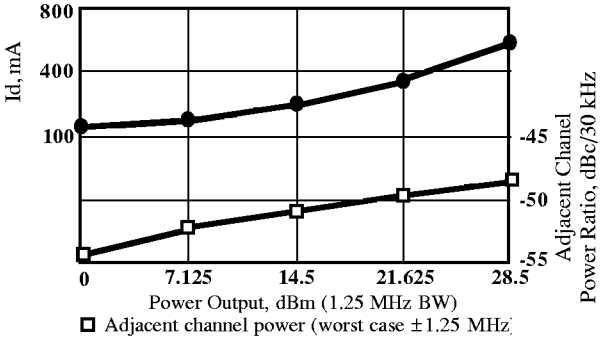
IS-98 CDMA Spectral Mask (Vdd=3.5V, 1,880 MHz, Po=+28.5 dBm)



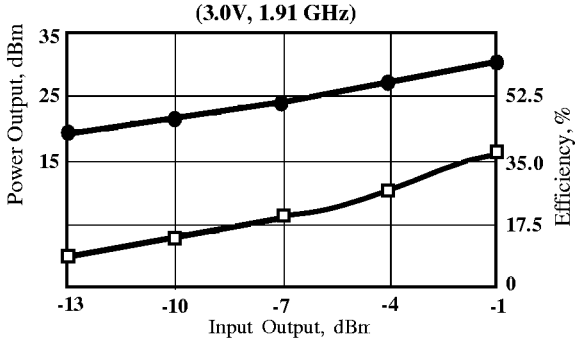
Id & IS-136 TDMA ACPR vs Power Output (3.5V, 1.91 GHz)



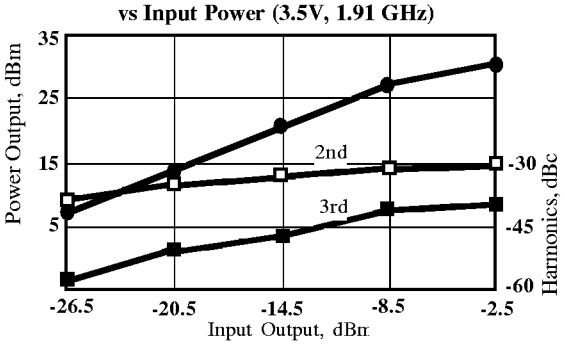
Id & IS-98 CDMA ACPR vs Power Output (3.5V, 1.91 GHz)



TDMA Power Output and Efficiency vs Input Power (3.0V, 1.91 GHz)



CDMA Power Output, 2nd and 3rd Harmonics vs Input Power (3.5V, 1.91 GHz)

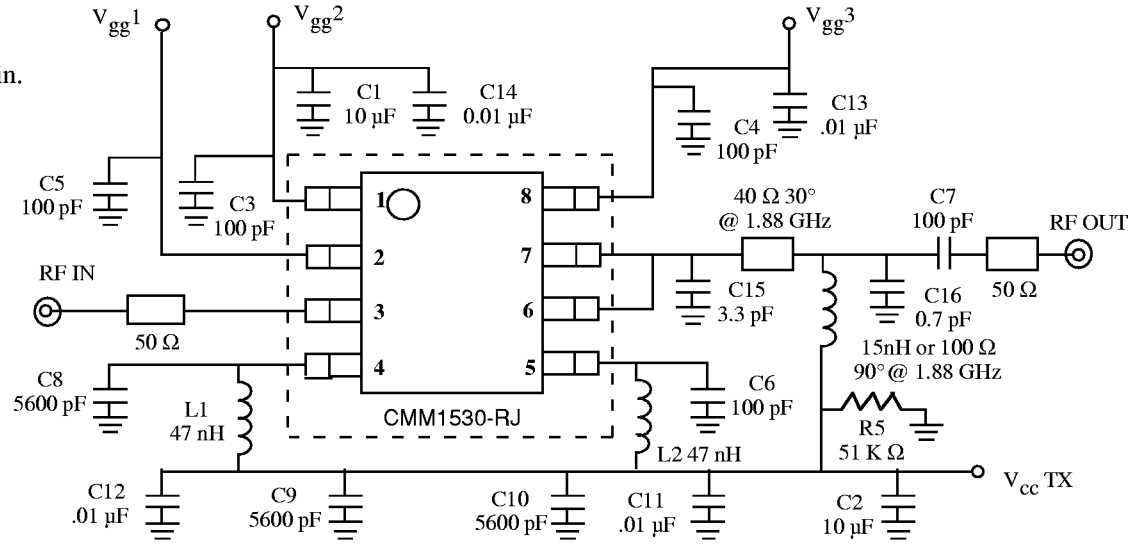


Recommended Matching Topology

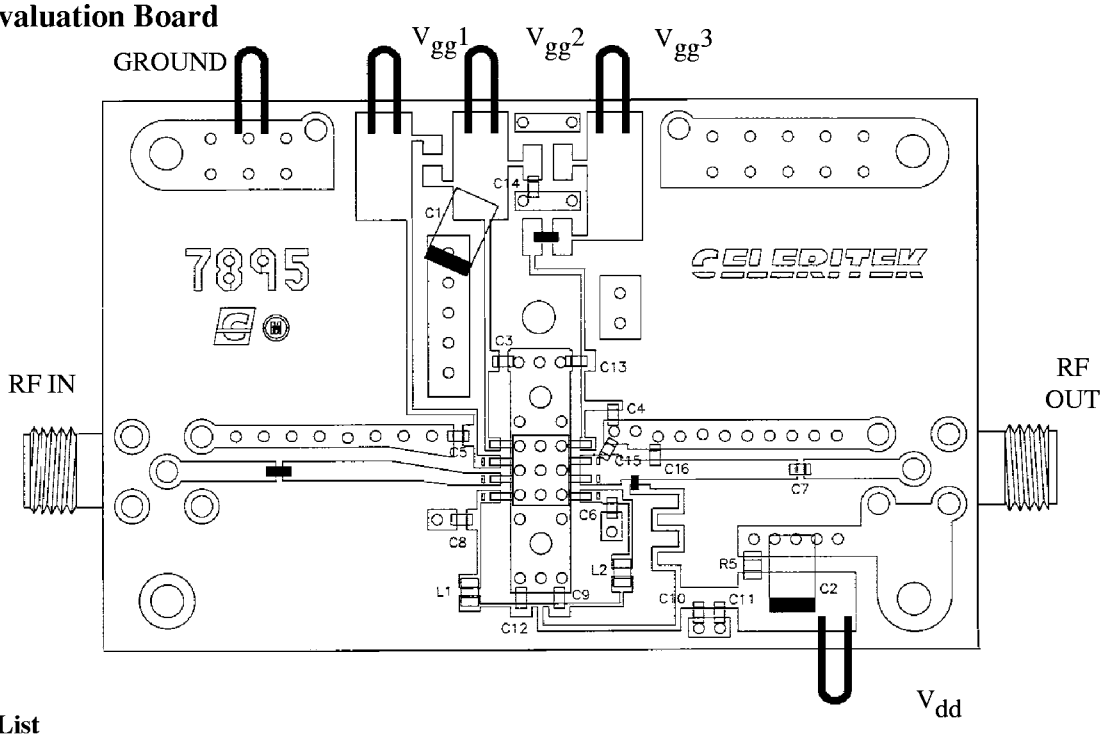
Note: This schematic represents the topology of the matching circuit recommended by Celeritek.

Evaluation Board Schematic

Board substrate:
ER = 4.60
Thickness = 0.031 in.



PB-CMM1530-RJ Evaluation Board



Evaluation Board Parts List

Part Type	Reference Designator	Description
Resistor	R5	0805, 51K Ω
Capacitor	C1, C2	C Case, 10µF
Capacitor	C8, C9, C10	0603, X7R, 5600pF
Capacitor	C11, C12, C13, C14	0603, X7R, .01µF
Capacitor	C3, C4, C5, C6, C7	0603, NPO, 100pF
Capacitor	C15	0603, Hi Q, 3.3pF
Capacitor	C16	0603, NPO, 0.7pF
Inductor	L1, L2	0805, 47nH

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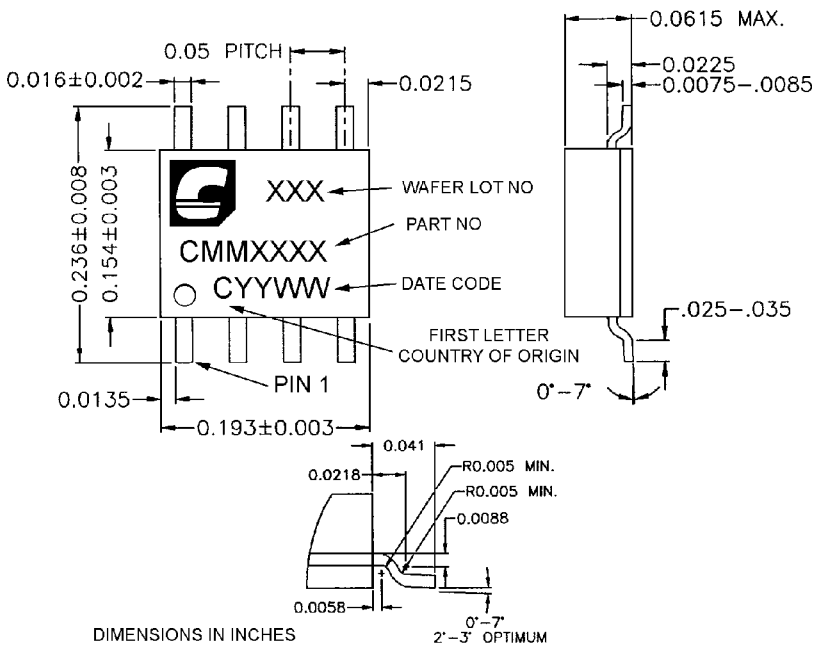
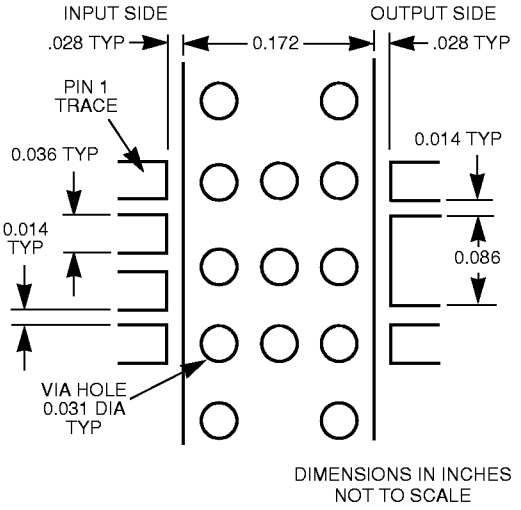
Physical Dimensions



Partial PCB Layout (for device position)



Ordering Information

The CMM1530-RJ is available in a surface mount plastic SOIC-8 package and devices are available in tube or tape and reel.

Part Number for Ordering	Package
CMM1530-RJ-00S0	**SOIC-8 CDMA surface mount power package in tube**
CMM1530-RJ-00T0	**SOIC-8 TDMA surface mount power package in tube**
CMM1530-RJ-00ST	**SOIC-8 CDMA surface mount power package in tape and reel**
CMM1530-RJ-00TT	**SOIC-8 TDMA surface mount power package in tape and reel**
PB-CMM1530-RJ-00S0	**Evaluation Board with SMA connectors for CMM1530-RJ-00S0 tested CDMA**
PB-CMM1530-RJ-00T0	**Evaluation Board with SMA connectors for CMM1530-RJ-00T0 tested TDMA**