AMERICAN MICROSYSTEMS, INC.

FS6017-02

Five PLL Clock Generator IC

November 1998

1.0 Features

- Five phase-locked loops (PLLs) generate five independent clocks from one reference clock
- Three PLL frequencies can be changed via logic level on the SEL input
- Clock outputs can be tristated to facilitate circuit board testing
- Small circuit board footprint (16-pin 0.150″ SOIC)
- Custom frequency selections available – contact your local AMI Sales Representative for more information

2.0 Description

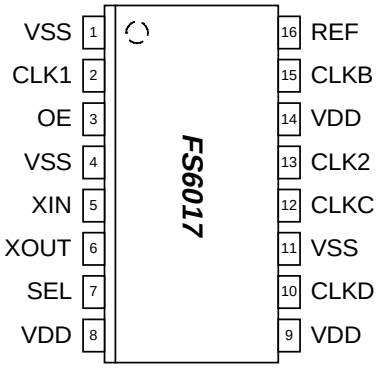
The FS6017 is a monolithic CMOS clock generator IC designed to minimize cost and component count in network computer applications.

Five internal high-performance phase-locked loops use an on-chip crystal oscillator as a reference for generation of various frequencies. The PLL-generated clock frequencies are related to the crystal oscillator frequency by exact ratios.

3.0 Applications

- Frequency Synthesis
- Network Computer (NC), Fast Network Computer, and Thin Client Applications

Figure 1: Pin Configuration



16-pin 0.150″ SOIC

Figure 2: Block Diagram

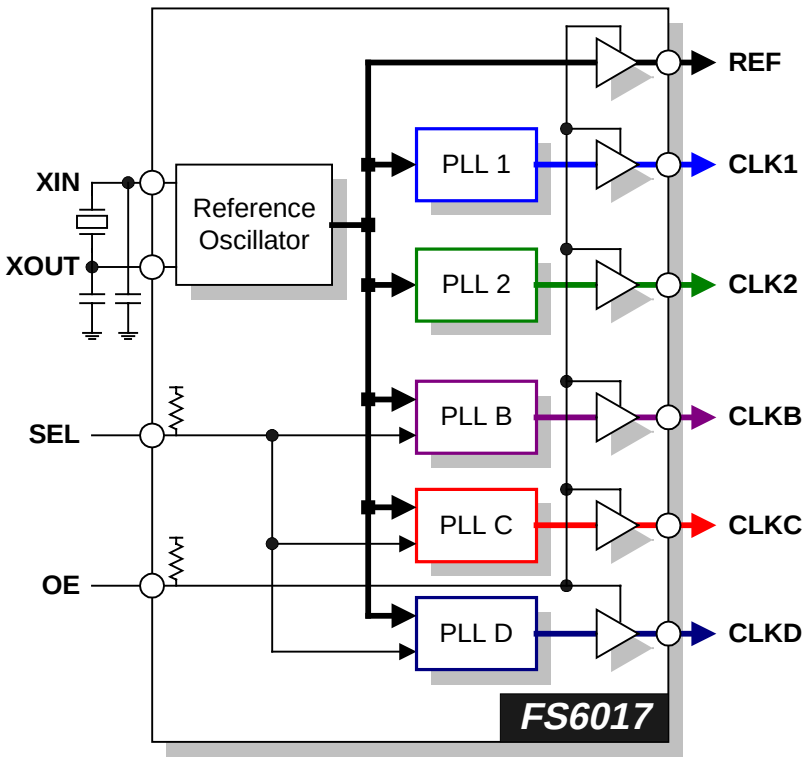


Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	P	VSS	Crystal Oscillator Ground
2	DO	CLK1	PLL 1 Clock Output
3	DI^U	OE	Output Enable
4	P	VSS	Ground
5	AI	XIN	Crystal Oscillator Feedback
6	AO	XOUT	Crystal Oscillator Drive
7	DI^U	SEL	Output Frequency Select
8	P	VDD	Power Supply (+5V)
9	P	VDD	Crystal Oscillator Power (+5V)
10	DO	CLKD	PLL D Clock Output
11	P	VSS	Ground
12	DO	CLKC	PLL C Clock Output
13	DO	CLK2	PLL 2 Clock Output
14	P	VDD	Power Supply (+5V)
15	DO	CLKB	PLL B Clock Output
16	DO	REF	Reference Oscillator Output

4.0 Functional Block Description

4.1 Phase-Locked Loops (PLLs)

Each one of the five on-chip PLLs in the FS6017 is a standard frequency- and phase-locked loop architecture. Each PLL multiplies the reference oscillator to the desired frequency by a ratio of integers. The frequency multiplication is exact.

4.2 Frequency Select (SEL)

Three of the PLLs can switch between one of two possible output frequencies depending on the logic state of the SEL pin. The clock outputs that can be changed are the CLKB, CLKC, and CLKD outputs. Note that the transitions are not glitch-free.

The SEL pin defaults to a logic-high through an internal pull-up.

Table 2: Output Frequencies

OUTPUT CLOCK	SEL PIN	FREQUENCY (MHz)
CLK1	-	11.2896
CLK2	-	32.0000
CLKB	1	56.0000
	0	64.0000
CLKC	1	40.0000
	0	48.0000
CLKD	1	80.0000
	0	3.6864

NOTE: Custom frequencies available – contact AMI for more information

4.3 Output Tristate Control (OE)

All clock outputs of the FS6017 may be tristated to facilitate circuit board testing. When the output enable (OE) pin is low, all outputs are placed in a high-impedance state and the outputs can neither drive nor load connected lines.

By default, all the clock outputs are enabled through an internal pull-up on the OE pin.

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4.4 Crystal Oscillator

An on-board 24MHz crystal oscillator provides the reference frequency for all five PLLs. Loading capacitors are left external to allow the user to vary crystal types and frequencies.

The oscillator operates the crystal in a parallel-resonant mode. Series-resonant crystals can also be used with the FS6017, although the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025 to 0.05%)

Since the entire operation of the FS6017 depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Take care to avoid routing clock lines near the crystal and, if possible, ground the crystal can to the ground plane.

The output of the crystal oscillator is directly observable at the REF output.

5.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V ± 10%	4.5	5	5.5	V
Ambient Operating Temperature Range	T_A		0		70	°C
Output Load Capacitance	C_L				15	pF
Crystal Resonator Frequency	f_{XIN}		5		27	MHz
Crystal Resonator Load Capacitance	C_{xtal}	Assumes 6pF external load capacitance typically achieved with 12pF from XIN to VSS and 12pF from XOUT to VSS		15		pF
Crystal Resonator Motional Capacitance	C_{MOT}			25		fF

Table 5: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs *	I_{DD}	OE = SEL = 5.0V		80		mA
Supply Current, Dynamic, with Tristated Outputs	I_{DD}	OE = 0V		55	80	mA
Control Inputs (SEL, OE)						
High-Level Input Voltage	V_{IH}		2.4		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}		-1		1	µA
Low-Level Input Current (pull-up)	I_{IL}	Outputs off; V_{IL} = 0V, V_{DD} = 5.5V	2	3.8	10	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}		1.5	2.4	3.5	V
High-Level Input Current	I_{IH}	V_{DD} = V_I = 5.5V	55	83	100	µA
Low-Level Input Current	I_{IL}	V_{DD} = 5.5V; V_I = 0V	-55	-81	-100	µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT (see Table 4)		9		pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XIN; XOUT unconnected		18		pF
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current	I_{OH}	V_{DD} = 5.5V, V_O = 0V	-10	-19	-33	mA
Low-Level Output Sink Current	I_{OL}	V_{DD} = V_O = 5.5V	10	26	33	mA
Clock Outputs (CLK1, CLK2, CLKB, CLKC, CLKD, REF)						
High-Level Output Source Current	I_{OH}	V_O = 2.4V	-26	-37		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V	7	9.2		mA
Output Impedance	z_{OH}	V_O = 0.5V_{DD}; output driving high		57		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		52		
Tristate Output Current	I_Z		-10		10	µA
Short Circuit Source Current *	I_{SCH}	V_O = 0V; shorted for 30s, max.		-50		mA
Short Circuit Sink Current *	I_{SCL}	V_O = 5V; shorted for 30s, max.		55		mA

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Table 6: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (REF)							
Duty Cycle *		From rising edge to rising edge at 2.5V	24.000	50		54	%
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	24.000		1000		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	24.000		1440		ps
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.1		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.2		ns
Clock Output (CLK1)							
Duty Cycle *		From rising edge to rising edge at 2.5V	32.000	46		50	%
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	32.000		490		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	32.000		1690		ps
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.2		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.0		ns
Clock Stabilization Time *	t_{STB}	From power-up to output active			1.3		ms
Clock Output (CLK2)							
Duty Cycle *		From rising edge to rising edge at 2.5V	11.289	43		47	%
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	11.289		840		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	11.289		2900		ps
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			4.0		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.1		ns
Clock Stabilization Time *	t_{STB}	From power-up to output active			1.3		ms
Clock Output (CLKB)							
Duty Cycle *		From rising edge to rising edge at 2.5V	56.000	39		43	%
			64.000	38		42	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	56.000		1350		ps
			64.000		1760		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	56.000		1990		ps
			64.000		1950		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.1		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.6		ns
Clock Stabilization Time *	t_{STB}	From power-up to output active			1.5		ms

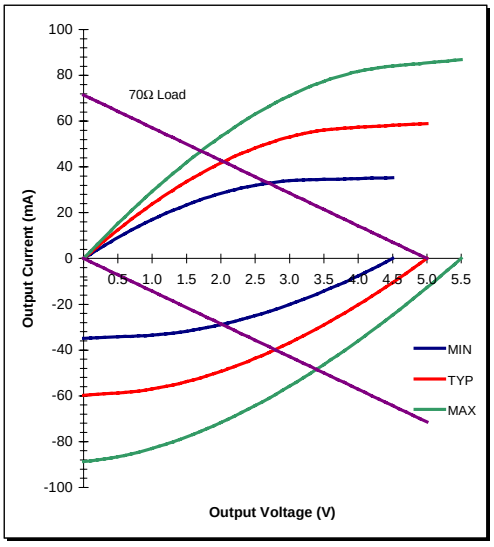
Table 7: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (CLKC)							
Duty Cycle *		From rising edge to rising edge at 2.5V	40.000	43		47	%
			48.000	42		46	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	40.000		1550		ps
			48.000		2070		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	40.000		1530		ps
			48.000		2720		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.0		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.3		ns
Clock Stabilization Time *	t_{STB}	From power-up to output active			1.3		ms
Clock Output (CLKD)							
Duty Cycle *		From rising edge to rising edge at 2.5V	80.000	39		43	%
			3.686	48		52	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	80.000		1260		ps
			3.686		1620		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			2.7		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.3		ns
Clock Stabilization Time *	t_{STB}	From power-up to output active			1.9		ms

Figure 3: CLK1, CLK2, CLKB, CLKC, CLKD, REF Clock Outputs

Voltage (V)	Low Drive Current (mA)			Voltage (V)	High Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-35	-60	-89
0.2	4	5	6	0.5	-34	-59	-87
0.5	9	13	15	1	-33	-57	-83
0.7	12	17	21	1.5	-32	-54	-78
1	17	24	29	2	-29	-49	-72
1.2	20	28	35	2.5	-25	-44	-64
1.5	23	34	42	2.7	-23	-41	-61
1.7	26	37	47	3	-20	-37	-56
2	28	42	53	3.2	-18	-34	-52
2.2	30	45	57	3.5	-14	-29	-46
2.5	32	48	63	3.7	-12	-26	-42
2.7	33	50	67	4	-8	-20	-36
3	34	53	71	4.2	-5	-16	-32
3.5	35	56	77	4.5	0	-11	-25
4	35	57	82	4.7		-6	-20
4.5	35	58	84	5		0	-13
5		59	85	5.2			-8
5.5			87	5.5			0



The data in this table represents nominal characterization data only.

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6.0 Package Information

Table 8: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

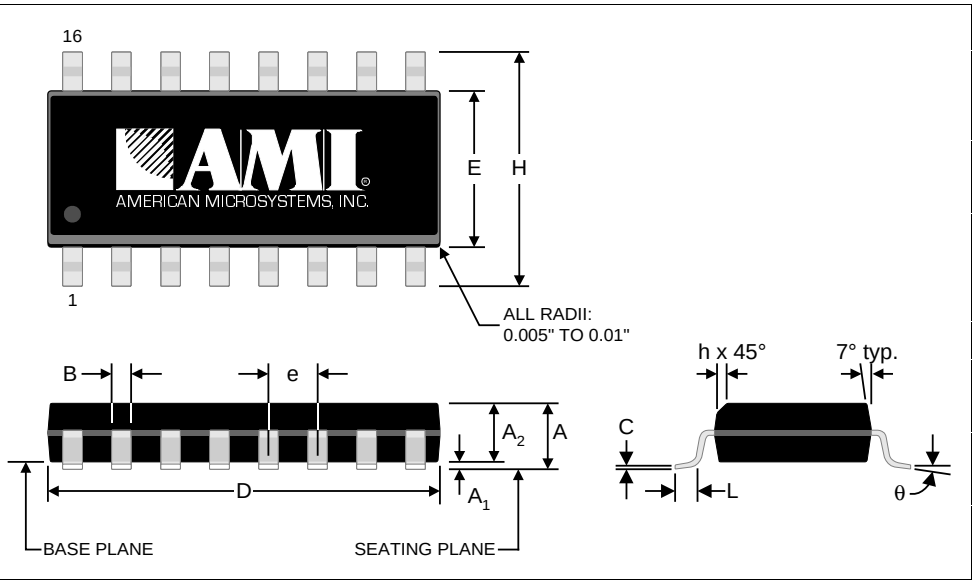

Table 9: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	109	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

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7.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	FONT	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11117-002	FS6017	-02	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape-and-Reel

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