CY7C197

256K x 1 Static RAM

Features

- **High speed**
  — 12 ns
- **CMOS for optimum speed/power**
- **Low active power**
  — 880 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

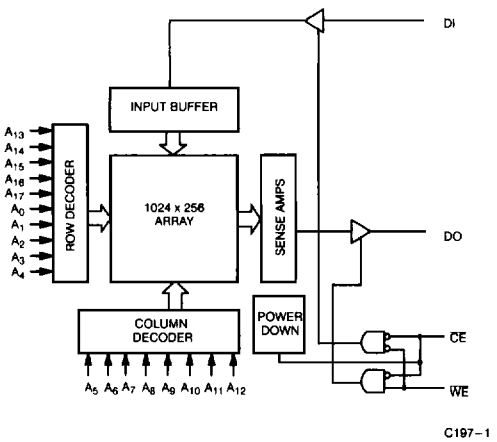
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The CY7C197 utilizes a die coat to ensure alpha immunity.

Logic Block Diagram



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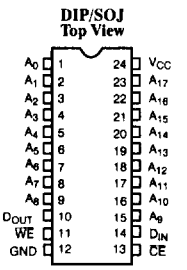
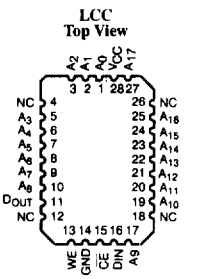
Pin Configurations



C197-2



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Selection Guide

		7C197-12	7C197-15	7C197-20	7C197-25	7C197-35	7C197-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	150	140	135	95	95	
	Military		160	150	105	105	105
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

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Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			7C197−12 Min.	7C197−12 Max.	7C197−15 Min.	7C197−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
			I_{OL} = 8.0 mA	Mil				0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		150		140	mA
				Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V		Com'l		10		10	mA
				Mil				15	

Shaded area contains preliminary information.

Notes:

1. $V_{(min.)}$ = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

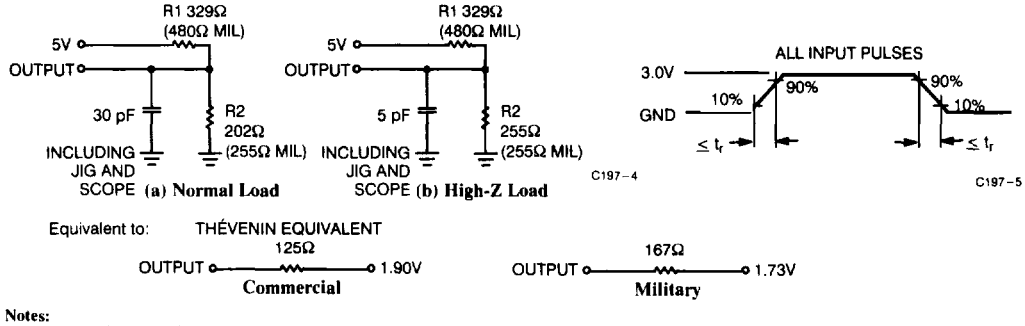
Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions			7C197-20 Min.	7C197-20 Max.	7C197-25, 35, 45 Min.	7C197-25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Mil		0.4		0.4	V
			I_{OL} = 12.0 mA	Com'l		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		Com'l		135		95	mA
				Mil		150		105	
I_{SB1}	Automatic $\overline{CE}$ Power Down Current—TTL Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} < 0.3V				15		15	mA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[7]



Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 8]

Parameter	Description	7C197–12		7C197–15		7C197–20		7C197–25		7C197–35		7C197–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		5		7	0	9	0	11	0	15	0	15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		25		30	ns
WRITE CYCLE[11]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		20		30		40		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	8		9		10		15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	2		2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7	0	10	0	11	0	15	0	15	ns

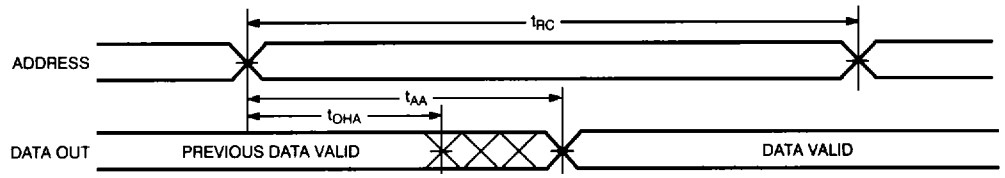
Shaded area contains preliminary information.

Notes:

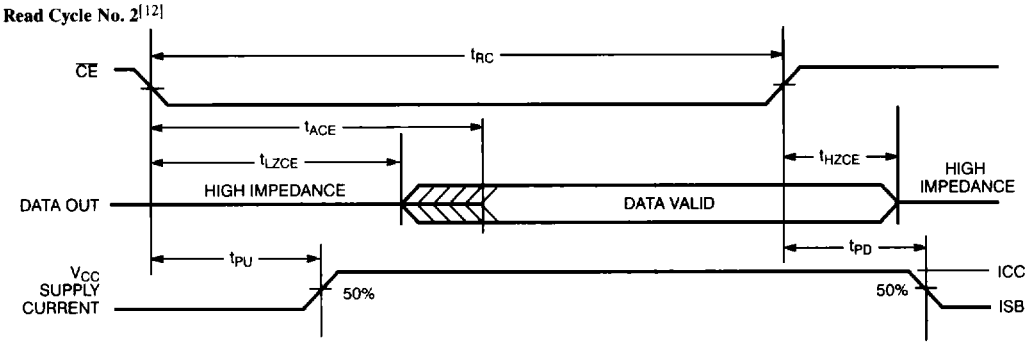
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

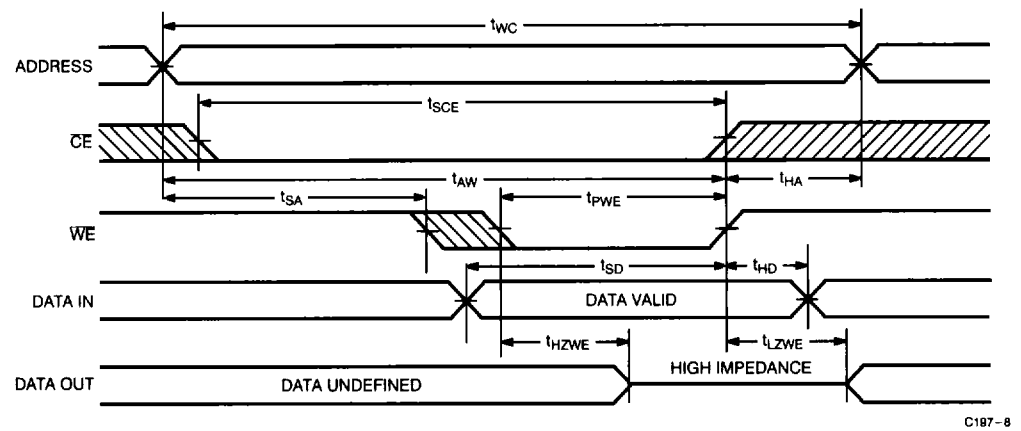
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12]



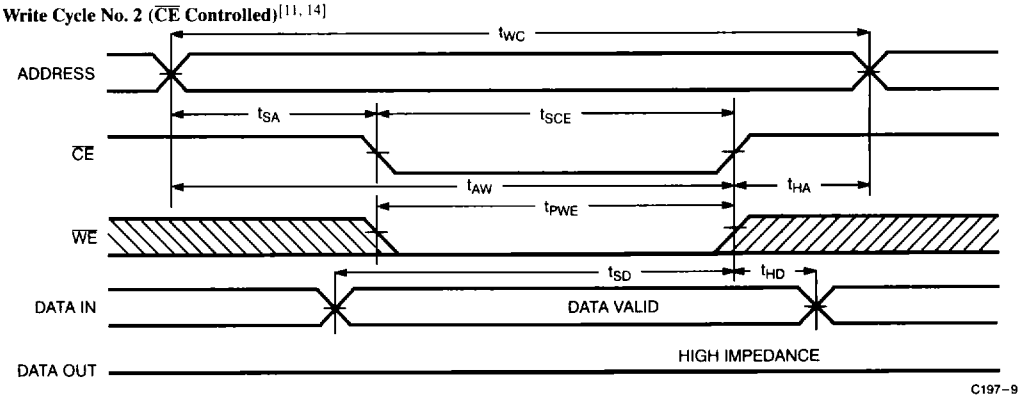
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



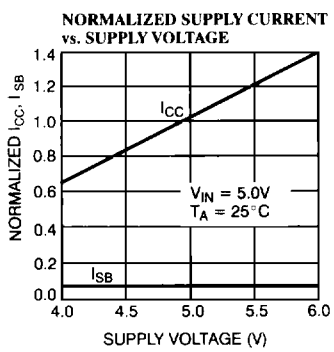
Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

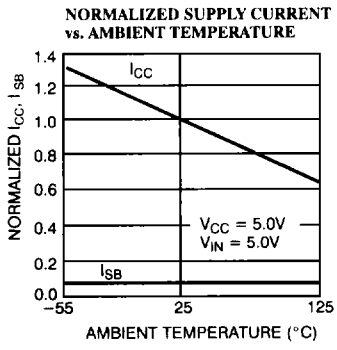
Switching Waveforms (continued)

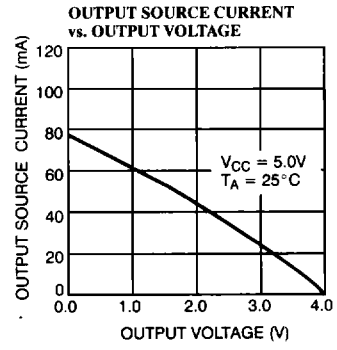
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 14]

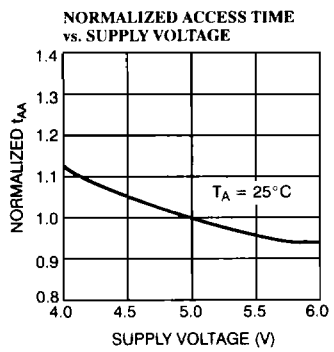


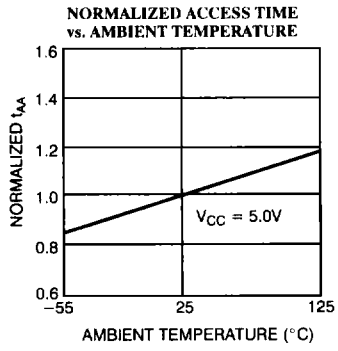
Typical DC and AC Characteristics

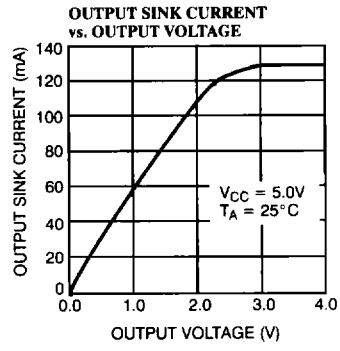






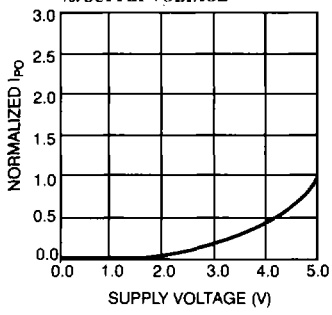




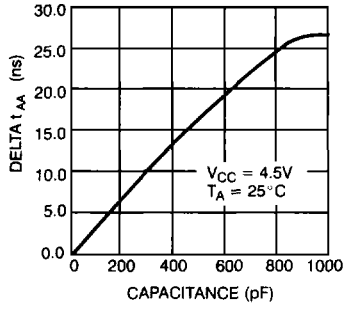


Typical DC and AC Characteristics (continued)

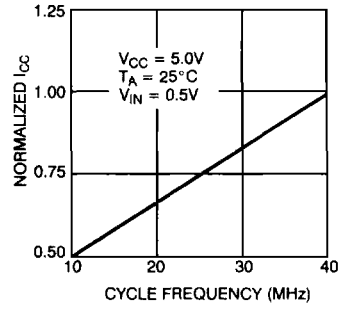
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C197 Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	**CY7C197–12PC**	**P13**	**24-Lead (300-Mil) Molded DIP**	**Commercial**
	CY7C197–12VC	**V13**	**24-Lead Molded SOJ**	
15	CY7C197–15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–15VC	V13	24-Lead Molded SOJ	
	CY7C197–15DMB	**D14**	**24-Lead (300-Mil) CerDIP**	**Military**
20	CY7C197–20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–20VC	V13	24-Lead Molded SOJ	
	CY7C197–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C197–25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–25VC	V13	24-Lead Molded SOJ	
	CY7C197–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–25LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
35	CY7C197–35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C197–35VC	V13	24-Lead Molded SOJ	
	CY7C197–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–35LMB	L54	24-Pin Rectangular Leadless Chip Carrier	
45	CY7C197–45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C197–45LMB	L54	24-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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