INCH-POUND
MIL-M-38510/135D
01 June 2005
SUPERSEDING
MIL-M-38510/135C
05 November 2003

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, LOW OFFSET OPERATIONAL AMPLIFIERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

Reactivated for new design as of 05 November 2003. May be used for either new or existing design acquisition.

The requirement for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, low offset operational amplifiers. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4)

1.2 Part or identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. Devices may be monolithic or they may consist of two separate independent die. The device types are as follows:

Device type	Circuit
01	Single operational amplifier, ultra low offset, internally compensated
02	Single operational amplifier, low offset, internally compensated
03	Single operational amplifier, ultra low offset, internally compensated, ultra low noise
04	Dual operational amplifier, low offset, ultra low noise internally compensated
05	Single operational amplifier, ultra low offset, internally compensated, ultra low noise, broadband

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43216-5000, or emailed to linear@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) .... ±22 V
Input voltage (V_{IN}) .... $\pm V_{CC}$
Differential input voltage range:
Device types 01 and 02 .... ±30 V
Device types 03, 04, and 05 .... ±0.7 V
Output short-circuit duration 1/
Lead temperature (soldering, 60 seconds) .... +300°C
Storage temperature range .... -65°C to +150°C
Junction temperature (T_J) .... +175°C 2/
Maximum power dissipation (P_D) .... 500 mW 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):
Device types 01 and 02 .... ±4.5 V dc to ±20.0 V
Device types 03, 04, and 05 .... ±4.5 V dc to ±18.0 V
Ambient operating temperature range (T_A) .... -55°C to +125°C

1.5 Power and thermal characteristics.

Case outlines	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
C	400 mW at T_A = +125°C	50°C/W	120°C/W
G	330 mW at T_A = +125°C	60°C/W	150°C/W
P	400 mW at T_A = +125°C	50°C/W	120°C/W
2	400 mW at T_A = +125°C	55°C/W	120°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

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1/ Output may be shorted to ground indefinitely at V_S = ±15 volts, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
2/ For short term test (in the specific burn-in and steady state life test configuration when required and up to 168 hours maximum), T_J = 175°C.
3/ Maximum power dissipation versus ambient temperature.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Circuit diagram and terminal connections. The circuit diagram and terminal connections shall be as specified on figure 1.

3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and unless otherwise specified, apply over the full recommended ambient operating temperature range for supply voltages from ±4.5 V dc to ±20 V dc for device types 01 and 02 and for supply voltages from ±4.5 V dc to ±18 V dc for device types 03, 04, and 05. Unless otherwise specified, source resistance (R_S) shall be 50 ohms for all tests.

3.5.1 Offset null circuits. The nulling inputs shall be capable of being nulled 0.5 mV beyond the specified offset voltage limits for $-55°C \leq T_A \leq 125°C$ using the circuit of figure 2.

3.5.2 Instability oscillations. The devices shall be free of oscillations when operated in the test circuits of this specification.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $\pm V_{CC} = \pm 15$ V, unnulled, see figure 3 and 3.5 unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	2/ 3/ 4/ see figure 4, $T_A = 25°C$	01,03, 05	-25	25	µV
			02	-75	75	
			04	-80	80	
		2/ 3/ $-55°C \leq T_A \leq +125°C$	01,03, 05	-60	60	
			02	-200	200	
			04	-180	180	
		End point limit 4/	01,03, 05	-100	100	
			02	-175	175	
			04	-180	180	
Input offset voltage temperature sensitivity	$\Delta V_{IO} / \Delta T$		01,03, 05	-0.6	0.6	µV/°C
			02	-1.3	1.3	
			04	-1.0	1.0	
Input bias current	$+I_{IB}$	$T_A = 25°C$ 2/	01	-2	2	nA
			02	-3	3	
			03,04, 05	-40	40	
		$-55°C \leq T_A \leq +125°C$ 2/	01	-4	4	
			02	-6	6	
			03,04, 05	-60	60	
		End point limit 4/	01	-3	3	
			02	-4.5	4.5	
			03,04, 05	-50	50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $\pm V_{CC} = \pm 15$ V, unnulled, see figure 3 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Input bias current	$-I_{IB}$	$T_A = 25°C$ 2/	01	-2	2	nA
			02	-3	3	
			03,04, 05	-40	40	
		$-55°C \leq T_A \leq +125°C$ 2/	01	-4	4	
			02	-6	6	
			03,04, 05	-60	60	
		End point limit 4/	01	-3	3	
			02	-4.5	4.5	
			03,04, 05	-50	50	
Input offset current	I_{IO}	$T_A = 25°C$ 2/	01	-2	2	nA
			02	-2.8	2.8	
			03,04, 05	-35	35	
		$-55°C \leq T_A \leq +125°C$ 2/	01	-4	4	
			02	-5.6	5.6	
			03,04, 05	-50	50	
Power supply rejection ratio	+PSRR	$+V_{CC} = 20$ V to 5 V, $-V_{CC} = -15$ V, $T_A = 25°C$	01,02	-10	10	μV/V
		$+V_{CC} = 18$ V to 5 V, $-V_{CC} = -15$ V, $T_A = 25°C$	03,04, 05	-10	10	
	-PSRR	$-V_{CC} = -20$ V to -5 V, $+V_{CC} = 15$ V, $T_A = 25°C$	01,02	-10	10	
		$-V_{CC} = -18$ V to -5 V, $+V_{CC} = 15$ V, $T_A = 25°C$	03,04, 05	-10	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $\pm V_{CC} = \pm 15$ V, unnulled, see figure 3 and 3.5 unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 20 V to 5 V, $-V_{CC}$ = -15 V, -55°C ≤ T_A ≤ +125°C	01,02	-20	20	µV/V
		$+V_{CC}$ = 18 V to 5 V, $-V_{CC}$ = -15 V, -55°C ≤ T_A ≤ +125°C	03,04, 05	-16	16	
	-PSRR	$-V_{CC}$ = -20 V to -5 V, $+V_{CC}$ = 15 V, -55°C ≤ T_A ≤ +125°C	01,02	-20	20	
		$-V_{CC}$ = -18 V to -5 V, $+V_{CC}$ = 15 V, -55°C ≤ T_A ≤ +125°C	03,04, 05	-16	16	
	PSRR	V_{CC} = ±4.5 V to ±20 V, T_A = +25°C	01,02	-10	10	
		V_{CC} = ±4.5 V to ±18 V, T_A = +25°C	03,04, 05	-10	10	
		V_{CC} = ±4.5 V to ±20 V, -55°C ≤ T_A ≤ +125°C	01,02	-20	20	
		V_{CC} = ±4.5 V to ±18 V, -55°C ≤ T_A ≤ +125°C	03,04, 05	-16	16	
Common mode rejection mode	CMRR	V_{CM} = ±13 V, T_A = +25°C	01,02	110		dB
		V_{CM} = ±11 V, T_A = +25°C	03,04, 05	114		
		V_{CM} = ±13 V, -55°C ≤ T_A ≤ +125°C	01,02	106		
		V_{CM} = ±10 V, -55°C ≤ T_A ≤ +125°C	03,04, 05	108		
Adjustment for input offset	V_{IO} Adj(+)	T_A = +25°C 2/	All	0.5		mV
	V_{IO} Adj(-)				-0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $\pm V_{CC}$ = ±15 V, unnulled, see figure 3 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output short circuit current	$I_{OS}(+)$	t ≤ 25 ms 5/ -55°C ≤ T_A ≤ +125°C	03,05	-70		mA
			04	-60		
		t ≤ 25 ms 5/ T_A = +25°C, +125°C	01,02	-65		
		t ≤ 25 ms 5/ T_A = -55°C	01,02	-70		
	$I_{OS}(-)$	t ≤ 25 ms 5/ -55°C ≤ T_A ≤ +125°C	03,04, 05		70	
		t ≤ 25 ms 5/ T_A = +25°C, +125°C	01,02		65	
		t ≤ 25 ms 5/ T_A = -55°C	01,02		70	
Supply current	I_{CC}	T_A = +25°C 2/ 6/	01,02		4	mA
			03,04, 05		5	
		-55°C ≤ T_A ≤ +125°C 2/ 6/	01,02		5	
			03,04, 05		6	
Output voltage swing (minimum)	V_{OP}	R_L = 1 kΩ, -55°C ≤ T_A ≤ +125°C	01,02	-10	10	V
		R_L = 600 Ω, -55°C ≤ T_A ≤ +125°C	03,04, 05	-10	10	
		R_L = 2,000 Ω, -55°C ≤ T_A ≤ +125°C	01,02	-12	12	
			03,04, 05	-11.5	11.5	
Open loop voltage gain (single ended)	A_{VS}	T_A = +25°C 7/	01	300		V/mV
			02	200		
			03,04, 05	1,000		
		-55°C ≤ T_A ≤ +125°C 7/	01	200		
			02	150		
			03,04, 05	600		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $\pm V_{CC}$ = ±15 V, unnulled, see figure 3 and 3.5 unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Slew rate	SR(+) and SR(-)	V_{IN} = ±5 V, A_V = 1, T_A = +25°C, see figure 7	01,02	.08		V/µs
			03,04	1.7		
		V_{IN} = ±1 V, A_V = 5, T_A = +25°C, see figure 7	05	11		
Input noise voltage density	En	f_O = 10 Hz, T_A = +25°C, see figure 5	01,02		18	nV / $\sqrt{Hz}$
			03,05		5.5	
			04		6.0	
		f_O = 100 Hz	01,02		14	
			03,05		4.0	
			04		5.0	
		f_O = 1 kHz	01,02		12	
			03,05		3.8	
			04		3.9	
Low frequency input noise voltage	Enpp	f_O = 0.1 Hz to 10 Hz, T_A = +25°C, see figure 6	01,02		0.6	μV_{PP}
			03,05		0.18	
			04		0.20	
Input noise current density	In	f_O = 10 Hz, T_A = +25°C, see figure 5	03,04, 05		5.66	pA / $\sqrt{Hz}$
		f_O = 100 Hz, T_A = +25°C, see figure 5	03,05		1.88	
			04		2.1	
		f_O = 1 kHz, T_A = +25°C, see figure 5	03,05		0.84	
			04		0.89	

1/ For devices marked with the "Q" certification mark, the parameters listed herein may be guaranteed if not tested to the limits specified in accordance with the manufacturer's QM plan.

2/ Tested at V_{CM} = 0 V, V_{CC} = ±15 V.

3/ Due to the inherent warm-up drift of types 01, 03, 04, and 05, testing shall occur no sooner than 5 minutes after application of power.

4/ Refer to table IV for end-point parameters.

5/ Continuous short circuit limits are considerably less than the indicated test limits since maximum power dissipation cannot be exceeded.

6/ For device type 04, I_{CC} is per amplifier.

7/ V_{OUT} = 0 to +10 for $A_{VS(+)}$ and V_{OUT} = 0 to -10 for $A_{VS(-)}$. R_L = 2,000 Ω.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III) Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters 1/	1*, 2, 3, 4, 7	1*, 2, 3, 4, 7
Group A test requirements 2/	1, 2, 3, 4, 5, 6, 7, 9	1, 2, 3, 4, 5, 6, 7, 9
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3 and table IV delta limits	N/A
Group C end-point electrical parameters 3/	1, 2, 3 and table IV delta limits	1 and table IV delta limits
Group D end-point electrical parameters 3/	1, 2, 3 and table IV endpoint limits	1 and table IV endpoint limits

1/ PDA applies to subgroup 1.
2/ Subgroup 9 shall have a sample size series number of 5 for class S and class B devices.
3/ Table IV end-point parameters shall be used for V_{IO} and I_{IB} for class S and class B devices.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer’s Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 8, 10, and 11 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein. Delta limits shall apply to group C inspection, and shall consist of tests specified in table IV herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the ground terminal of the device under test (DUT). Current values given are for conventional current and are positive when flowing into the referenced terminal.

4.5.2 Life test cooldown procedures. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, they shall be cooled to within 10°C of their power stable condition at room temperature prior to removal of the bias.

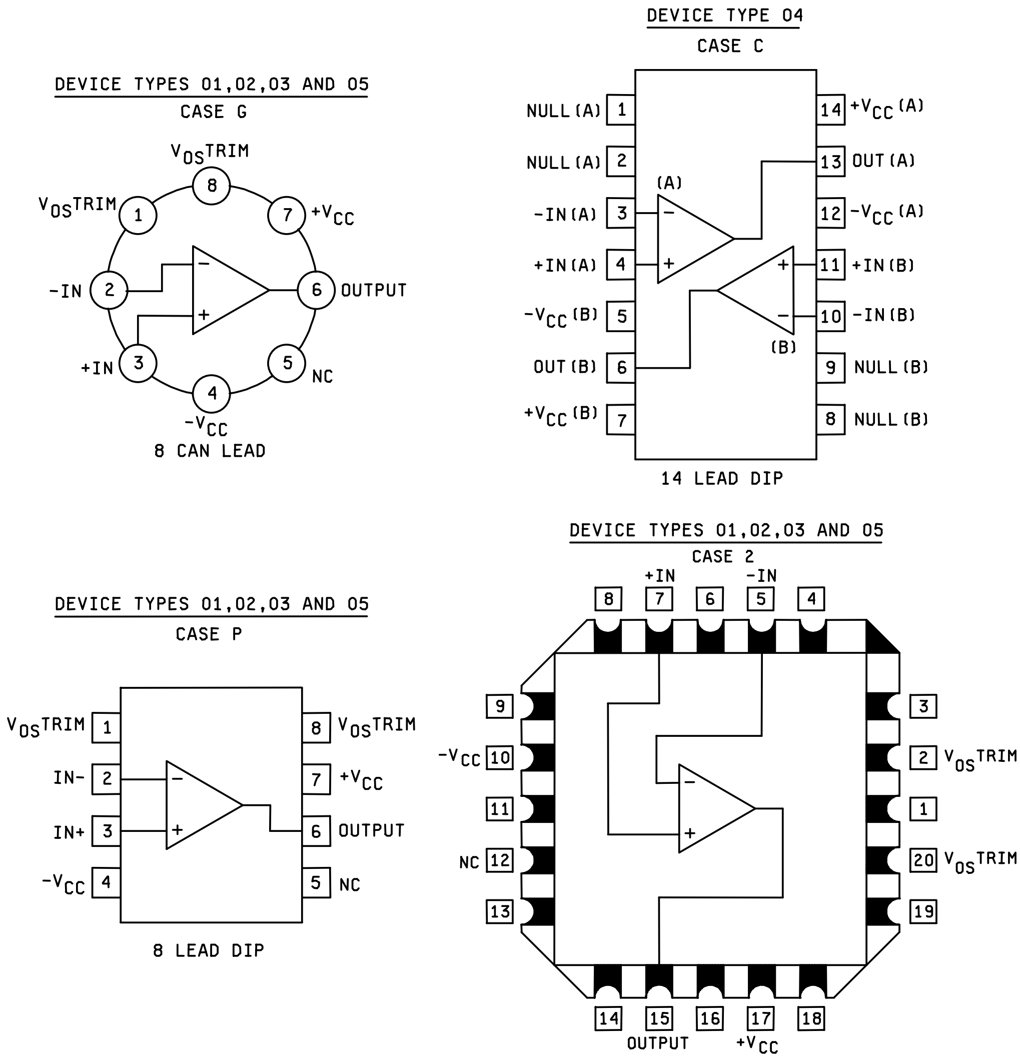


Figure 1. Terminal connections.

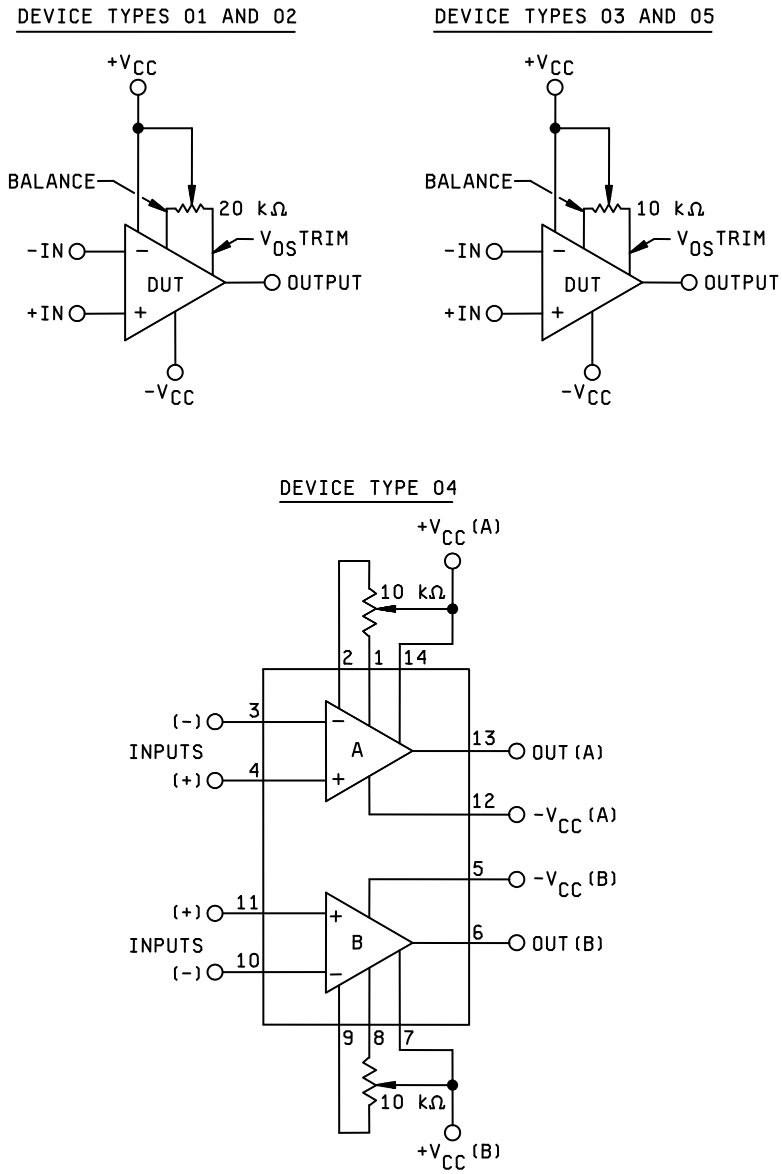
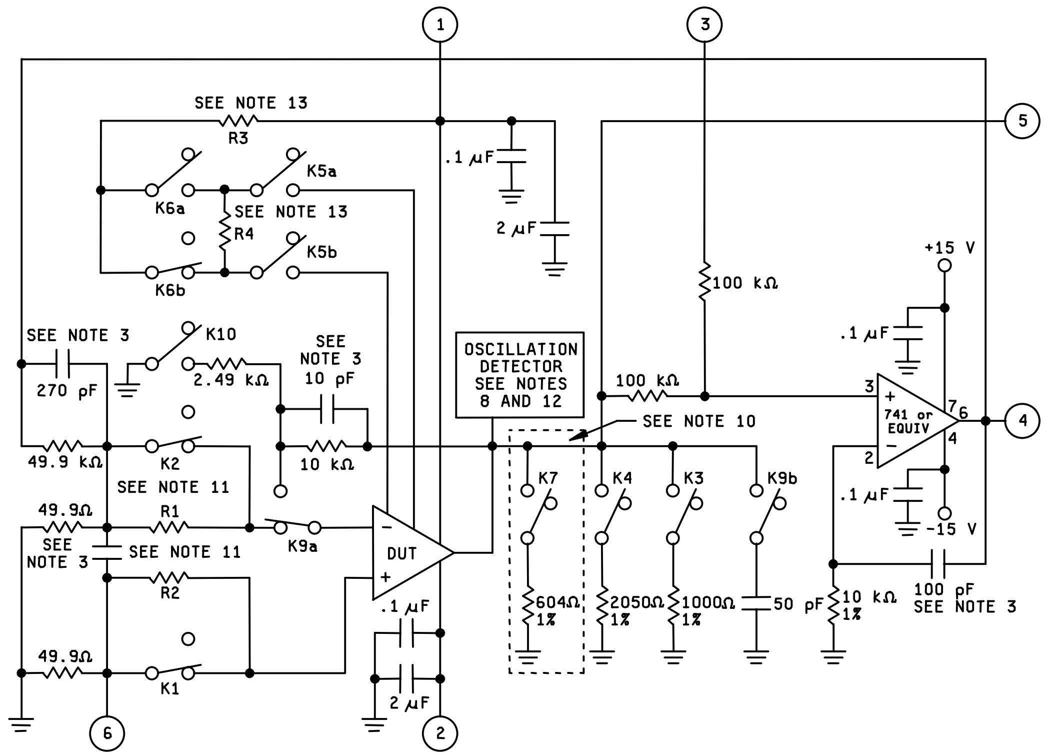


FIGURE 2. Offset null circuit.



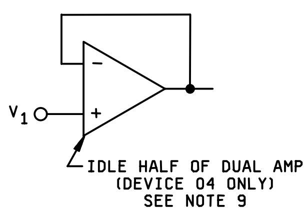


FIGURE 3. Test circuit for static tests and slew rate.

NOTES:

1. All resistors are ±0.1 % percent tolerance and all capacitors are ±10% unless specified otherwise.

2. Precautions shall be taken to prevent damage to the device under test (DUT) during insertion into socket and change of relay state (example: disable voltage supplies, current limit $\pm V_{CC}$, etc.).

3. Compensation capacitors should be added as required for test circuit stability. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.

4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.

5. All relays are shown in the normal de-energized state.

6. Saturation of the nulling amp is not allowed on tests where the Pin 4 value is measured.

7. The load resistors 1000 Ω and 2050 Ω yield effective load resistance of 100 Ω and 2000 Ω respectively.

8. Any oscillation greater than 300 mV pk-pk in amplitude shall be cause for device failure.

9. Device type 04 only, test both halves for all tests. The idle half of the dual amplifiers shall be maintained in this configuration where V_1 is midway between $+V_{CC}$ and $-V_{CC}$, or the manufacturer has the option to connect the idle half in a V_{ID} configuration such that the inputs are maintained at the same common mode voltage as the device under test.

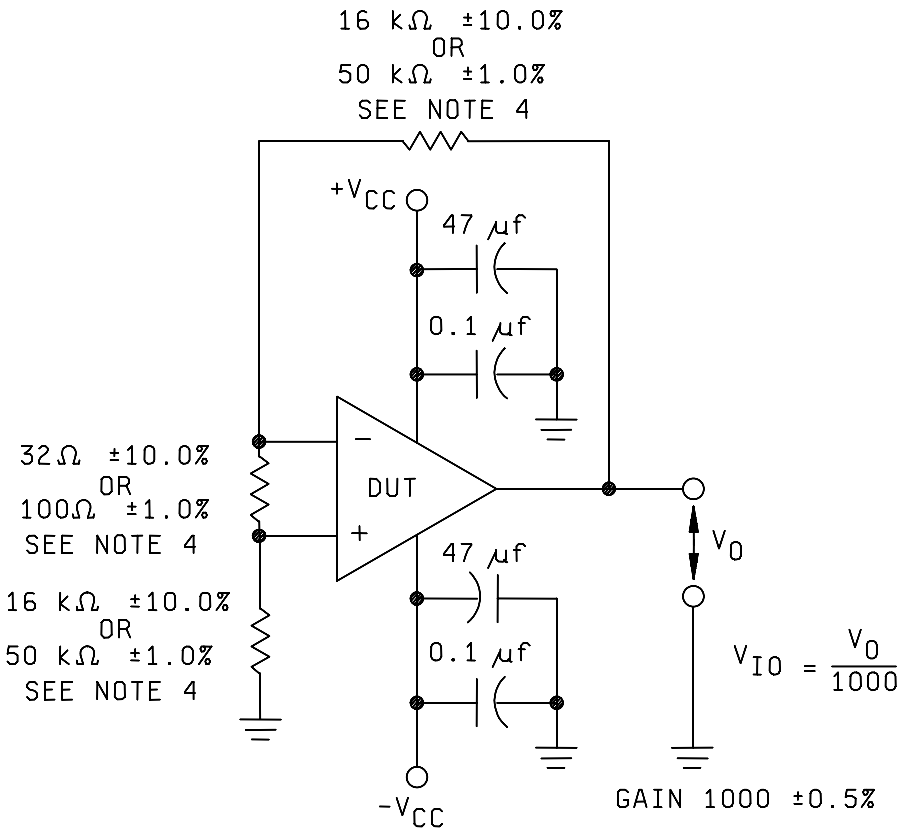
10. Circuit within dashed area used for devices 03, 04, and 05 only.

11. For devices 01 and 02: R1 = 500 kΩ ± .01%; R2 = 500 kΩ ± .01%.
    For device 03, 04, and 05: R1 = 50 kΩ ± .01%; R2 = 50 kΩ ± .01%.

12. When using this test circuit for measuring slew rate, the oscillation detector shall be disabled.

13. For devices 01 and 02: R3 = 27 kΩ, ±5 %, R4 = 100 kΩ, ±5 %.
    For devices 03, 04, and 05: R3 = 0 Ω, R4 = 10 kΩ, ±5 %.

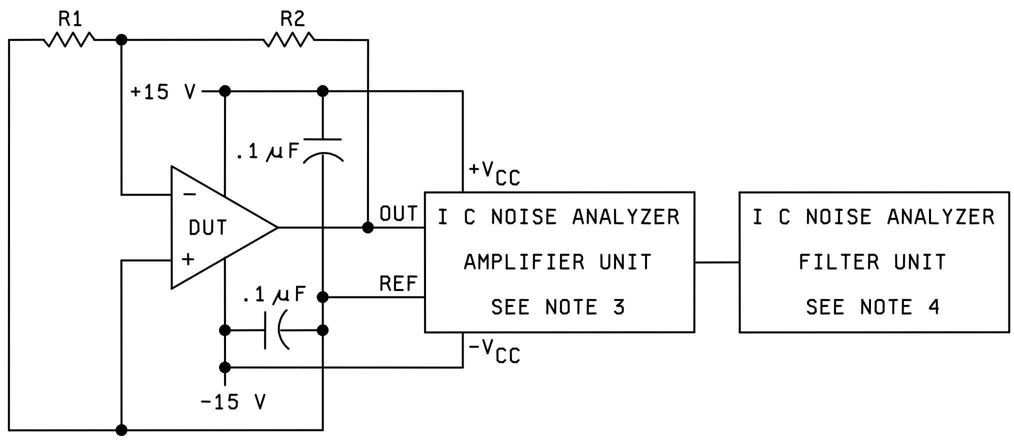
FIGURE 3. Test circuit for static tests and slew rate – Continued.



NOTES:

1. Same configuration used for both amplifiers of device 04.
2. Low thermal EMF sockets are recommended. The number of solder joints and dissimilar-metal junctions are to be minimized. The test circuit should contain a minimum number of components. All components should have the lowest possible temperature coefficients.
3. The temperature of the test circuit should be equal to that of the device under test (DUT).
4. Resistors 16 kΩ ±10.0%, 32 Ω ±10%, and 16 kΩ ±10.0 % must be used together or resistors 50 kΩ ±1.0%, 100 Ω ±1%, and 50 kΩ ±1.0% must be used together.

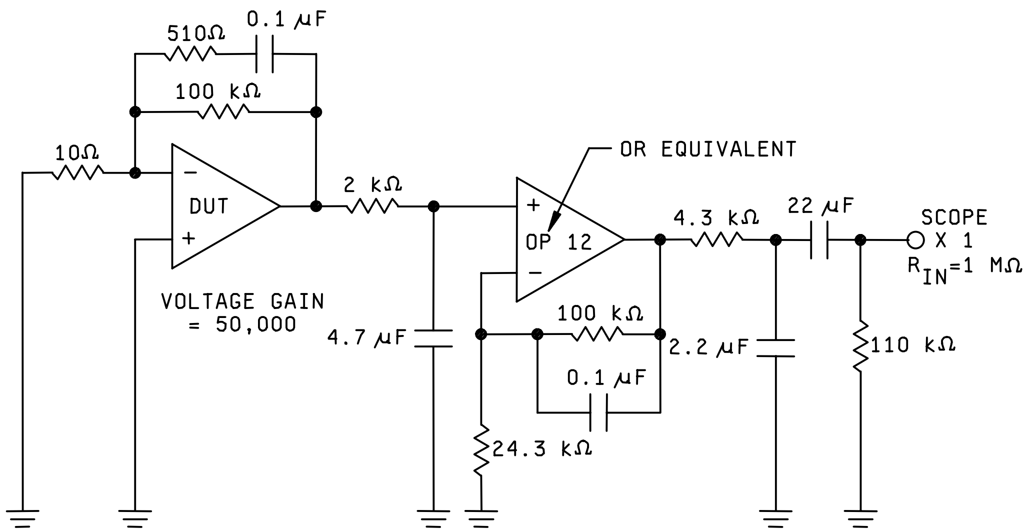
FIGURE 4. Voltage offset test circuit.



NOTES:

1. Input noise voltage density (En) test: R1 = 50 Ω, R2 = 10 kΩ.
   Input noise current density (In) test: R1 = 105 kΩ, R2 = 2 MΩ.
2. All resistors are metal film and ±1% tolerance. Capacitors are in microfarads and are ±10% tolerance.
3. Quan-Tech model 2283 or equivalent.
4. Quan-Tech model 2181 or equivalent.

FIGURE 5. Noise density test circuit.

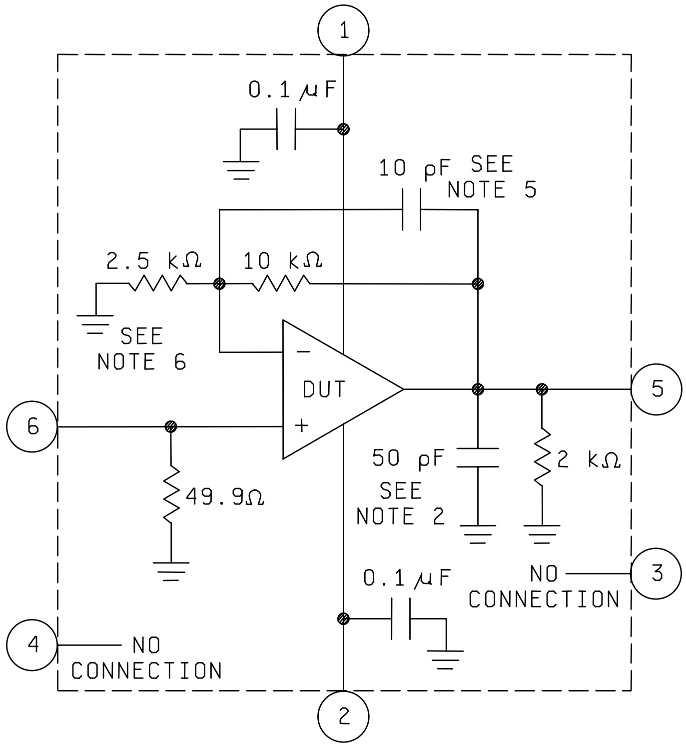


NOTES:

1. All capacitor values are for non polarized capacitors only.

2. Resistors values are ±1.0%.

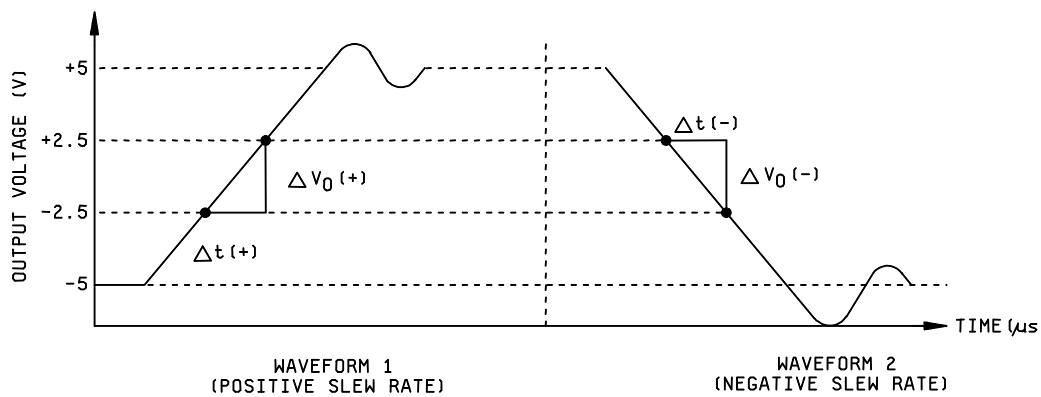
FIGURE 6. Low frequency test circuit.



NOTES:

1. Resistors are ±1.0 percent tolerance and capacitors are ±10 percent tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the device under test during insertion into socket and in applying power.
4. Pulse input and output characteristics are shown on the next space.
5. Compensation capacitors should be added as required for test circuit stability. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.
6. For device type 05 only.

FIGURE 7. Test circuit for slew rate.



Parameter symbol	Device type	Input pulse signal at $t_r \leq 50$ ns	Output pulse signal	Equation
SR(+)	01, 02, 03, 04	-5 V to +5 V step (AV = 1)	Waveform 1	$SR(+) = \Delta V_O(+) / \Delta t(+)$
SR(-)	01, 02, 03, 04	+5 V to -5 V step (AV = 1)	Waveform 2	$SR(-) = \Delta V_O(-) / \Delta t(-)$
SR(+)	05	-1 V to +1 V step (AV = 5)	Waveform 1	$SR(+) = \Delta V_O(+) / \Delta t(+)$
SR(-)	05	+1 V to -1 V step (AV = 5)	Waveform 2	$SR(-) = \Delta V_O(-) / \Delta t(-)$

FIGURE 7. Test circuit for slew rate - Continued.

TABLE III. Group A inspection for device types 01 and 02.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes 1/	Adapter pin number 1	2	3	Energized relays	Measured pin No.	Value	Units	Equation	Device type	Limits Min	Max	Unit
1 T_A = +25°C	$+I_{IB}$	4001 "	1 2		15 15	-15 -15	0 0	None K1	4 4	E1 E2	V V	V_{IO} = E1 $+I_{IB}$ = 2 (E1 – E2)	01 02	-2 -3	2 3	nA "
	$-I_{IB}$	"	3		15	-15	0	K2	4	E3	V	$-I_{IB}$ = 2 (E3 – E1)	01 02	-2 -3	2 3	" "
	I_{IO}	"	4	2/								I_{IO} = 2 (2E1 – E2 –E3)	01 02	-2 -2.8	2 2.8	nA
	+PSRR	4003	5		20 5	-15 -15	0 0	None	4	E4 E5	V "	+PSRR = 66 (E4 – E5)	01,02	-10	10	µV/V
	-PSRR	4003	6		15 15	-20 -5	0 0	None	4	E6 E7	V "	-PSRR = 66 (E6 – E7)	01,02	-10	10	µV/V
	PSRR	4003	7		4.5 20	-4.5 -20	0 0	None	4	E8 E9	V "	PSRR = 32.25 x (E8 - E9)	01,02	-10	10	µV/V
	CMRR	4003	8		28 2	-2 -28	-13 13	None	4	E10 E11	V "	CMRR = 20 log |26000/(E11 – E10)|	01,02	110		dB
	V_{IO} ADJ(+)		9		15	-15	0	K5	4	E12	"	V_{IO} ADJ(+) = E1 – E12	01,02	0.5		mV
	V_{IO} ADJ(-)		10		15	-15	0	K5,K6	4	E13	"	V_{IO} ADJ(-) = E1 – E13	01,02		-0.5	mV
	$I_{OS(+)}$	3011	11	3/	15	-15	-10	None	5	I1	mA	$I_{OS(+)}$ = I1	01,02	-65		mA
	$I_{OS(-)}$	3011	12	3/	15	-15	10	None	5	I2	mA	$I_{OS(-)}$ = I2	01,02		65	mA
	I_{CC}	4005	13		15	-15	0	None	1	I3	mA	I_{CC} = I3	01,02		4	mA
2 T_A = +125°C	V_{IO}	4001	14	Fig. 4	15	-15	0			E14	V	V_{IO} = E14/1000	01 02	-60 -200	60 200	µV "
	$+I_{IB}$	4001 "	16 17		15 15	-15 -15	0 0	None K1	4 4	E15 E16	" "	V_{IO} = E15 $+I_{IB}$ = 2 (E15 – E16)	01 02	-4 -6	4 6	nA "
	$-I_{IB}$	" "	18		15	-15	0	K2	"	E17	"	$-I_{IB}$ = 2 (E17 – E15) -	01 02	-4 -6	4 6	" "
	I_{IO}	"	19	2/								I_{IO} = 2 (2E15 – E16 –E17)	01 02	-4 -5.6	4 5.6	nA
	+PSRR	"	20		20 5	-15 -15	0 0	None	4	E18 E19	V V	+PSRR = 66(E18 – E19)	01,02	-20	20	µV/V
	-PSRR	"	21		15 15	-20 -5	0 0	None	4	E20 E21	V V	-PSRR = 66(E20 – E21)	01,02	-20	20	µV/V
	PSRR	"	22		4.5 20	-4.5 -20	0 0	None	4	E22 E23	V V	PSRR = 32.25 x (E22 – E23)	01,02	-20	20	µV/V
	CMRR	4003	23		28 2	-2 -28	-13 13	None	4	E24 E25	V "	CMRR = 20 log |26000/(E24 – E25)|	01,02	106		dB
	$I_{OS(+)}$	3011	24	3/	15	-15	-10	None	5	I4	mA	$I_{OS(+)}$ = I4	01,02	-65		mA
	$I_{OS(-)}$	3011	25	3/	15	-15	10	None	5	I5	mA	$I_{OS(-)}$ = I5	01,02		65	mA
	I_{CC}	4005	26		15	-15	0	None	1	I6	mA	I_{CC} = I6	01,02		5	mA

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin number			Energized relays	Measured pin			Equation	Device type	Limits		Unit
				1/	1	2	3		No.	Value	Units			Min	Max	
3 T_A = -55°C	V_{IO}	4001 “	27	Fig. 4	15	-15	0			E26	V	V_{IO} = E26/1000	01 02	-60 -200	60 200	µV “
	$+I_{IB}$	4001 “	29 30		15 15	-15 -15	0 0	None K1	4 “	E27 E28	“ “	V_{IO} = E27 $+I_{IB}$ = 2 (E27 – E28)	01 02	-4 -6	4 6	nA “
	$-I_{IB}$	“ “	31		15	-15	0	K2	“	E29	“	$-I_{IB}$ = 2 (E29 – E27)	01 02	-4 -6	4 6	“ “
	I_{IO}	4001	32	2/								I_{IO} = 2 (2E27 – E28 –E29)	01 02	-4 -5.6	4 5.6	nA
	+PSRR	4003	33		20 5	-15 -15	0 0	None	4	E30 E31	V “	+PSRR = 66 (E30 – E31)	01,02	-20	20	µV/V
	-PSRR	4003	34		15 15	-20 -5	0 0	None	4	E32 E33	V “	-PSRR = 66 (E32 – E33)	01,02	-20	20	µV/V
	PSRR	4003	35		4.5 20	-4.5 -20	0 0	None	4	E34 E35	V “	PSRR = 32.25 x (E34 – E35)	01,02	-20	20	µV/V
	CMRR	4003	36		28 2	-2 -28	-13 13	None	4	E36 E37	V “	CMRR = 20 log |26000/(E36 – E37)|	01,02	106		dB
	$I_{OS(+)}$	3011	37	3/	15	-15	-10	None	5	I7	mA	$I_{OS(+)}$ = I7	01,02	-70		mA
	$I_{OS(-)}$	3011	38	3/	15	-15	10	None	5	I8	mA	$I_{OS(-)}$ = I8	01,02		70	mA
	I_{CC}	3005	39		15	-15	0	None	1	I9	mA	I_{CC} = I9	01,02		5	mA
4 T_A = +25°C	$+V_{OP}$	4004	40 41		15	-15	-15	K3 K4	5	E38 E39	V V	$+V_{OP}$ = E38 $+V_{OP}$ = E39	01,02 01,02	10 12		V “
	$-V_{OP}$	4004	42 43		15	-15	15	K3 K4	5	E40 E41	V V	$-V_{OP}$ = E40 $-V_{OP}$ = E41	01,02 01,02		-10 -12	“ “
	$A_{VS}(+)$	4004	44		15	-15	-10	K4	4	E42	V	$A_{VS}(+)$ = 10/(E1 – E42)	01 02	300 200		V/mV
	$A_{VS}(-)$	4004	45		15	-15	10	K4	4	E43	V	$A_{VS}(-)$ = 10/(E43 – E1)	01 02	300 200		V/mV
	V_{IO}	4001	46	Fig. 4	15	-15	0			E44	V	V_{IO} = E44/1000	01 02	-25 -75	25 75	µV
5 T_A = +125°C	$+V_{OP}$	4004	47 48		15	-15	-15	K3 K4	5	E45 E46	V V	$+V_{OP}$ = E45 $+V_{OP}$ = E46	01,02 01,02	10 12		V “
	$-V_{OP}$	4004	49 50		15	-15	15	K3 K4	5	E47 E48	V V	$-V_{OP}$ = E47 $-V_{OP}$ = E48	01,02 01,02		-10 -12	“ “
	ΔV_{IO}/ ΔT	4001	15	Fig. 4 4/								$\Delta V_{IO} / \Delta T$ = (E14 – E44)/100(1000)	01 02	-0.6 -1.3	0.6 1.3	µV/°C
	$A_{VS}(+)$	4004	51		15	-15	-10	K4	4	E49	V	$A_{VS}(+)$ = 10/(E15 – E49)	01 02	200 150		V/mV
	$A_{VS}(-)$	4004	52		15	-15	10	K4	4	E50	V	$A_{VS}(-)$ = 10/(E50 – E15)	01 02	200 150		V/mV

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin nunbers			Energized relays	Measured pin			Equation	Device type	Limits		Unit
					1	2	3		No.	Value	Units			Min	Max	
6	$+V_{OP}$	4004	53		15	-15	-15	K3	5	E51	V	$+V_{OP}$ = E51	01,02	10		V
		“	54					K4		E52	“	$+V_{OP}$ = E52	01,02	12		“
T_A = -55°C	$-V_{OP}$	4004	55		15	-15	15	K3	5	E53	V	$-V_{OP}$ = E53	01,02		-10	V
		“	56					K4		E54	“	$-V_{OP}$ = E54	01,02		-12	“
	ΔV_{IO}/ ΔT	4001	28	Fig. 4 4/								ΔV_{IO} / ΔT = (E26 – E44) / 80(1000)	01	-0.6	0.6	µV/°C
													02	-1.3	1.3	
	$A_{VS(+)}$	4004	57		15	-15	-10	K4	4	E55	V	$A_{VS(+)}$ = 10 / (E27 – E55)	01	200		V/mV
													02	150		“
	$A_{VS(-)}$	4004	58		15	-15	10	K4	4	E56	V	$A_{VS(-)}$ = 10 / (E56 – E27)	01	200		V/mV
													02	150		“
7	SR(+)	4002	59	5/ 6/	15	-15	0	K4,K9	5	ΔV_O(+), Δt(+)	V / µs	SR(+) = ΔV_O(+) / Δt(+)	01,02	.08		V/µs
T_A = +25°C	SR(-)	4002	60	5/ 6/	15	-15	0	K4, K9	5	ΔV_O(-), Δt(-)	V / µs	SR(-) = ΔV_O(-) / Δt(-)	01,02	.08		V/µs
	En		61	f_O = 10 Hz						E57	nV / $\sqrt{Hz}$	En = E57	01,02		18	nV / $\sqrt{Hz}$
			62	f_O = 100 Hz						E58		En = E58			14	
			63	f_O = 1 kHz Fig. 5						E59		En = E59			12	
	Enpp		64	Fig. 6						E60	V_{PP}	Enpp = E60 / 50000	01,02		0.6	μV_{PP}

See footnotes at end of table.

TABLE III. Group A inspection for device types 03, 04, and 05.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin number 1	Adapter pin number 2	Adapter pin number 3	Energized relays	Measured pin No.	Measured pin Value	Measured pin Units	Equation	Device type	Limits Min	Limits Max	Unit
1 T_A = +25°C	$+I_{IB}$	4001 "	1 2		15 15	-15 -15	0 0	None K1	4 4	E1 E2	V V	V_{IO} = E1 $+I_{IB}$ = 20 (E1 – E2) $+I_{IB}$ = 2 (E1 – E2) - device type 05	03,04, 05	-40	40	nA "
	$-I_{IB}$	"	3		15	-15	0	K2	4	E3	V	$-I_{IB}$ = 20 (E3 – E1) $-I_{IB}$ = 2 (E3 – E1) - device type 05	03,04, 05	-40	40	" "
	I_{IO}	"	4	2/								I_{IO} = 20 (2E1 – E2 –E3) I_{IO} = 2 (2E1 – E2 –E3) – device type 05	03,04, 05	-35	35	nA
	+PSRR	4003	5		18 5	-15 -15	0 0	None	4	E4 E5	V "	+PSRR = 76.9 (E4 – E5)	03,04, 05	-10	10	µV/V
	-PSRR	4003	6		15 15	-18 -5	0 0	None	4	E6 E7	V "	-PSRR = 76.9 (E6 – E7)	03,04, 05	-10	10	µV/V
	PSRR	4003	7		4.5 18	-4.5 -18	0 0	None	4	E8 E9	V "	PSRR = 37.04 x (E8 - E9)	03,04, 05	-10	10	µV/V
	CMRR	4003	8		26 4	-4 -26	-11 11	None	4	E10 E11	V "	CMRR = 20 log |22000/(E11 – E10)|	03,04, 05	114		dB
	V_{IO} ADJ(+)		9		15	-15	0	K5	4	E12	"	V_{IO} ADJ(+) = E1 – E12	03,04, 05	0.5		mV
	V_{IO} ADJ(-)		10		15	-15	0	K5,K6	4	E13	"	V_{IO} ADJ(-) = E1 – E13	03,04, 05		-0.5	mV
	$I_{OS(+)}$	3011	11	3/	15	-15	-10	None	5	I1	mA	$I_{OS(+)}$ = I1	03,05 04	-70 -60		mA
	$I_{OS(-)}$	3011	12	3/	15	-15	10	None	5	I2	mA	$I_{OS(-)}$ = I2	03,04,05		70	mA
	I_{CC}	4005	13		15	-15	0	None	1	I3	mA	I_{CC} = I3	03,04,05		5	mA
2 T_A = +125°C	V_{IO}	4001	14	Fig. 4	15	-15	0			E14	V	V_{IO} = E14/1000	03,05 04	-60 -180	60 180	µV "
	$+I_{IB}$	4001 "	16 17		15 15	-15 -15	0 0	None K1	4 4	E15 E16	" "	V_{IO} = E15 $+I_{IB}$ = 20 (E15 – E16) $+I_{IB}$ = 2 (E15 – E16) – device type 05	03,04, 05	-60	60	nA "
	$-I_{IB}$	" "	18		15	-15	0	K2	"	E17	"	$-I_{IB}$ = 20 (E17 – E15) $-I_{IB}$ = 2 (E17 – E15) – device type 05	03,04, 05	-60	60	" "
	I_{IO}	"	19	2/								I_{IO} = 20 (2E15 – E16 –E17) I_{IO} = 2 (2E15 – E16 –E17) – device type 05	03,04, 05	-50	50	nA
	+PSRR	4003	20		18 5	-15 -15	0 0	None	4	E18 E19	V "	+PSRR = 76.9 (E18 – E19)	03,04, 05	-16	16	µV/V
	-PSRR	4003	21		15 15	-18 -5	0 0	None	4	E20 E21	V "	-PSRR = 76.9 (E20 – E21)	03,04, 05	-16	16	µV/V
	PSRR	4003	22		4.5 18	-4.5 -18	0 0	None	4	E22 E23	V "	PSRR = 37.04 x (E22 – E23)	03,04, 05	-16	16	µV/V
	CMRR	4003	23		25 5	-5 -25	-10 10	None	4	E24 E25	V "	CMRR = 20 log |20000/(E24 – E25)|	03,04, 05	108		dB

See footnotes at end of table.

TABLE III. Group A inspection for device types 03, 04, and 05 – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin number			Energized relays	Measured pin			Equation	Device type	Limits		Unit
				1/	1	2	3		No.	Value	Units			Min	Max	
2 T_A = +125°C	$I_{OS(+)}$	3011	24	3/	15	-15	-10	None	5	I4	mA	$I_{OS(+)}$ = I4	03,05 04	-70 -60		mA
	$I_{OS(-)}$	3011	25	3/	15	-15	10	None	5	I5	mA	$I_{OS(-)}$ = I5	03,04,05		70	mA
	I_{CC}	4005	26		15	-15	0	None	1	I6	mA	I_{CC} = I6	03,04,05		6	mA
3 T_A = -55°C	V_{IO}	4001 “	27	Fig. 4	15	-15	0			E26	V	V_{IO} = E26/1000	03,05 04	-60 -180	60 180	µV “
	$+I_{IB}$	4001 “	29 30		15 15	-15 -15	0 0	None K1	4 “	E27 E28	“ “	V_{IO} = E27 $+I_{IB}$ = 20 (E27 – E28) $+I_{IB}$ = 2 (E27 – E28) – device type 05	03,04, 05	-60	60	nA “
	$-I_{IB}$	“ “	31		15	-15	0	K2	“	E29	“	$-I_{IB}$ = 20 (E29 – E27) $-I_{IB}$ = 2 (E29 – E27) – device type 05	03,04, 05	-60	60	“ “
	I_{IO}	4001	32	2/								I_{IO} = 20 (2E27 – E28 –E29) I_{IO} = 2 (2E27 – E28 –E29) – device type 05	03,04, 05	-50	50	nA
	+PSRR	4003	33		18 5	-15 -15	0 0	None	4	E30 E31	V “	+PSRR = 76.9 (E30 – E31)	03,04, 05	-16	16	µV/V
	-PSRR	4003	34		15 15	-18 -5	0 0	None	4	E32 E33	V “	-PSRR = 76.9 (E32 – E33)	03,04, 05	-16	16	µV/V
	PSRR	4003	35		4.5 18	-4.5 -18	0 0	None	4	E34 E35	V “	PSRR = 37.04 x (E34 – E35)	03,04, 05	-16	16	µV/V
	CMRR	4003	36		25 5	-5 -25	-10 10	None	4	E36 E37	V “	CMRR = 20 log |20000/(E36 – E37)|	03,04, 05	108		dB
	$I_{OS(+)}$	3011	37	3/	15	-15	-10	None	5	I7	mA	$I_{OS(+)}$ = I7	03,05 04	-70 -60		mA
	$I_{OS(-)}$	3011	38	3/	15	-15	10	None	5	I8	mA	$I_{OS(-)}$ = I8	03,04,05		70	mA
	I_{CC}	3005	39		15	-15	0	None	1	I9	mA	I_{CC} = I9	03,04,05		6	mA
4 T_A = +25°C	$+V_{OP}$	4004	40 41		15	-15	-15	K7 K4	5	E38 E39	V V	$+V_{OP}$ = E38 $+V_{OP}$ = E39	03,04, 05	10 11.5		V “
	$-V_{OP}$	4004	42 43		15	-15	15	K7 K4	5	E40 E41	V V	$-V_{OP}$ = E40 $-V_{OP}$ = E41	03,04, 05		-10 -11.5	“ “
	$A_{VS}(+)$	4004	44		15	-15	-10	K4	4	E42	V	$A_{VS}(+)$ = 10/(E1 – E42)	03,04, 05	1000		V/mV
	$A_{VS}(-)$	4004	45		15	-15	10	K4	4	E43	V	$A_{VS}(-)$ = 10/(E43 – E2)	03,04, 05	1000		V/mV
	V_{IO}	4001	46	Fig. 4	15	-15	0			E44	V	V_{IO} = E44/1000	03,05 04	-25 -80	25 80	µV
5 T_A = +125°C	$+V_{OP}$	4004	47 48		15	-15	-15	K7 K4	5	E45 E46	V V	$+V_{OP}$ = E45 $+V_{OP}$ = E46	03,04, 05	10 11.5		V “
	$-V_{OP}$	4004	49 50		15	-15	15	K7 K4	5	E47 E48	V V	$-V_{OP}$ = E47 $-V_{OP}$ = E48	03,04, 05		-10 -11.5	“ “

See footnotes at end of table.

TABLE III. Group A inspection for device types 03, 04, and 05 – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin number			Energized relays	Measured pin			Equation	Device type	Limits		Unit
				1/	1	2	3		No.	Value	Units			Min	Max	
5	$\Delta V_{IO}/\Delta T$	4001	15	Fig. 4 4/								$\Delta V_{IO} / \Delta T = (E14 - E44)/100(1000)$	03,05 04	-0.6 -1.0	0.6 1.0	µV/°C
T_A = +125°C	$A_{VS}(+)$	4004	51		15	-15	-10	K4	4	E49	V	$A_{VS}(+) = 10/(E15 - E49)$	03,04, 05	600		V/mV
	$A_{VS}(-)$	4004	52		15	-15	10	K4	4	E50	V	$A_{VS}(-) = 10/(E50 - E15)$	03,04, 05	600		V/mV
6	$+V_{OP}$	4004	53 54		15	-15	-15	K7 K4	5	E51 E52	V V	$+V_{OP} = E51$ $+V_{OP} = E52$	03,04, 05	10 11.5		V “
T_A = -55°C	$-V_{OP}$	4004	55 56		15	-15	15	K7 K4	5	E53 E54	V V	$-V_{OP} = E53$ $-V_{OP} = E54$	03,04, 05		-10 -11.5	“ “
	$\Delta V_{IO}/\Delta T$	4001	28	Fig. 4 4/								$\Delta V_{IO} / \Delta T = (E26 - E44) / 100(1000)$	03,05 04	-0.6 -1.0	0.6 1.0	µV/°C
	$A_{VS}(+)$	4004	57		15	-15	-10	K4	4	E55	V	$A_{VS}(+) = 10/(E27 - E55)$	03,04, 05	600		V/mV
	$A_{VS}(-)$	4004	58		15	-15	10	K4	4	E56	V	$A_{VS}(-) = 10/(E56 - E27)$	03,04, 05	600		V/mV
7	SR(+)	4002	59	5/ 6/, 7/	15	-15	0	K4,K9, K10	5	$\Delta V_O(+)$, $\Delta t(+)$	V / µs	$SR(+) = \Delta V_O(+) / \Delta t(+)$	03,04 05	1.7 11		V/µs
T_A = +25°C	SR(-)	4002	60	5/ 6/, 7/	15	-15	0	K4,K9, K10	5	$\Delta V_O(-)$, $\Delta t(-)$	V / µs	$SR(-) = \Delta V_O(-) / \Delta t(-)$	03,04 05	1.7 11		V/µs
	En		61 62 63	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz Fig. 5						E57 E58 E59	nV / $\sqrt{Hz}$	En = E57 En = E58 En = E59	03,05 04 03,05 04 03,05 04		5.5 6.0 4.0 5.0 3.8 3.9	nV / $\sqrt{Hz}$
	Enpp		64	Fig. 6						E60	V_{PP}	Enpp = E60 / 50000	03,05 04		.18 .20	μV_{PP}
9 T_A = +25°C	In		65 66 67	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz Fig. 5						E61 E62 E63	pA / $\sqrt{Hz}$	$In = \{[(E61)^2 - (E57)^2 - (1.64 \times 10^{-15})]\ 10^{-10}\}\ 0.5$ $In = \{[(E62)^2 - (E58)^2 - (1.64 \times 10^{-15})]\ 10^{-10}\}\ 0.5$ $In = \{[(E63)^2 - (E59)^2 - (1.64 \times 10^{-15})]\ 10^{-10}\}\ 0.5$	03,05 04 03,05 04 03,05 04		5.66 5.66 1.88 2.1 0.84 0.89	pA / $\sqrt{Hz}$

1/ All tests apply to figure 3, unless otherwise specified. For devices marked with the “Q” certification mark, the parameters listed herein may be guaranteed if not tested to the limits specified in accordance with the manufacturer’s QM plan,

2/ I_{IO} is calculated using data from previous tests.

3/ $I_{OS}(+)$ and $I_{OS}(-)$ are measured with the output shorted to ground for less than 25 milliseconds.

4/ $\Delta V_{IO} / \Delta t$ is calculated using data from previous tests.

5/ Slew rate can be measured using figure 7. All test signals for figure 3 are shown on figure 7.

6/ The oscillation detector will be disconnected during slew rate tests.

7/ Slew rate: For device types 03 and 04 energize relays K4 and K9. For device type 05 energize relays K4, K9, and K10.

TABLE IV. Group C end point and Group B, class S, electrical parameters.

(V_{CM} = 0, $\pm V_{CC}$ = ±15 V for all device types)
T_A = 25°C for Group C end-point limits, -55°C ≤ T_A ≤ +125°C for Group B, class S, end-point limits.

Test	Device 01				Device 02				Units
	Limit		Delta		Limit		Delta		
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IO}	-135	135	-75	75	-300	300	-100	100	µV
$+I_{IB}$	-5	5	-1	1	-7.5	7.5	-1.5	1.5	nA
$-I_{IB}$	-5	5	-1	1	-7.5	7.5	-1.5	1.5	nA

Test	Devices 03 and 05				Device 04				Units
	Limit		Delta		Limit		Delta		
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IO}	-135	135	-75	75	-280	280	-100	100	µV
$+I_{IB}$	-70	70	-10	10	-70	70	-10	10	nA
$-I_{IB}$	-70	70	-10	10	-70	70	-10	10	nA

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service, or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6.0 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. Pin and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for "JAN" marking.

j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor’s parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, and MIL-HDBK-1331.

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	OP-07A
02	OP-07, 714
03	OP-27A
04	OP-227A
05	OP-37A

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army – CR
Navy - EC
Air Force - 11
NASA - NA
DLA – CC

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force – 03, 19, 99

Preparing activity:
DLA - CC

Project 5962-2121

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.