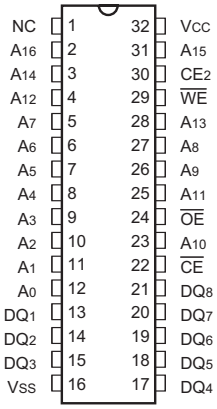
128K x 8 Static RAM

FEATURES

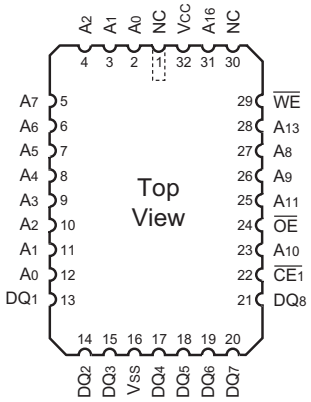
- 128K x 8 Static RAM with Chip Select Powerdown, Output Enable and Single or Dual Chip Selects
- High Speed — to 15 ns maximum
- Operational Power, -L Version
  Active: 140 mA at 15 ns
  Standby: 1 mA max
- Data Retention at 2 V for Battery Backup Operation
- Screened to MIL-STD-883, Class B or to SMD 5962-89598
- Package Styles Available:
  - 32-pin Ceramic 400mil DIP(#D12)
  - 32-pin Ceramic LCC(#K11)
  - 32-pin Ceramic SOJ(#Y1)
  - 32-pin Quad Ceramic LCC(#KA1)

Pin Configuration

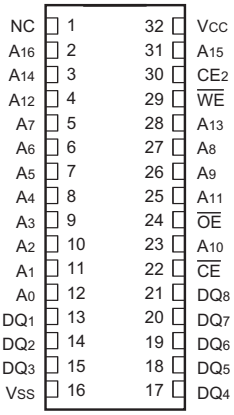
32-pin Ceramic DIP
32-pin Ceramic SOJ



32-pin Quad CLCC



32-pin Ceramic LCC



OVERVIEW

The L7C108 and L7C109 are high-performance, low-power CMOS static RAMs. The storage circuitry is organized as 131,072 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. The L7C108 has a single active-low Chip Enable. The L7C109 has two Chip Enables (one active-low). These devices are available in three speeds with maximum access times from 15 ns to 45 ns.

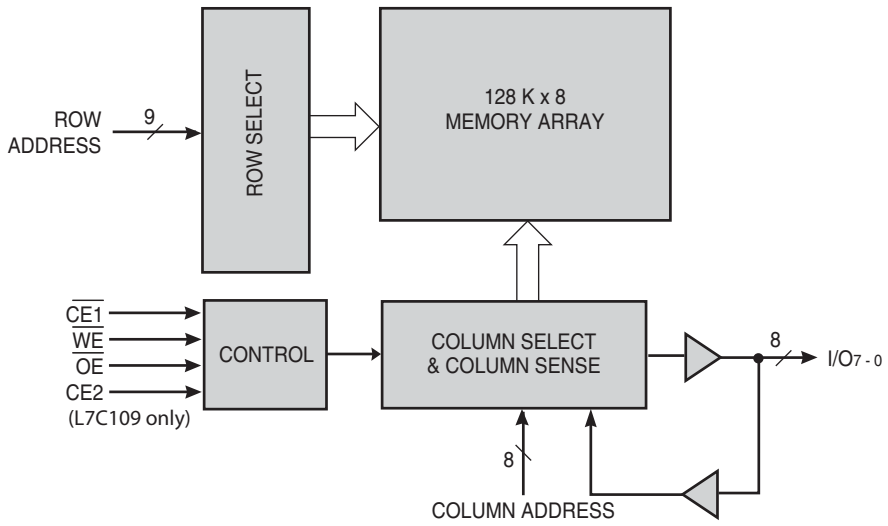
Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 140 mA (-L Version) at 15 ns. Data may be retained in inactive storage with a supply voltage as low as 2 V.

The L7C108 and L7C109 provide asynchronous (unclocked) operation with matching access and cycle times. The Chip Enables and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{16}. For the L7C108, reading from a designated location is accomplished by presenting an address and driving $\overline{CE_1}$ and $\overline{OE}$ LOW while $\overline{WE}$ remains HIGH. For the L7C109, $\overline{CE_1}$ and $\overline{OE}$ must be LOW while CE_2 and $\overline{WE}$ are HIGH.The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE_1}$ or $\overline{OE}$ is HIGH, or CE_2 (L7C109) or $\overline{WE}$ is LOW. Writing to an addressed location is accomplished when the active-low $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, and CE_2 (L7C109) is HIGH. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C108 and L7C109 can withstand an injection current of up to 200 mA on any pin without damage.

L7C108-109 Block Diagram



Truth Table

Mode	$\overline{OE}$	$\overline{CE1}$	CE2*	$\overline{WE}$	DQ	POWER
Standby	X	≥ V_{IH}	X	X	High - Z	Standby (I_{CC2})
Standby	X	X	≤ V_{IL}	X	High - Z	Standby (I_{CC2})
Standby	X	≥ V_{CC} - 0.2 V	X	X	High - Z	Standby (I_{CC3})
Standby	X	X	≤ G_{ND} + 0.2 V	X	High - Z	Standby (I_{CC3})
Read	L	L	H	H	Q	Active
Read	H	L	H	H	High - Z	Active
Write	X	L	H	L	D	Active

* *Note: for L7C109 only*

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature.....-65°C to +150°C
Operating ambient temperature.....-55°C to +125°C
Vcc supply voltage with respect to ground.....-0.5 V to +7.0 V
Input signal with respect to ground.....-3.0 V to +7.0 V
Signal applied to high impedance output.....-3.0 V to +7.0 V
Output current into low outputs.....25 mA
Latchup current.....>200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active, Operation, Military	-55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	L7C108/109 Min	L7C108/109 Max	L7C108/109-L Min	L7C108/109-L Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5V, I_{OH} = -4 mA	2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	-0.5	0.8	-3.0	0.8	V
I_{Ix}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	-10	+10	-10	+10	µA
I_{CC2}	V_{CC} Current, TTL Standby	(Note 7)		25		25	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		10		5	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 2 V (Notes 9, 10)		-		0.75	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5 V		8		8	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)		8		8	pF

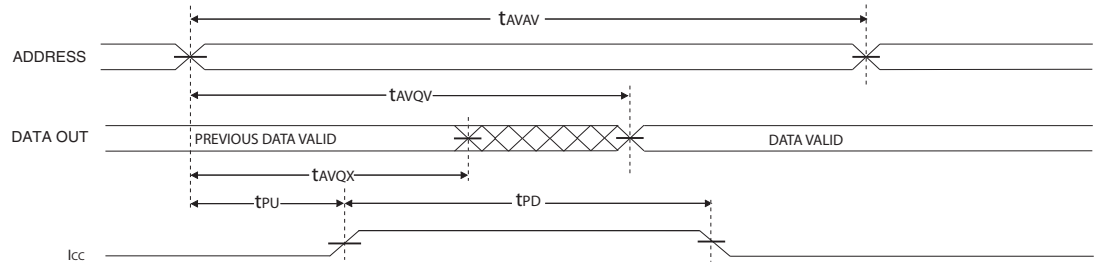
Symbol	Parameter	Test Condition	L7C108/109 15	20	25	35	45	L7C108/109-L 15	20	25	35	45	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	140	140	140	135	125	140	140	140	130	125	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

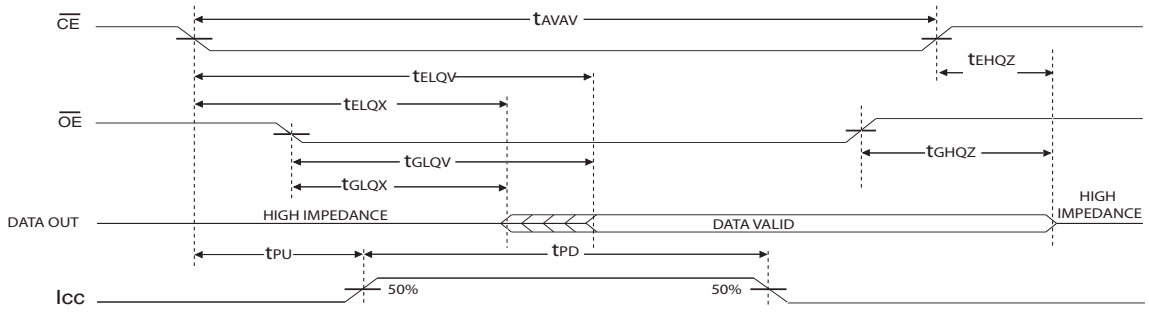
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C108/109									
		15/15-L		20/20-L		25/25-L		35/35-L		45/45-L	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	15		20		25		35		45	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		15		20		25		35		45
t_{AVQX}	Address Change to Output Change	3		3		3		3		3	
t_{ELQV}	Chip Enable Low to Output Valid (Notes 13, 15)		15		20		25		35		45
t_{ELQX}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
t_{EHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		7		8		10		15		20
t_{GLQV}	Output Enable Low to Output Valid		8		10		10		15		20
t_{GLQX}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{GHQZ}	Output Enable High to Output High Z (Notes 20, 21)		6		6		10		15		20
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0		0	

READ CYCLE - ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE - $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*

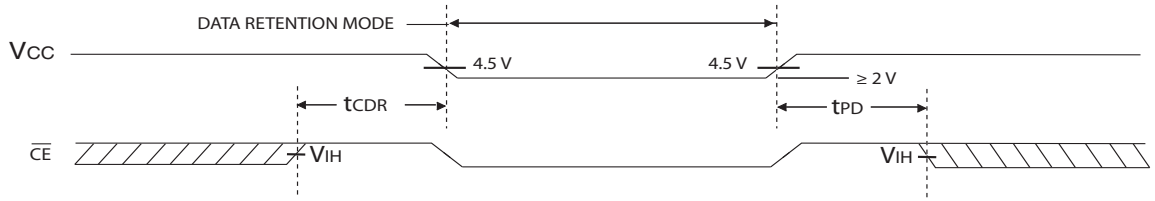


SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L7C108/109									
		15/15-L		20/20-L		25/25-L		35/35-L		45/45-L	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{PD}	Operation Recovery Time (Notes 10, 19)		15		20		25		35		45
t_{CDR}	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

DATA RETENTION *Notes 9, 10*

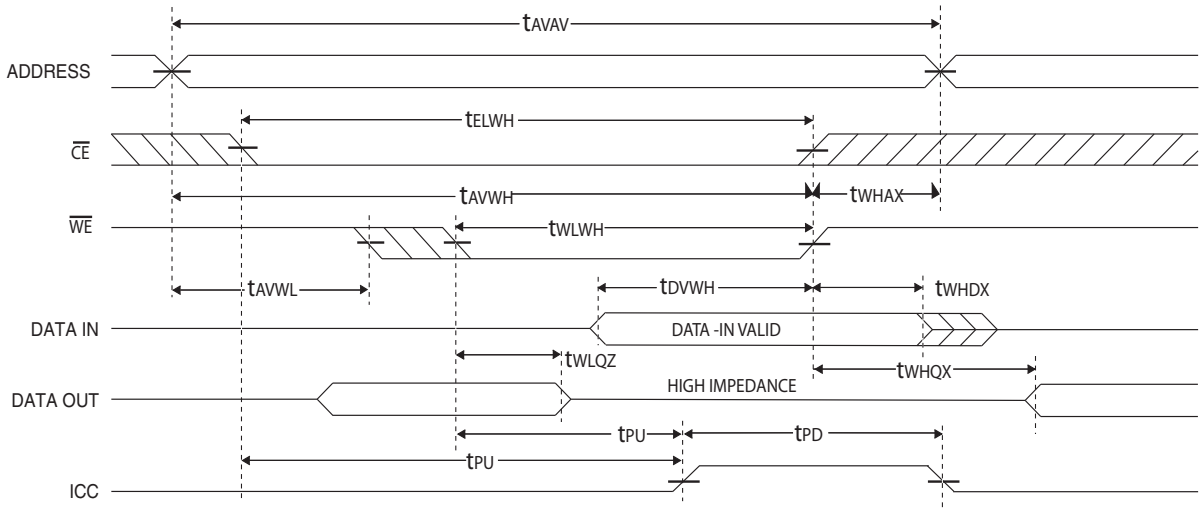


WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

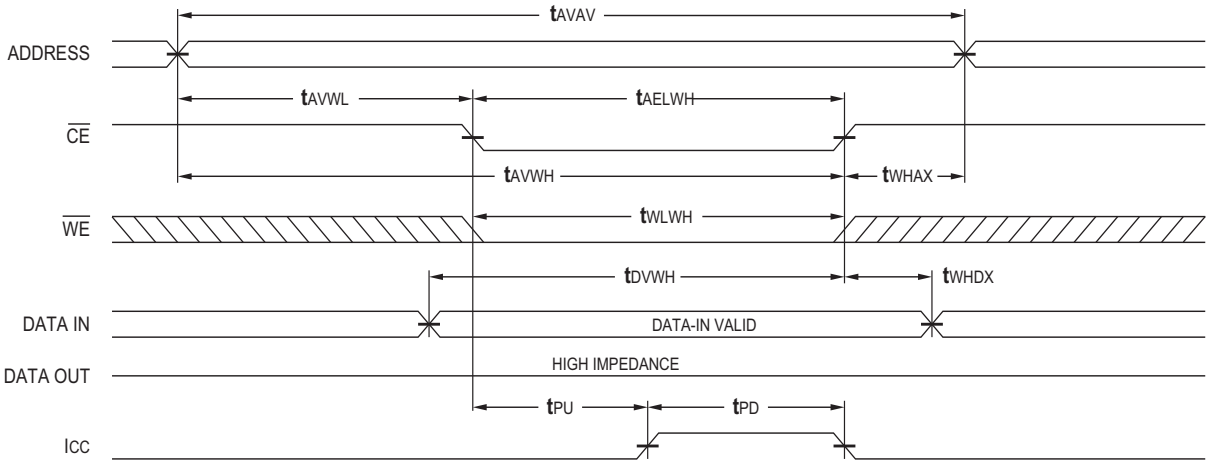
Symbol	Parameter	L7C108/109									
		15/15-L		20/20-L		25/25-L		35/35-L		45/45-L	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	15		20		25		35		45	
t_{ELWH}	Chip Enable Low to End of Write Cycle	12		12		20		25		35	
t_{AVWL}	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
t_{AVWH}	Address Setup to End of Write Cycle	15		17		20		25		35	
t_{WHAX}	Address Hold After End Of Write	0		0		0		0		0	
t_{WLWH}	Write Enable Pulse Width Low	12		15		20		30		40	
t_{DVWH}	Data Setup to End of Write Cycle	7		10		12		20		20	
t_{WHDX}	Data Hold to End of Write	0		0		0		0		0	
t_{WHQX}	Write Enable High to Output Low Z (Notes 20, 21)	5		5		5		5		5	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		8		10		25		30

SWITCHING CHARACTERISTICS *Over Operating Range*

WRITE CYCLE - $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*

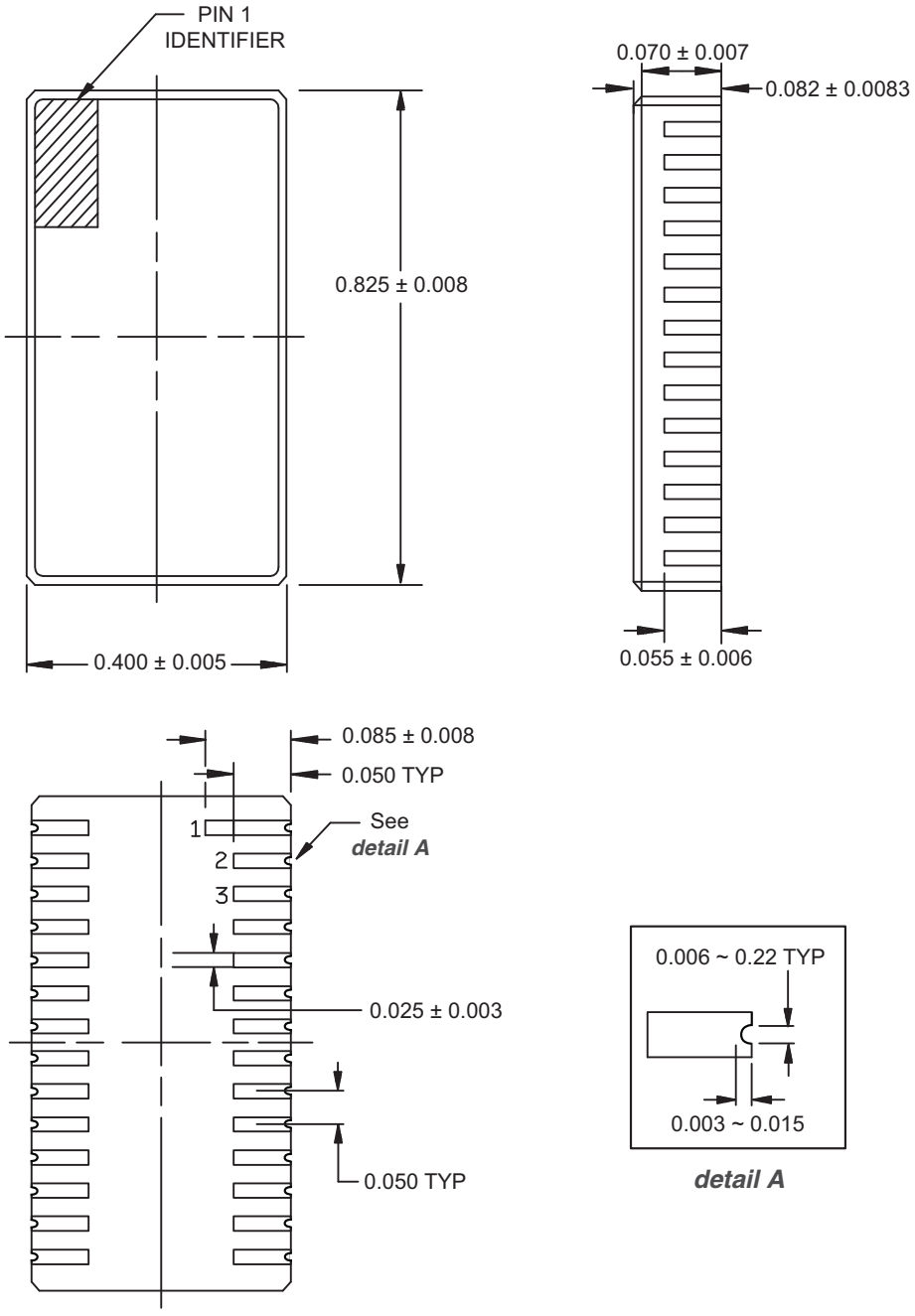


WRITE CYCLE - $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



PACKAGE INFORMATION

PKG K: 32L Ceramic Dual LCC (MD-K11)

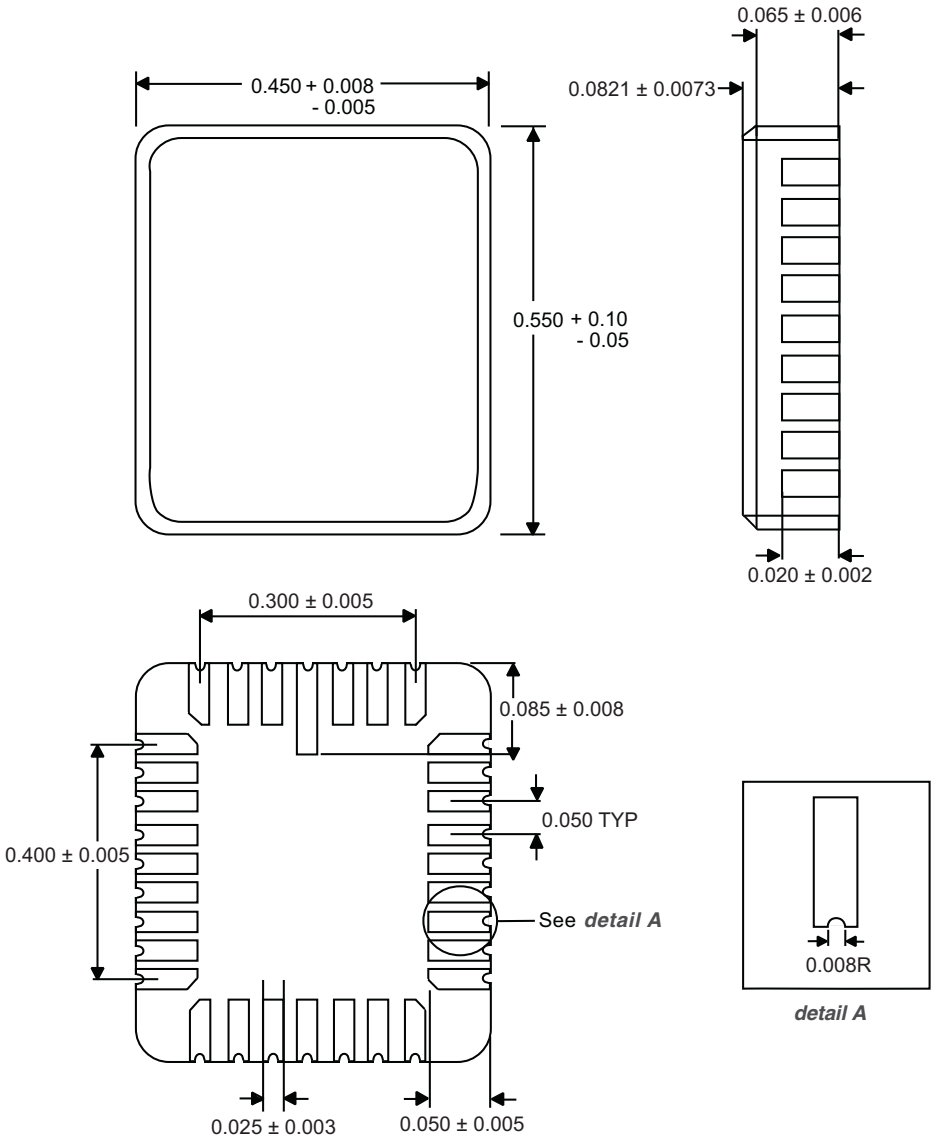


SMD 5962-89598 Case 'U' / Ordering Code 'K'

**All measurements in inches*

PACKAGE INFORMATION

PKG KA: 32L CERAMIC QUAD LCC (MD-KA1)

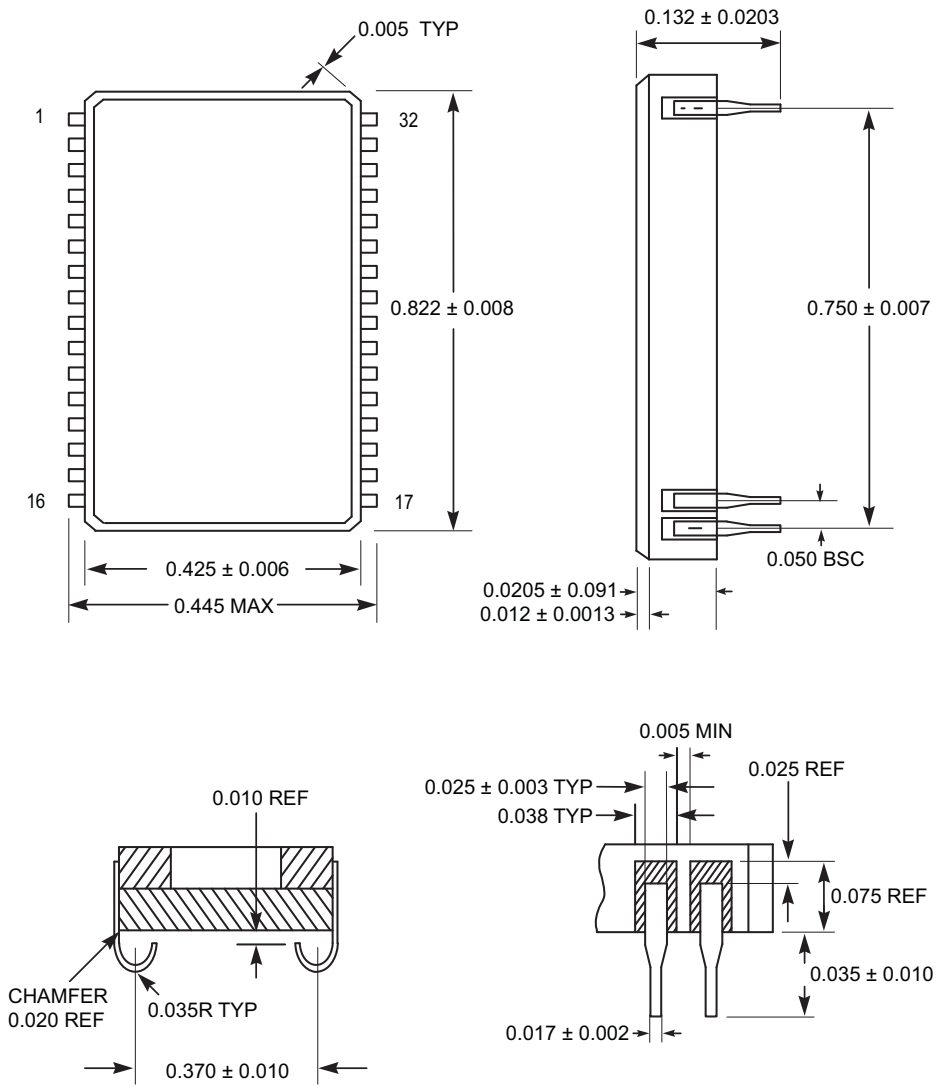


SMD 5962-89598 Case 'M' / Ordering Code "KA"

*All measurements in inches

PACKAGE INFORMATION

PKG Y: 32L CERAMIC SOJ (MD-Y1)



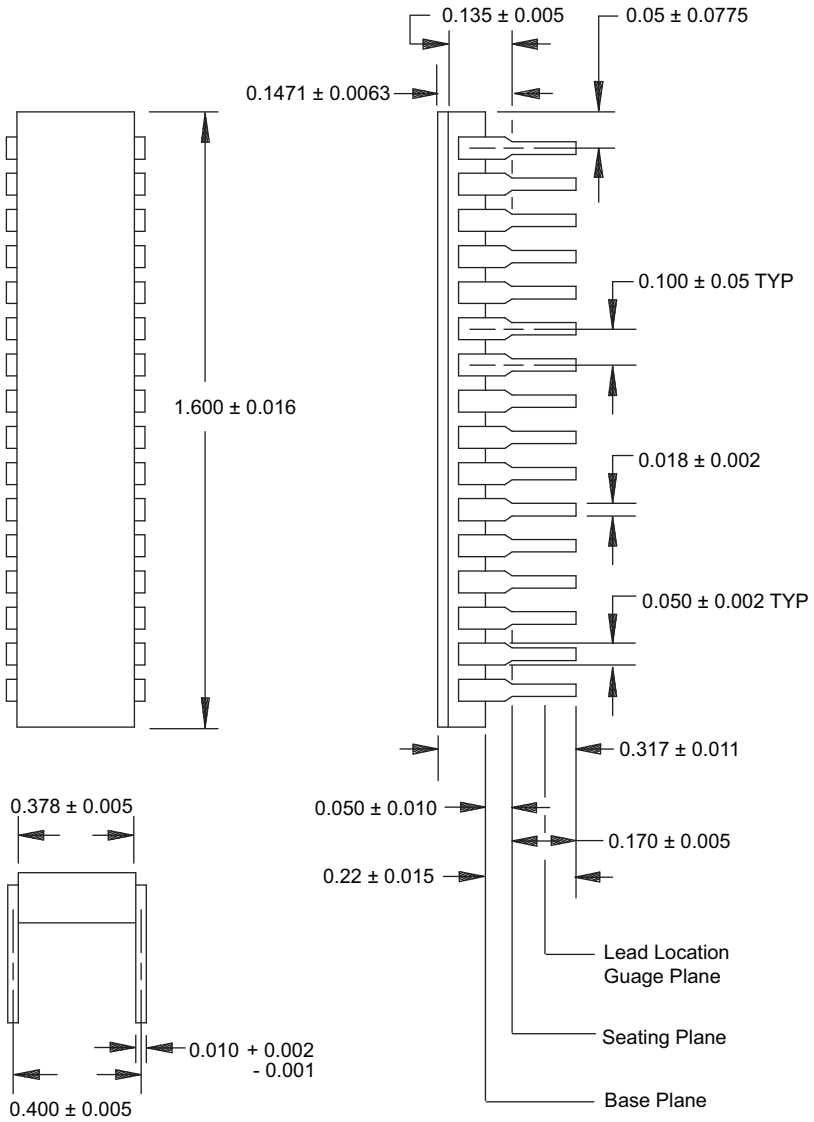
(Note: Case 'Y' ships for Case '7' as compatible replacement)

SMD 5962-89598 Case 'Y' and '7' / Ordering Code 'Y'

**All measurements in inches*

PACKAGE INFORMATION

PKG D: 32L CERAMIC DIP (MD-D12)



SMD 5962-89598 Case 'Z' / Ordering Code 'D'

**All measurements in inches*

SMD Cross Reference Table

LOGIC Part #	SMD Part #
L7C109DMB45	5962-8959835MZA
L7C109DMB35	5962-8959836MZA
L7C109DMB25	5962-8959837MZA
L7C109DMB20	5962-8959838MZA
L7C109DMB15	5962-8959841MZA
L7C109YMB45	5962-8959835M7A
L7C109YMB35	5962-8959836M7A
L7C109YMB25	5962-8959837M7A
L7C109YMB20	5962-8959838M7A
L7C109YMB15	5962-8959841M7A
L7C109YMB45	5962-8959835MYA
L7C109YMB35	5962-8959836MYA
L7C109YMB25	5962-8959837MYA
L7C109YMB20	5962-8959838MYA
L7C109YMB15	5962-8959841MYA
L7C109KAMB45	5962-8959835MMA
L7C109KAMB35	5962-8959836MMA
L7C109KAMB25	5962-8959837MMA
L7C109KAMB20	5962-8959838MMA
L7C109KAMB15	5962-8959841MMA
L7C109KMB45	5962-8959835MUA
L7C109KMB35	5962-8959836MUA
L7C109KMB25	5962-8959837MUA
L7C109KMB20	5962-8959838MUA
L7C109KMB15	5962-8959841MUA

LOGIC Part #	SMD Part #
L7C108DMB45	5962-8959827MZA
L7C108DMB35	5962-8959828MZA
L7C108DMB25	5962-8959829MZA
L7C108DMB20	5962-8959839MZA
L7C108DMB15	5962-8959844MZA
L7C108YMB45	5962-8959827M7A
L7C108YMB35	5962-8959828M7A
L7C108YMB25	5962-8959829M7A
L7C108YMB20	5962-8959839M7A
L7C108YMB15	5962-8959844M7A
L7C108YMB45	5962-8959827MYA
L7C108YMB35	5962-8959828MYA
L7C108YMB25	5962-8959829MYA
L7C108YMB20	5962-8959839MYA
L7C108YMB15	5962-8959844MYA

SMD Cross Reference Table

LOGIC Part #	SMD Part #
L7C109DMB45L	5962-8959818MZA
L7C109DMB35L	5962-8959819MZA
L7C109DMB25L	5962-8959820MZA
L7C109DMB20L	5962-8959821MZA
L7C109YMB45L	5962-8959818M7A
L7C109YMB35L	5962-8959819M7A
L7C109YMB25L	5962-8959820M7A
L7C109YMB20L	5962-8959821M7A
L7C109YMB45L	5962-8959818MYA
L7C109YMB35L	5962-8959819MYA
L7C109YMB25L	5962-8959820MYA
L7C109YMB20L	5962-8959821MYA
L7C109KAMB45L	5962-8959818MMA
L7C109KAMB35L	5962-8959819MMA
L7C109KAMB25L	5962-8959820MMA
L7C109KAMB20L	5962-8959821MMA
L7C109KMB45L	5962-8959818MUA
L7C109KMB35L	5962-8959819MUA
L7C109KMB25L	5962-8959820MUA
L7C109KMB20L	5962-8959821MUA
L7C109FMB20L	5962-8959821MTA
L7C108DMB45L	5962-8959810MZA
L7C108DMB35L	5962-8959811MZA
L7C108DMB25L	5962-8959812MZA
L7C108DMB20L	5962-8959840MZA
L7C108DMB15L	5962-8959848MZA

LOGIC Part #	SMD Part #
L7C108YMB45L	5962-8959810M7A
L7C108YMB35L	5962-8959811M7A
L7C108YMB25L	5962-8959812M7A
L7C108YMB20L	5962-8959840M7A
L7C108YMB15L	5962-8959848M7A
L7C108YAMB45L	5962-8959810MYA
L7C108YMB35L	5962-8959811MYA
L7C108YMB25L	5962-8959812MYA
L7C108YMB20L	5962-8959840MYA
L7C108YMB15L	5962-8959848MYA

ORDERING INFORMATION

L 7C 108 D M B 15 L

Indicates a LOGIC Devices product

SRAM

PART NUMBER:
108 = 1M SRAM with single chip enable (available in packages 'D' and 'Y')
109 = 1M SRAM with dual chip enables (available in ALL packages)

PACKAGE CODE:
D = 32 pin Sidebrazed DIP 400mil
K = 32 pin Ceramic LCC
KA = 32 pin Quad Ceramic LCC
Y = 32 pin Ceramic SOJ

SCREENING LEVEL:
M = Military Temperature, -55°C to +125°C
E = Extended Temperature, -40°C to +105°C
I = Industrial Temperature, -40°C to +85°C

COMPLIANCE:
B = MIL-STD-883 Compliant

SPEED GRADE:
[M]: 15/20/25/35/45
[E]: 15/20/25/35/45
[I]: 15/20/25/35/45

LOW POWER OPTION:
L = Low Power
No Mark Means Standard Power

Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE_1}$ = V_{CC}, CE_2 = GND.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for reading, i.e., $\overline{CE_1}$ ≤ V_{IL}, CE_2 ≥ V_{IH}, $\overline{WE}$ ≥ V_{IH}, with outputs disabled, $\overline{OE}$ ≥ V_{IH}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE_1}$ ≥ V_{IH}, CE_2 ≤ V_{IL}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e. $\overline{CE_1}$ = V_{CC}, CE_2 = GND. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0V. $\overline{CE_1}$ must be ≥ V_{CC} - 0.2 V or CE_2 must be ≤ 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} - 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE_1}$, CE_2, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE_1}$ low, CE_2 high).

15. All address lines are valid prior-to or coincident-with the $\overline{CE_1}$ and CE_2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE_1}$ and CE_2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE_1}$ and CE_2 going active, the output remains in a high impedance state.

18. If $\overline{CE_1}$ and CE_2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Rising edge of CE_2 ($\overline{CE_1}$ active) or the falling edge of $\overline{CE_1}$ (CE_2 active).

b. Falling edge of $\overline{WE}$ ($\overline{CE_1}$, CE_2 active).

c. Transition on any address line ($\overline{CE_1}$, CE2, active).

d. Transition on any data line ($\overline{CE_1}$, CE_2, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE_1}$, CE_2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

Figure 1a.

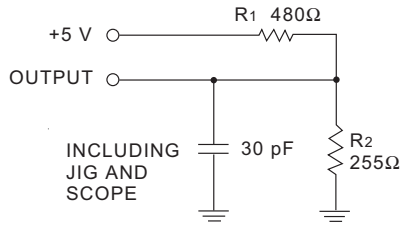


Figure 1b.

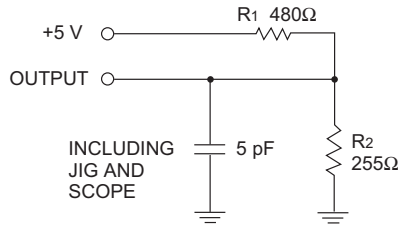
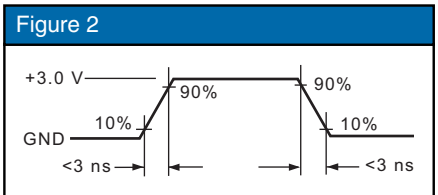


Figure 2



Revision History L7C108/L7C109

Revision	Engineer	Issue Date	Description Of Change
A	COM	10/8/2008	Initial Release
B	JM	10/30/2008	Datasheet Format Revision
C	DH/JM	07/02/2009	Updated specs: 1. Added 10ns & 12 speed columns in ICC1 table 2. Added 10ns speed and AC specs in the AC table 3. Updated all DC power specs in DC table 4. Corrected symbol names in AC and Timing diagrams 5. Added speed bin to ordering info table 6. Removed commercial temp offering 7. Added an extended temp offering
D	DH	06/11/10	Revisions: 1. Removed 10 & 12ns bins 2. Removed 32LD FP (to be re-introduced wiht our silicon, if market warrants) 3. Removed SOJ package variant “YA” 4. Add notation for SMD 5962-89598 that Package ‘Y’ will be supplied as a “7” compatible package 5. Increased ICC1, ICC2, and ICC4@2V for standard power 6. Increased ICC2 and ICC4@2V for low power 7. Removed appropriate DSCC and LOGIC part numbers from ordering tables and PN generator 8. Modified LOGIC Devices “YA” package reference to ‘Y’ 9. Corrections to package dimensions for MD-K11 and MD-Y1
E	JM	07/30/10	Updated mechanical drawings for all packages
F	DH	08/11/10	Revisions: 1. Removed all 108 KA (quad LCC) and K (dual LCC) package variants from SMD cross reference table. 2. Updated order information chart to reflect current package availabilities. 3. Changed ICC2 conditions to match ICC3 conditions. 4. Changed operating current to be calculated during the READ cycle.