mosaic

Mosaic Semiconductor Inc.

256K x 1 SRAM

MSM1256T/V-25/35

Issue 1.2 : April1991

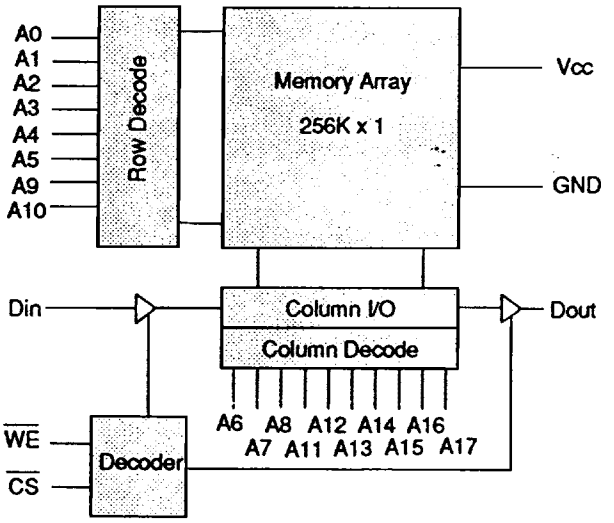
ADVANCE PRODUCT INFORMATION

262,144 x 1 BiCMOS High Speed Static RAM

Features

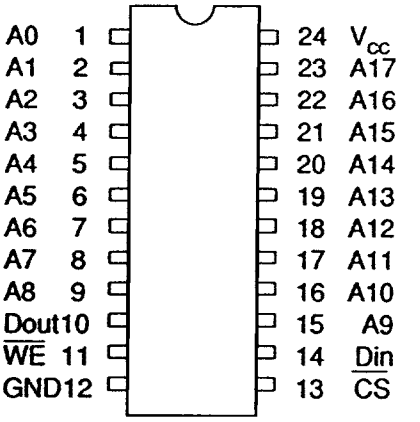
Very Fast Access Times of 25/35 ns
Standard 24 pin Dual-in-Line Package
Low Power Standby - 50 mW
Low Power Operation - 500 mW
Completely Static Operation
Equal Access and Cycle Times
Directly TTL compatible
Common data inputs & outputs
May be Processed to MIL-STD-883C (suffix MB)

Block Diagram



Pin Definitions

Package Type: 'T','V'



Pin Functions

A0-A17	Address inputs
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{cc}	Power(+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
24	0.3" Dual-in-Line (DIL)	T	Ceramic	JEDEC
24	0.1" Vertical-in-Line (VIL)	V	Ceramic	JEDEC

Package details and dimensions on page 5.

Absolute Maximum Ratings

Input Voltage on any pin	V_T	-0.5* to +7	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

*Note: V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	$V_{I/O}$	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-3.0 *	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (1256I)
	T_{AM}	-55	-	125	°C (1256M,MB)

*Pulse Width less than 20nS, V_{CC}, V_{IN}, V_{OUT} min = -0.5V

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{IL}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} $V_{I/O}$=Gnd to V_{CC}	-	-	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT} =0mA, V_{IN}=V_{IH} / V_{IL}	-	-	100	mA
Average Power Supply Current	I_{CC1}	Min. Cycle,duty=100%, I_{OUT} =0mA	-	-	120	mA
Standby Current	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	-	-	10	mA
	I_{SB2}	$\overline{CS}$=V_{IH}	-	-	30	mA
Output High Voltage	V_{OH}	I_{OH}=-4.0 mA	2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}=8.0 mA	-	-	0.4	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (f=1 MHz, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} =0V	-	6	pF
Output Capacitance:	C_{OUT}	V_{OUT}=0V	-	10	pF

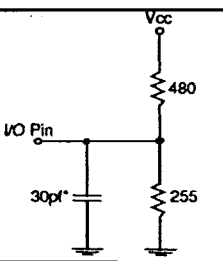
Note: This parameter is sampled and not 100% tested.

AC Test Conditions (V_{CC}=5V±10%, T_A=-55 to 125 °C)

* Input pulse high level V_{IH}=3.0V
* Input pulse low level V_{IL}=0V
* Input rise time t_R=5 nS
* Input fall times t_F=5 nS
* Input and output timing reference level 1.5V
  Output load (see fig.1.)

Output Load Diagram

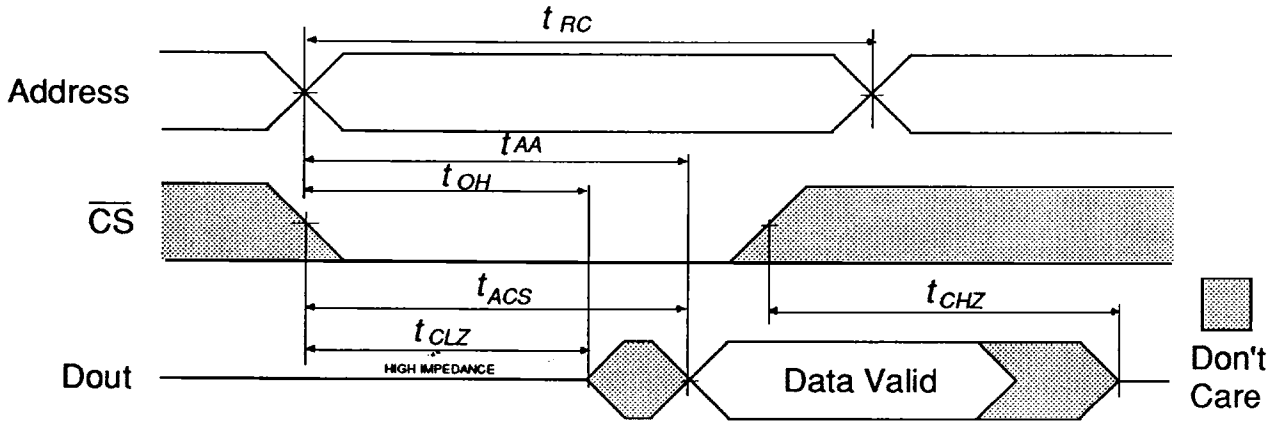
*Including scope and jig capacitance



Electrical Characteristics & Recommended AC Operating Conditions

Parameter	Symbol	-25 min	-25 max	-35 min	-35 max	Unit
Read Cycle Time	t_{RC}	25	-	35	-	ns
Address Access Time	t_{AA}	-	25	-	35	ns
Chip Select Access Time	t_{ACS}	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Chip Select to Output in Low Z	t_{CLZ}	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	15	ns

Read Cycle Timing Waveform (1)



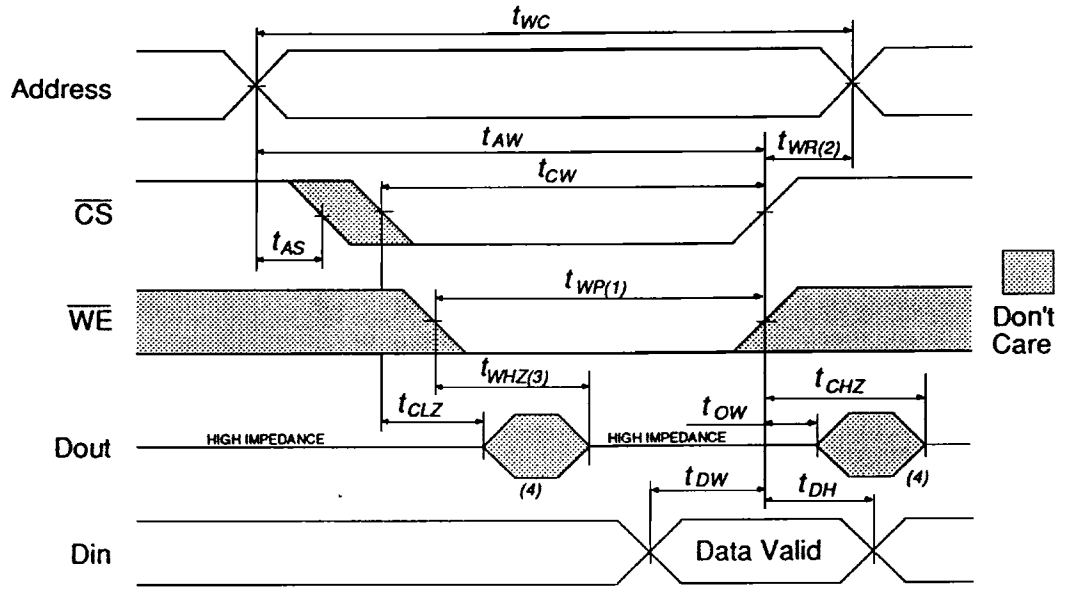
Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

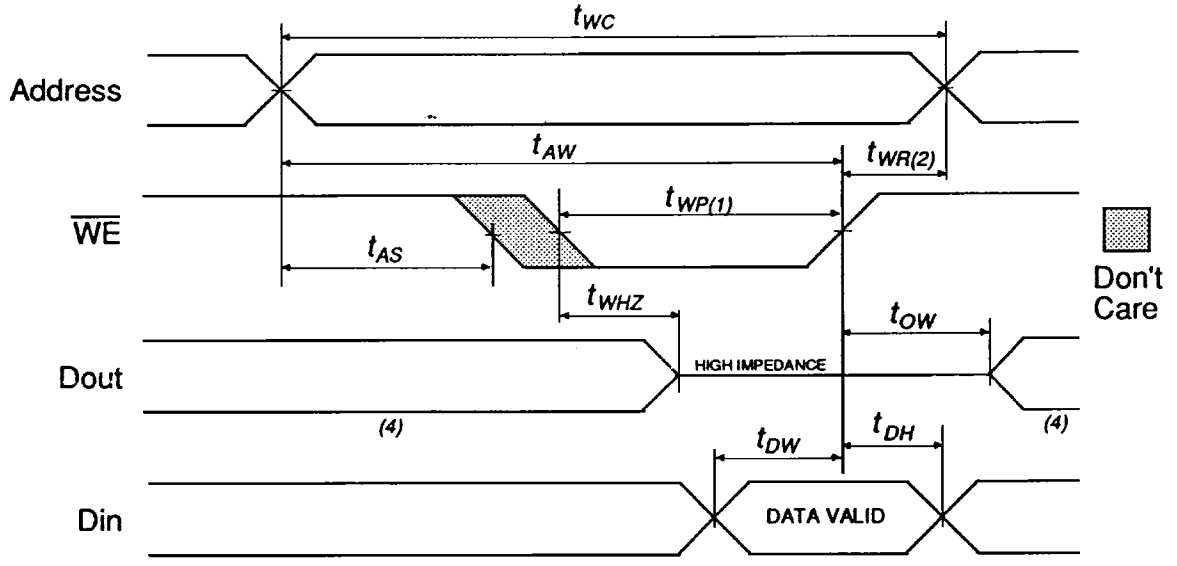
Parameter	Symbol	-25 min	-25 max	-35 min	-35 max	Unit
Write Cycle Time	t_{WC}	25	-	35	-	ns
Chip Selection to End of Write	t_{CW}	20	-	30	-	ns
Address Valid to End of Write	t_{AW}	20	-	30	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	20	-	30	-	ns
Write Recovery Time	t_{WR}	3	-	3	-	ns
Write to Output in High Z	t_{WHZ}*	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	0	-	0	-	ns

*Note:this parameter is sampled and not 100% tested.

Write Cycle No.1 Timing Waveform ($\overline{CS}$ Controlled)



Write Cycle No.2 Timing Waveform ($\overline{CE}$ = V_{IL})($\overline{WE}$ Controlled)

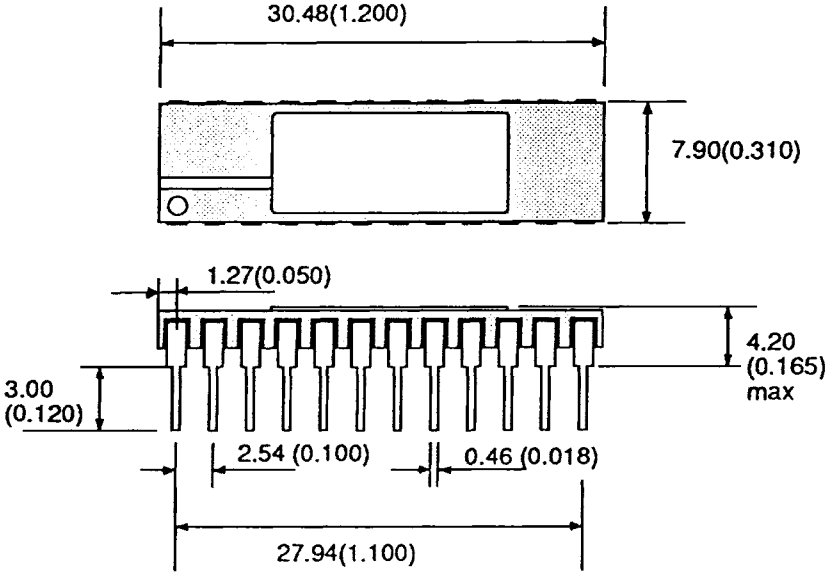


Notes:

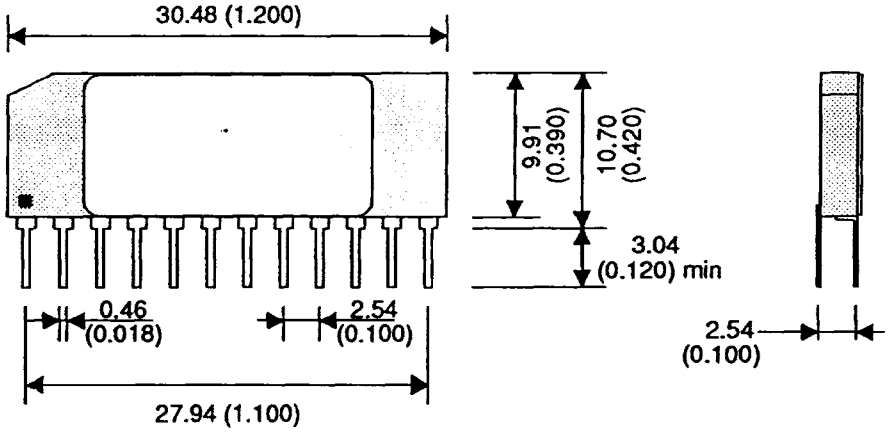
1. A write occurs during the low overlap of $\overline{CS}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
4. At any conditions, t_{CHZ} is less than t_{CLZ}.

Package Details Dimensions in mm (inches). Tolerance on all dimensions ±0.254(0.010).

24 Pin DIL ('T' Package)



24 Pin Vertical In line ('V' Package)



Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ +150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM1256T MB-25

Speed	25,35 ns	
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL STD 883C
Power Consumption	Blank	= Standard Part
Package	T	= 24 Pin 0.3" Dual-in-Line
	V	= 24 Pin 0.1" Vertical-in-Line

mosaic
Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058