Frequency Synthesizer for Radio Tuning

Description

The U4256BM is a single chip frequency synthesizer in BICMOS technology. Together with the AM/FM IC U4255BM, it performs a complete AM/FM car radio front end, which is recommended also for RDS (Radio Data System) applications. It is controlled by 3-wire bus and contains also Digital to Analog Converters (DACs) for automatic alignment of the AM/FM tuner.

Features

- Reference oscillator up to 15 MHz (tuned)
- Oscillator buffer output (for AM up/down conversion)
- Two programmable 16-bit dividers
- Fine-tuning steps: AM ≥ 1 kHz, FM ≥ 2 kHz
- Fast response time due to integrated loop push-pull stage
- 3-wire bus (enable, clock and data; 3 V and 5 V micro-controllers acceptable)
- Four programmable switching outputs (open drain)
- Three DACs for software controlled tuner alignment
- Low power consumption
- High S/N ratio
- Integrated band gap − only one supply voltage necessary

Block Diagram

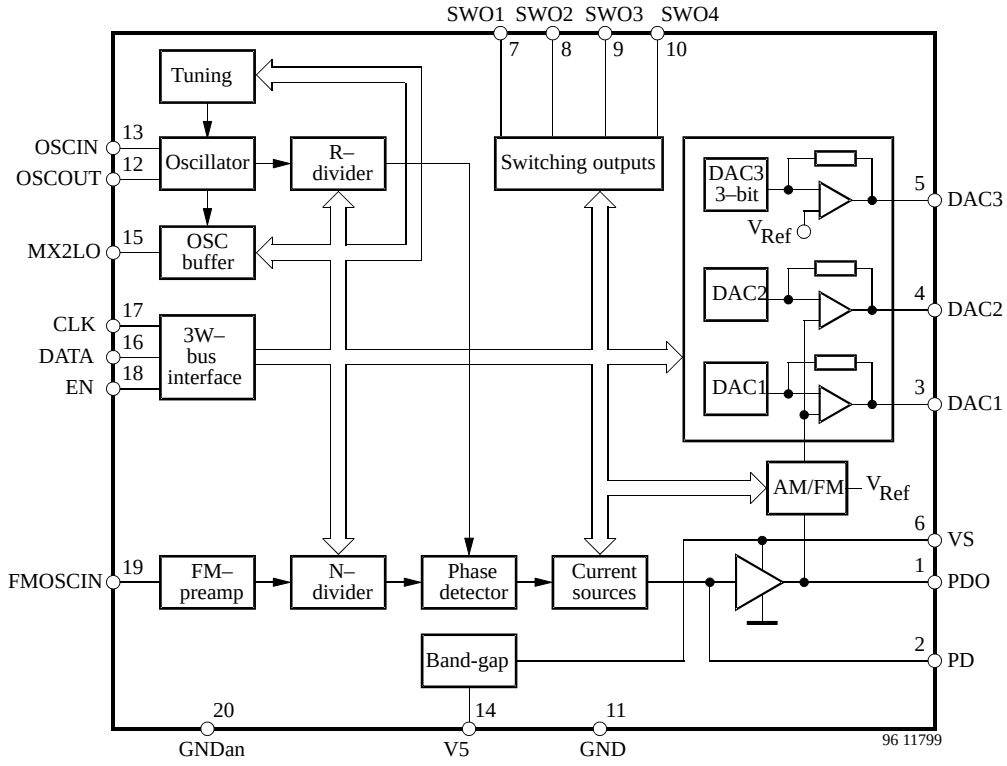


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U4256BM-AFS	SSO20	
U4256BM-AFSG3	SSO20	Taped and reeled

Preliminary Information

Pin Description

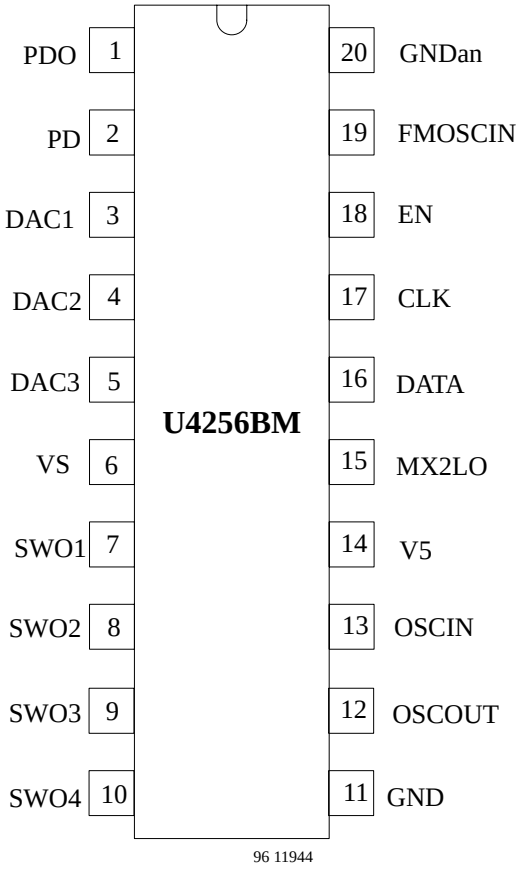


Figure 2. Pinning

Pin	Symbol	Function
1	PDO	Analog output
2	PD	Current output
3	DAC1	Output 1, digital to analog converter
4	DAC2	Output 2, digital to analog converter
5	DAC3	Output 3, digital to analog converter
6	VS	Supply voltage analog part
7	SWO1	Switching output 1
8	SWO2	Switching output 2
9	SWO3	Switching output 3
10	SWO4	Switching output 4
11	GND	Ground, digital part
12	OSCOUT	Oscillator output
13	OSCIN	Oscillator input
14	V5	Capacitor band gap
15	MX2LO	Oscillator buffer output
16	DATA	Data input
17	CLK	Clock
18	EN	Enable
19	FMOSCIN	FM-oscillator input
20	GNDan	Ground, analog part

Circuit Description

The U4256BM is a single chip PLL circuit, designed for AM/FM RDS (Radio Data System) applications. The special design allows to build automatic alignment tuner systems. Two programmable DACs (Digital to Analog Converter) support the computer controlled alignment.

The U4256BM has a very fast response time of maximum 800 µs (at 2 mA, fref = 100 kHz, measured on MPX signal). It performs a high signal to noise ratio.

Only one supply voltage is necessary, due to a integrated band gap.

The U4256BM is controlled via 3-wire bus.

Functional Description

The U4256BM is especially designed for AM up/down converter systems, together with the tuner U4255BM. Due to the integrated DACs, an automatic tuner alignment is possible. All the functions of the U4256BM can be software controlled via a serial 3-wire bus, consisting of Enable, Clock and Data. The format and procedure for the data transfer from the microcontroller is shown in figures 3, 4 and table Data Transfer. All requested data have to be transferred via 16-bit or 24-bit commands. Due to the 8-bit structure, the serial output interface of a microcontroller can be used for the data transfer. The PLL functions can be controlled by 24-bit commands, while the alignment functions are controlled by 16-bit commands. The alignment function control normally is set once by switching on the tuner. Then the tuner automatically will be aligned. The data for alignment are stored in a separate EPROM. Via integrated capacitors it is possible to tune the reference oscillator (this function is controlled via the 3-wire bus).

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15)

Parameters		Symbol	Value	Unit
Analog supply voltage	Pin 6	V_S	8 to 15	V
Input voltage	Pins 16, 17 and 18	V_I	–0.3 to +12	V
Output current	Pins 7, 8, 9 and 10	I_O	–1 to +5	mA
Output drain voltage	Pins 7, 8, 9 and 10	V_{OD}	15	V
Ambient temperature range		T_{amb}	–40 to +85	°C
Storage temperature range		T_{stg}	–40 to +125	°C
Junction temperature		T_j	125	°C
Electrostatic handling		V_{ESD}	t.b.d.	V

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	when soldered to PCB	R_{thJA}	140	K/W

Operating Range

All voltages are referred to GND (Pin 15)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 6	V_S	8	8.5	14	V
Ambient temperature		T_{amb}	–40		+85	°C
Input frequency	Pin 19	RFi	70		160	MHz
Programmable divider		SF	2		65535	
Crystal oscillator	Pins 12 and 13	fXTAL	0.1		15	MHz

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = +8.5 V, T_{amb} = +25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**Pin 6**					
Analog supply voltage		V_A	8	8.5	12	V
Supply current	**Pin 20**					
Analog supply current		I_A	4.5	10	20	mA
OSCIN	**Pin 13**					
Input voltage	f = 0.1 to 15 MHz	V_{OSC}	100			mV_{rms}
FMOSCIN	**Pin 19**					
Input voltage	f = 70 to 120 MHz f = 120 to 160 MHz	V_{FMOSC} V_{FMOSC}	40 150			mV_{rms} mV_{rms}
PD	**Pin 2**					
Output current 1	PD = 2.5 V		20	25	30	µA
Output current 2	PD = 2.5 V		80	100	120	µA
Output current 3	PD = 2.5 V	± IPD	400	500	600	µA
Output current 4	PD = 2.5 V		1600	2000	2400	µA
Leakage current	PD = 2.5 V	± IPDL			20	nA

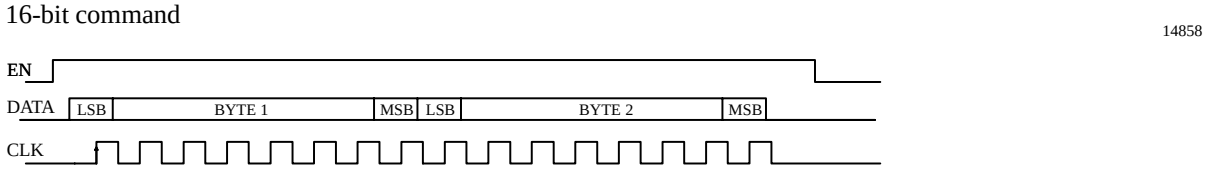
Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = +8.5 V, T_{amb} = +25°C

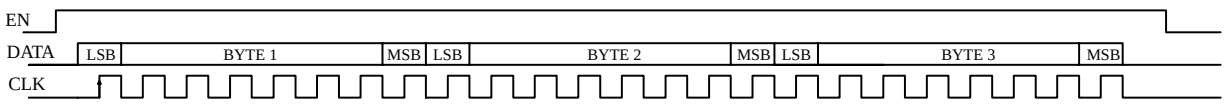
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
PDO	**Pin 1**					
Saturation voltage HIGH LOW	$V_{SATH} - (V_A - V_{PDOFM})$, I = 15 mA	V_{SATH} V_{SATL}	 100	 200	500 400	mV mV
SWO1, SWO2, SWO3, SWO4 (open drain)	**Pins 7, 8, 9 and 10**					
Output leakage current HIGH	I = 1 mA, V7,8,9,10 = 8.5 V	I_{OHL}			100	nA
Output voltage LOW		V_{SWOL}		100	400	mV
DAC1, DAC2	**Pins 3 and 4**					
Output current		$I_{DAC1, 2}$			1	mA
Output voltage		$V_{DAC1, 2}$	0.3		$V_S - 0.5$	V
Gain range (resolution 256 steps)			0.6		2.3	
Offset range (resolution 24 steps)			–0.6		0.7	V
DAC 3	**Pin 5**					
Output current		I_{DAC3}			1	mA
Output voltage (resolution 16 steps)		V_{DAC3}	0.25		6	V
MX2LO						
Output AC voltage	At Pin15: 47 pF and 1 kΩ	V_{MX2LO}	80	120	200	mV_{pp}
Output DC voltage		V_{DC}	1.6	1.9	2.1	V

3-Wire Bus Description

16-bit command



24-bit command



e.g., Divider

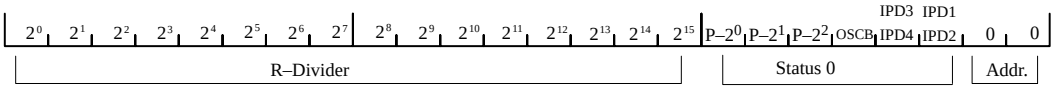


Figure 3. Pulse diagram

Data Transfer

A

MSB		BYTE 2					LSB	MSB	BYTE 1						LSB
ADDR.		Oscillator tuning function													
1	0	8pF	32pF	16pF	8pF	4pF	2pF	1pF	0.5pF						
		B85	B84	B83	B82	B81	B80	B79	B78	B77	B76	B75	B74	B73	B72

B

MSB		Byte 3					LSB	MSB	BYTE 2							LSB	MSB	BYTE 1							LSB
ADDR.		STATUS 0						R – DIVIDER																	
0	0	IPD 1,2	IPD 3,4	OSCB 0 = on, 1 = off	$P–2^2$	$P–2^1$	$P–2^0$	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
		B71	B70	B69	B68	B67	B66	B65	B64	B63	B62	B61	B60	B59	B58	B57	B56	B55	B54	B53	B52	B51	B50

C

MSB		BYTE 2					LSB	MSB	BYTE 1						LSB
ADDR.		DAC1 – GAIN & OFFSET													
0	0	$O–2^5$	$O–2^4$	$O–2^3$	$O–2^2$	$O–2^1$	$O–2^0$	$G–2^7$	$G–2^6$	$G–2^5$	$G–2^4$	$G–2^3$	$G–2^2$	$G–2^1$	$G–2^0$
		B49	B48	B47	B46	B45	B44	B43	B42	B41	B40	B39	B38	B37	B36

D

MSB		Byte 3					LSB	MSB	BYTE 2							LSB	MSB	BYTE 1							LSB
ADDR.		STATUS 1						N – DIVIDER																	
0	1	0	AM = 1 FM = 0	SWO4 1=off, 0=on	SWO3 1=off, 0=on	SWO2 1=off, 0=on	SWO1 1=off, 0=on	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
		B35	B34	B33	B32	B31	B30	B29	B28	B27	B25	B24	B23	B22	B22	B21	B20	B19	B18	B17	B16	B15	B14

E

MSB		BYTE 2					LSB	MSB	BYTE 1						LSB
ADDR.		DAC2 – GAIN & OFFSET													
0	1	$O–2^5$	$O–2^4$	$O–2^3$	$O–2^2$	$O–2^1$	$O–2^0$	$G–2^7$	$G–2^6$	$G–2^5$	$G–2^4$	$G–2^3$	$G–2^2$	$G–2^1$	$G–2^0$
		B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Timing Information

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
3-wire bus, ENABLE, DATA, CLOCK **Pins 16, 17, 18**						
Input voltage HIGH LOW		V_{BUS} V_{BUS}	2.0		 1.0	V V
Clock frequency					1.0	MHz
Period of CLK HIGH LOW		t_H t_L	250 250			ns ns
Rise time EN, DA, CLK		t_r			400	ns
Fall time EN, DA, CLK		t_f			100	ns
Set-up time		t_s	100			ns
Hold time EN		t_{HEN}	250			ns
Hold time DA		t_{HDA}	0			ns

Bus Timing

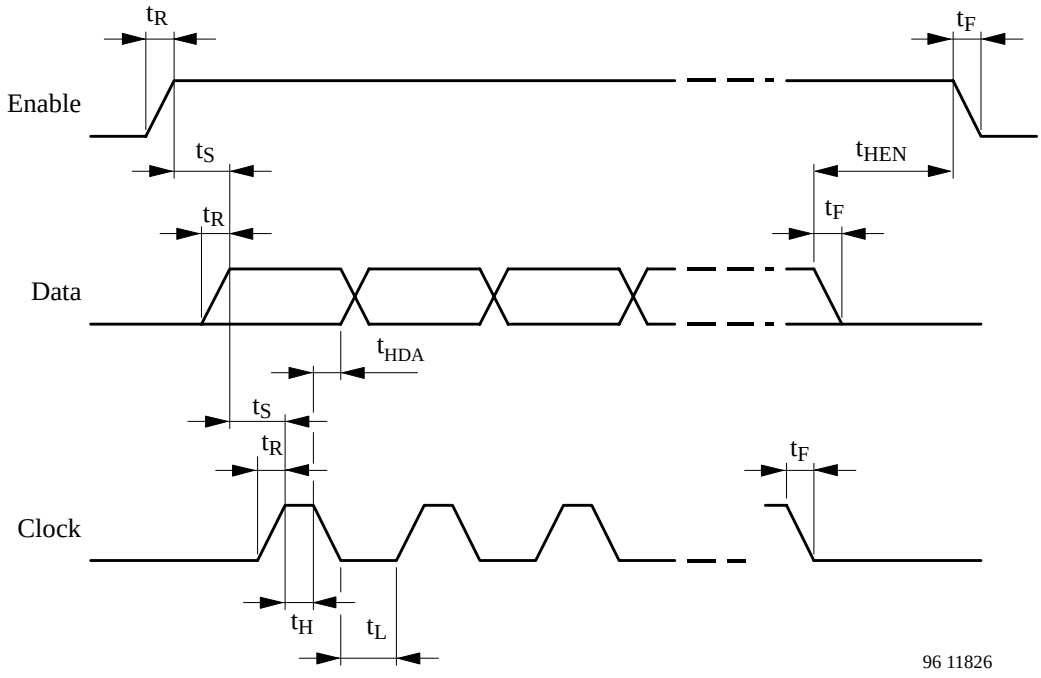


Figure 4. Bus timing

Bus Control

The charge pump current can be choosen by setting the Bits IPD1, 2 (Bit 71) and IPD3, 4 (Bit 70) as following:

IPD (µA)	IPD1, 2	IPD3, 4
25	0	0
100	0	1
500	1	0
2000	1	1

The oscillator buffer output can be switched by the OSCB Bit as following (Bit 69):

MX2LO AC Voltage	OSCB
ON	0
OFF	1

The DAC3 output voltage can be controlled by the Bits P-2^0 to P-2^2 (Bits 66 to 68) as following:

DAC3 Offset Approx.	Bit68	Bit67	Bit66
0.5 V	0	0	0
1.1 V	0	0	1
1.8 V	0	1	0
2.4 V	0	1	1
3.1 V	1	0	0
3.7 V	1	0	1
4.4 V	1	1	0
5.0 V	1	1	1

The FM/AM function can be controlled by setting the FM/AM Bit 34 as following:

FM/AM	Bit 34
FM	0
AM	1

The switching output SWO1 to SWO4 can be controlled as following (Bits 30 to 33):

Switch Output	Bit
SWOx = ON	0
SWOx = OFF	1

The gain of DAC1 has a range of 0.7 x V(PDO) to 2.15 x V(PDO). V(PDO) is the PLL tuning voltage output. This range is divided into 256 steps. So one step is approximately (2.15–0.7)/256 = 5.664 m. The gain can be controlled by the Bits 36 to 43 (G–2^0 to G–2^7) as following:

Gain DAC1 Approx.	B43	B42	B41	B40	B39	B38	B37	B36
0.7	0	0	0	0	0	0	0	0
0.70566	0	0	0	0	0	0	0	1
0.71133	0	0	0	0	0	0	1	0
0.71699	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...
1.00019	0	0	1	1	0	1	0	1
...	...	...	...	...	...	...	...	...
2.1386	1	1	1	1	1	1	0	1
2.14434	1	1	1	1	1	1	1	0
2.15 m	1	1	1	1	1	1	1	1

The offset of DAC1 has a range of 0.5 to –0.6. This range is divided into 64 steps. So one step is approximately 1.1V/63 = 17.2 m. The offset can be controlled by the Bits 44 to 49 (O–2^0 to O–2^5) as following:

Offset DAC1 Approx.	B49	B48	B47	B46	B45	B44
0.5	0	0	0	0	0	0
0.4828	0	0	0	0	0	1
0.4656	0	0	0	0	1	0
0.4484	0	0	0	0	1	1
...	...	...	...	...	...	...
–0.0156	0	1	1	1	1	0
...	...	...	...	...	...	...
0.5656	1	1	1	1	0	1
–0.5828	1	1	1	1	1	0
–0.6	1	1	1	1	1	1

The tuning capacity for the crystal oscillator has a range of 0.5 pF to 71.5 pF. The values are coded binary. The tuning can be controlled by the Bits 78 to 85 as following:

C (pF)	B85	B84	B83	B82	B81	B80	B79	B78
0	1	1	1	1	1	1	1	1
0.5	1	1	1	1	1	1	1	0
1.0	1	1	1	1	1	1	0	1
1.5	1	1	1	1	1	1	0	0
...	...	...	...	...	...	...	...	...
63.5	1	0	0	0	0	0	0	0
71.5	0	0	0	0	0	0	0	0

The gain of DAC2 has a range of 0.7 x V(PDO) to 2.15 x V(PDO). V(PDO) is the PLL tuning voltage output. This range is divided into 256 steps. So one step is approximately (2.15–0.7)/256 = 5.664 m. The gain can be controlled by the bits 0 to 7 ($G–2^0$ to $G–2^7$) as following:

Gain DAC2 Approx.	B7	B6	B5	B4	B3	B2	B1	B0
0.7	0	0	0	0	0	0	0	0
0.70566	0	0	0	0	0	0	0	1
0.71133	0	0	0	0	0	0	1	0
0.71699	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...
1.00019	0	0	1	1	0	1	0	1
...	...	...	...	...	...	...	...	...
2.1386	1	1	1	1	1	1	0	1
2.14434	1	1	1	1	1	1	1	0
2.15 m	1	1	1	1	1	1	1	1

The offset of DAC2 has a range of 0.5 to –0.6. This range is divided into 64 steps. So one step is approximately 1.1V/63 = 17.2 m. The offset can be controlled by the Bits 8 to 13 ($O–2^0$ to $O–2^5$) as following:

Offset DAC2 Approx.	B13	B12	B11	B10	B9	B8
0.5	0	0	0	0	0	0
0.4828	0	0	0	0	0	1
0.4656	0	0	0	0	1	0
0.4484	0	0	0	0	1	1
...	...	...	...	...	...	...
–0.0156	0	1	1	1	1	0
...	...	...	...	...	...	...
0.5656	1	1	1	1	0	1
–0.5828	1	1	1	1	1	0
–0.6	1	1	1	1	1	1

Input / Output Interface Circuits

PDO

PDO is the loop amplifier output of the PLL. The bipolar output stage is a rail-to-rail amplifier.

PD

PD is the current charge pump output of the PLL. The current can be controlled by setting the Bits IDP1, 2 and IDP3, 4. The loop filter has to be designed corresponding to the choosen pump current and the internal reference frequency. A recommendation can be found in the application circuit.

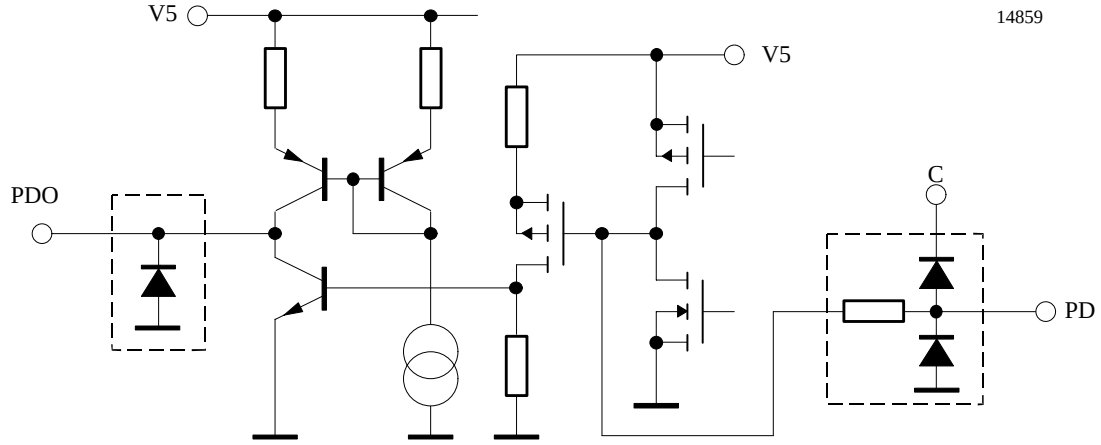


Figure 5.

FMOSCIN

FMOSCIN is the preamplifier input for the FM/AM oscillator signal.

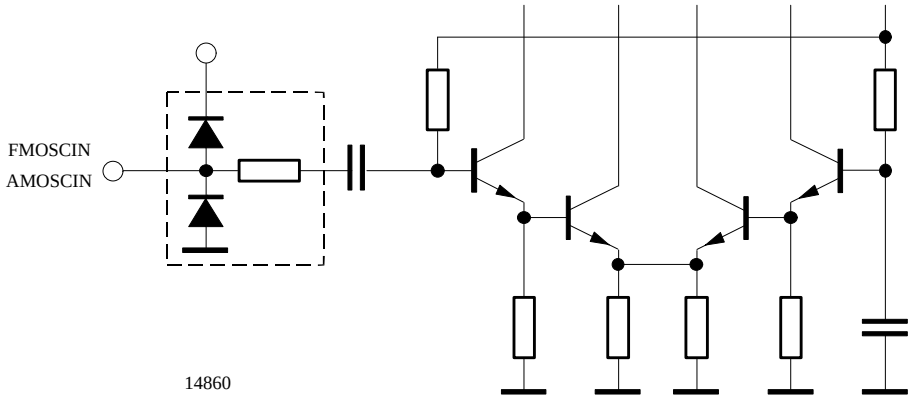


Figure 6.

MX2LO

MX2LO is the buffered output of the crystal oscillator.

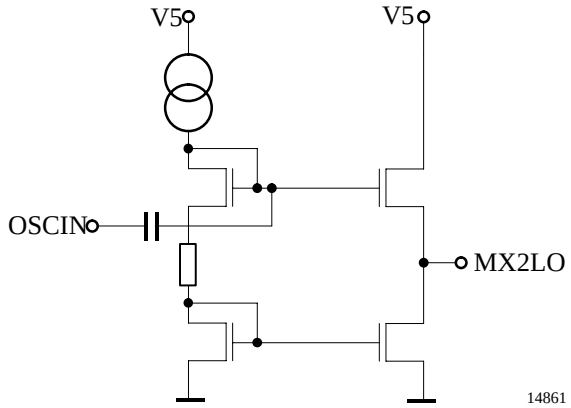


Figure 7.

DAC 1, 2 and 3

DAC 1 to 3 are the outputs for automatic tuner alignment.

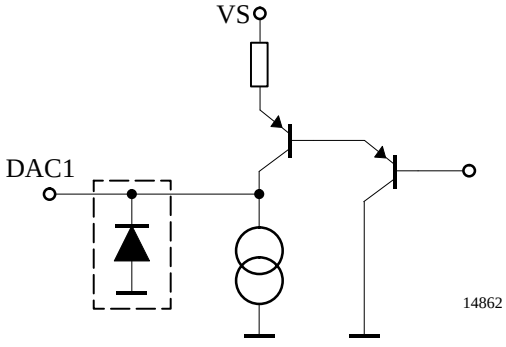


Figure 8.

EN, DATA, CLK

All functions can be controlled via a 3-wire bus consisting of ENABLE, DATA and CLOCK. The bus is designed for microcontrollers which operate with 3 V supply voltage. Details of the data transfer protocol are shown in the table ‘Data Transfer’.

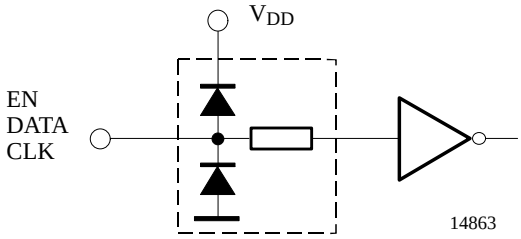


Figure 9.

SWO1, 2, 3 and 4

All switching outputs are ‘open drain’ and can be set and reset by software control. Details are described in the data transfer protocol.

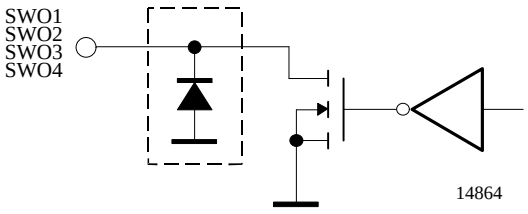


Figure 10.

OSCIN, OSCOUT

A crystal resonator (up to 16 Mhz) is connected between OSCIN and OSCOUT in order to generate the reference frequency. The complete application circuit is shown in figure 15. If a reference is available, it can be applied at OSCIN. The minimum voltage should be 100mVrms. In this case, pin OSCOUT has to be open.

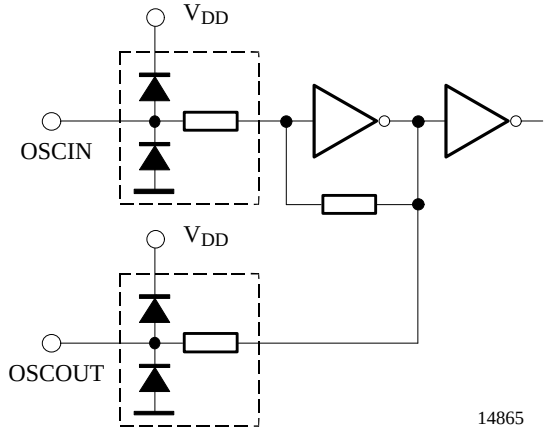


Figure 11.

Application Information

Function of DAC1, 2 in the FM Mode

For automatic tuner alignment, the DAC1 and 2 of the U4256BM can be controlled by setting gain and offset values. The following figure shows the principle of the operation in FM mode. The gain is in the range of 0.7 to 2.15. The offset range is +0.5 V to –0.6 V. For alignment, DAC1 and 2 are connected to the varicaps of the preselection filter and the IF filter. For alignment, offset and gain is set for having the best tuner tracking

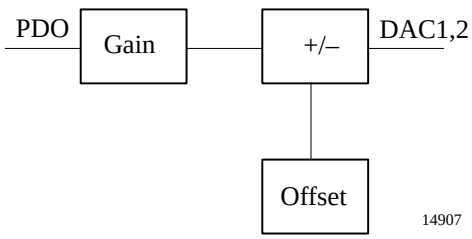


Figure 12.

Function of DAC1, 2 in the AM Mode

In AM mode, DAC1, 2 can be used as standard DAC converters. The resolution of 8 bit is controlled via the gain bits in a range of approximately 0.5 V to 7 V, depending on the offset value.

FMOSCIN Sensitivity

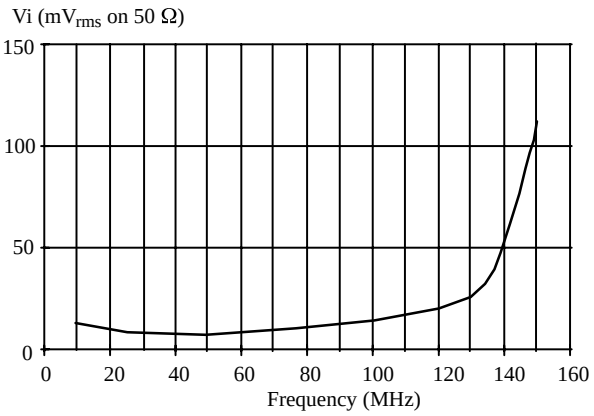


Figure 13.

Oscillator Tuning Function Schematic

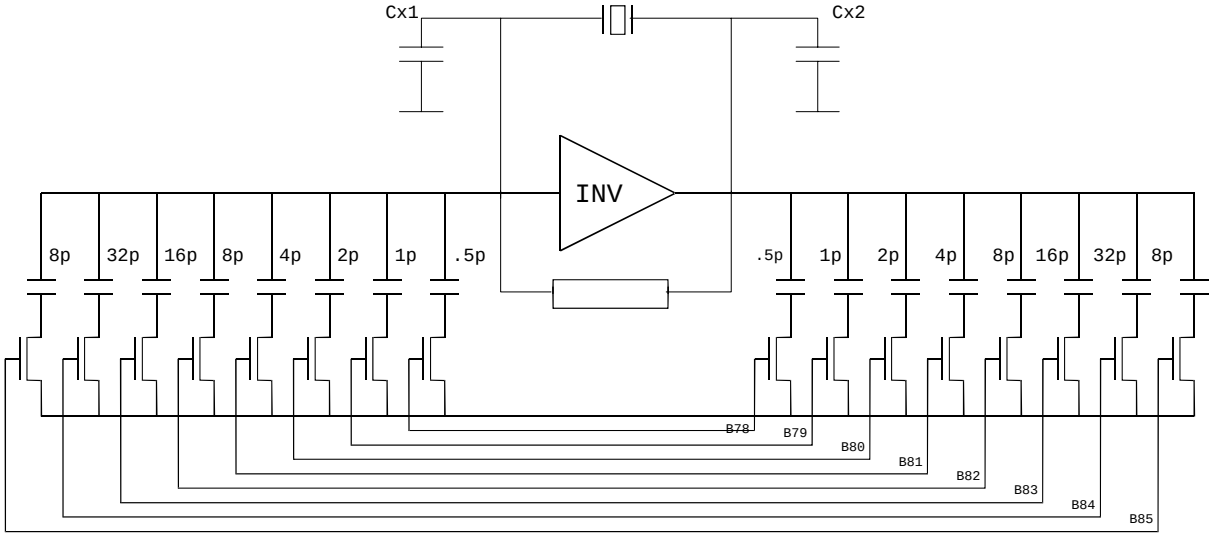


Figure 14.

Application Circuit

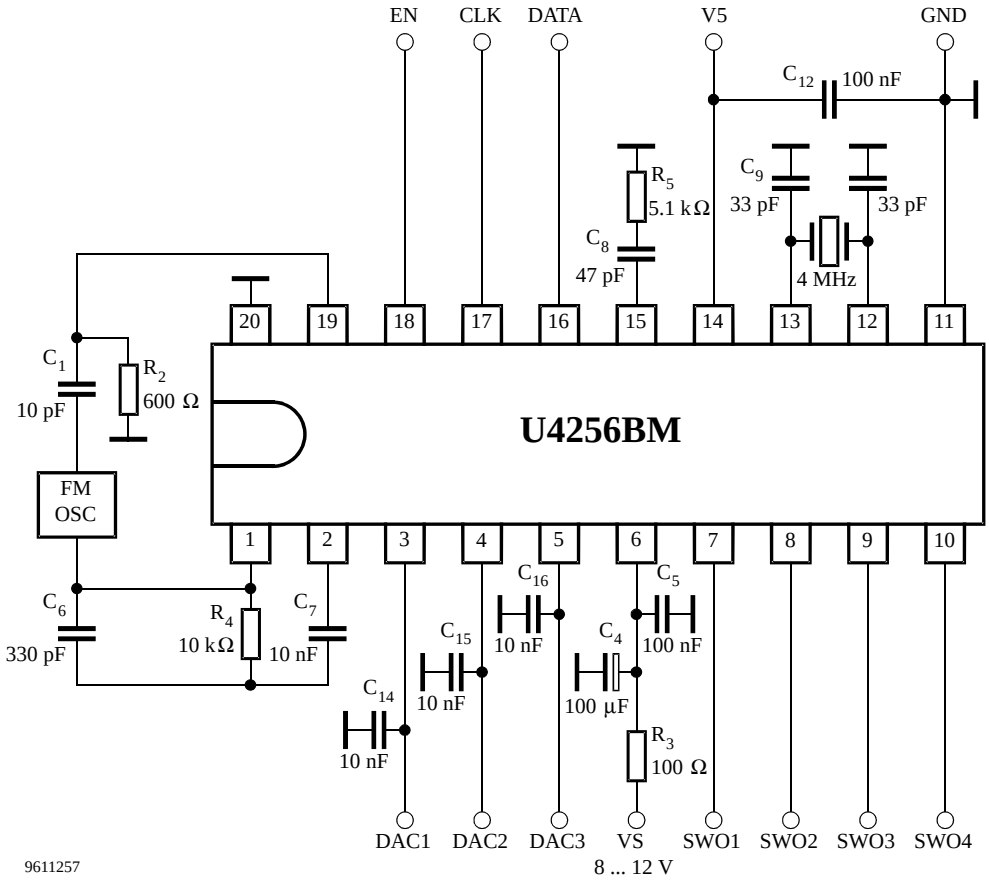


Figure 15. Application circuit

Application Board Schematic

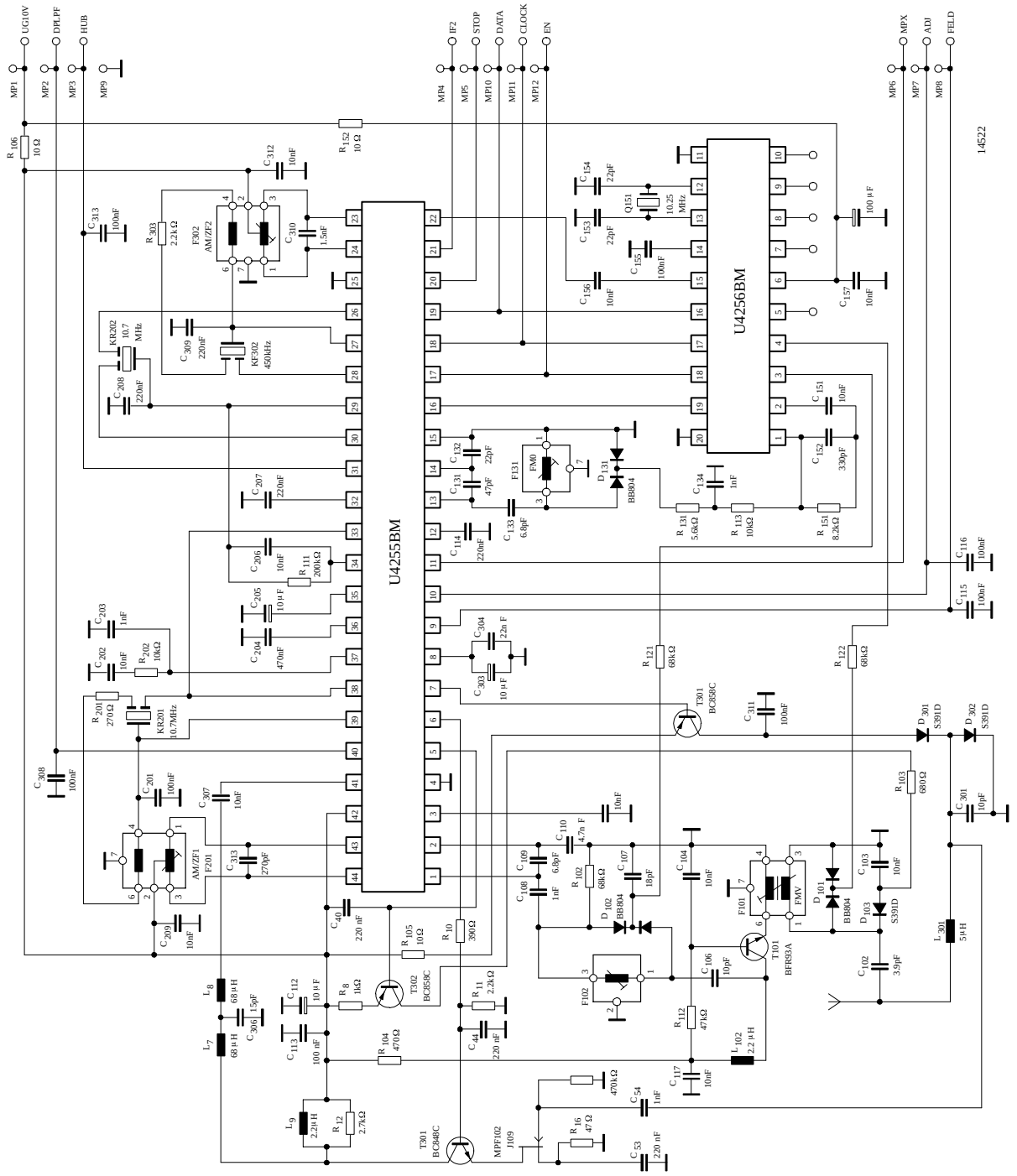
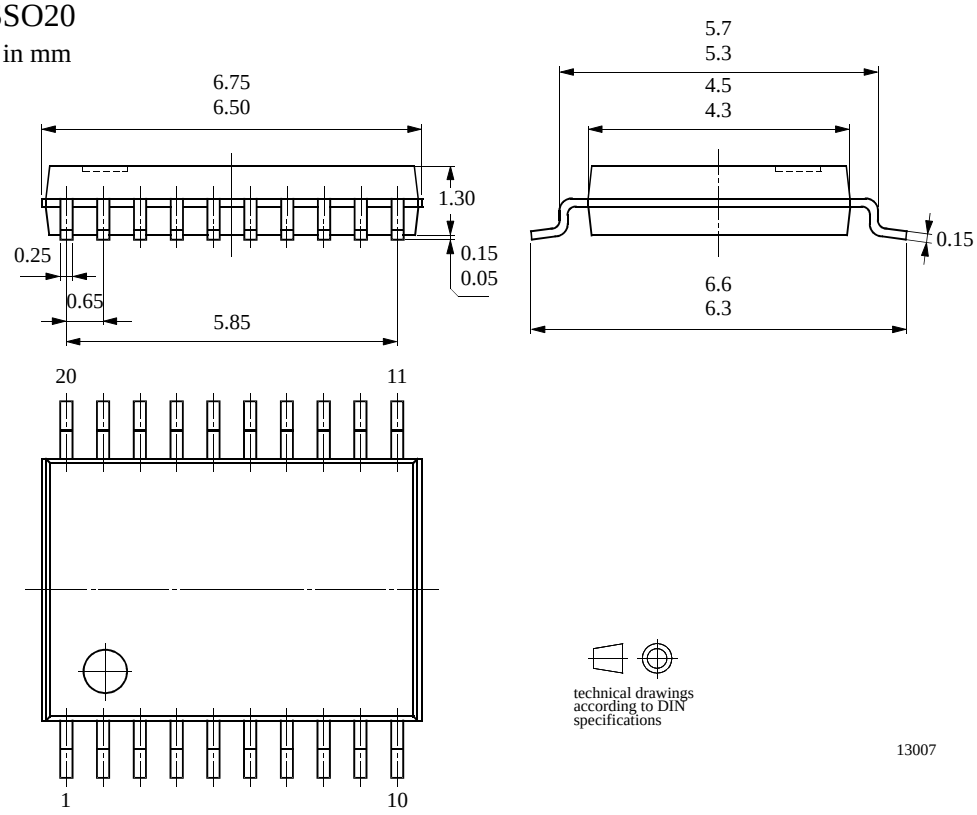


Figure 16. Application borad schematic

Package Information

Package SSO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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