



**FLASH-ROM MODULE 8MByte (8M x 8-Bit) – SMM Packages**  
**Part No. HMF8M8F4V,HMF8M8F4VT**

## GENERAL DESCRIPTION

The HMF8M8F4V is a high-speed flash read only memory (FROM) module containing 8,388,608 words organized in a x8bit configuration. The module consists of four 2M x 8 FROM mounted on a 100-pin, MMC connector FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Four chips enable inputs, /CS(/CS0, /CS1, /CS2, /CS3) are used to enable the module's 4 chips independently. Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3V DC power supply and all inputs and outputs are LVTTTL-compatible.

## PIN ASSIGNMENT

### FEATURES

- w Part identification
  - HMF8M8F4V  
(Bottom boot block configuration)
  - HMF8M8F4VT  
(Top boot block configuration)
- w Access time: 80, 90, 120ns
- w High-density 8MByte design
- w High-reliability, low-power design
- w Single + 3V to 3.6V power supply
- w 100-Pin Designed
  - 50-Pin Fine Pitch MMC Connector P1,P2
- w Minimum 1,000,000 write/erase cycle
- w 20-year data retention at 125 °C
- w Flexible sector architecture
- w Embedded algorithms
- w Erase suspend / Erase resume
- w The used device is Am29LV116B

### OPTIONS

w Timing

80ns access	- 80
90ns access	- 90
120ns access	-120

w Packages

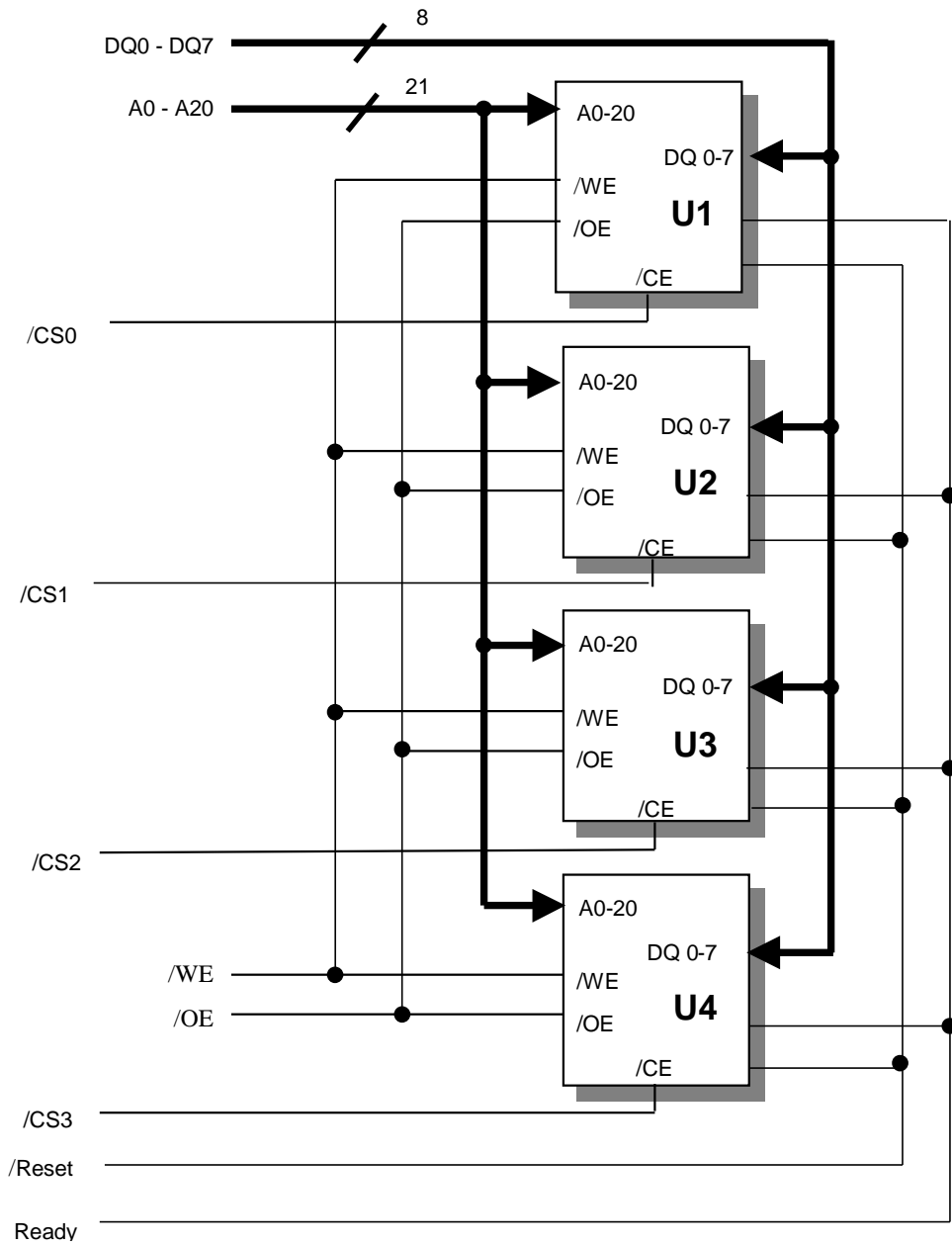
100-pin MMC	F
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### MARKING

50-PIN P1 Connector				50-PIN P2 Connector			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	VCC	26	VCC	1	VCC	26	VCC
2	NC	27	NC	2	NC	27	NC
3	NC	28	A19	3	/WE	28	NC
4	A20	29	A18	4	NC	29	NC
5	NC	30	A17	5	Ready	30	NC
6	NC	31	A16	6	NC	31	NC
7	NC	32	A15	7	NC	32	NC
8	VSS	33	VSS	8	VSS	33	VSS
9	NC	34	A14	9	/OE	34	NC
10	NC	35	A13	10	/CS0	35	/CS2
11	NC	36	NC	11	/CS1	36	/CS3
12	NC	37	DQ7	12	NC	37	NC
13	VSS	38	VSS	13	VSS	38	VSS
14	DQ6	39	DQ5	14	NC	39	NC
15	DQ4	40	A12	15	NC	40	NC
16	DQ3	41	A11	16	NC	41	NC
17	DQ2	42	A10	17	/Reset	42	NC
18	VSS	43	VSS	18	VSS	43	VSS
19	DQ1	44	A9	19	NC	44	NC
20	DQ0	45	A8	20	NC	45	NC
21	A0	46	A7	21	NC	46	NC
22	A1	47	A6	22	NC	47	NC
23	A2	48	A5	23	VSS	48	VSS
24	A3	49	A4	24	NC	49	NC
25	VCC	50	VCC	25	VCC	50	VCC

Note: P1-A23(27Pin) must be Grounded

FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

MODE	/CS	/OE	/WE	RESET	DQ
STANDBY	$V_{CC} \pm 0.3V$	X	X	$V_{CC} \pm 0.3V$	HIGH-Z
RESET	X	X	X	L	HIGH-Z
SECTOR PROTECT	L	H	L	$V_{ID}$	$D_{IN}, D_{OUT}$
SECTOR UNPROTECT	L	H	L	$V_{ID}$	$D_{IN}, D_{OUT}$
READ	L	L	H	H	$D_{OUT}$
WRITE	L	H	L	H	$D_{OUT}$

**Note** : X means don't care

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Voltage on Any Pin Relative to $V_{SS}$	-0.5V to $V_{CC} + 0.5V$
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	-0.5V to +4.0V
Output Short Circuit Current	200mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C

Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	RANGE
$V_{CC}$ for regulated Supply Voltage	+3.0V to 3.6V
$V_{CC}$ for full voltage	+2.7V to 3.6V

## DC AND OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Load Current	$V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC} \text{ max}$	$I_{L1}$		$\pm 1.0$	$\mu A$
Output Leakage Current	$V_{OUT} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC} \text{ max}$	$I_{L0}$		$\pm 1.0$	$\mu A$
Output High Voltage	$I_{OH} = -2.0mA$ , $V_{CC} = V_{CC} \text{ min}$	$V_{OH}$	0.85 $V_{CC}$		V
Output Low Voltage	$I_{OL} = 4.0mA$ , $V_{CC} = V_{CC} \text{ min}$	$V_{OL}$		0.45	V
$V_{CC}$ Active Read Current	$/CE = V_{IL}$ , $/OE = V_{IH}$ , $f = 5MHz$	$I_{CC1}$		16	mA

Vcc Active Write Current	/CE = V <sub>IL</sub> , /OE=V <sub>IH</sub>	I <sub>CC2</sub>		30	mA
Vcc Standby Current	/CE, RESET=V <sub>CC</sub> ±0.3V	I <sub>CC3</sub>		5	mA
Vcc Reset Current	RESET=V <sub>SS</sub> ±0.3V,	I <sub>CC4</sub>		5	mA
Low Vcc Lock-Out Voltage		V <sub>LKO</sub>	2.3	2.5	V

## ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	Sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	9	300	μS	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	Excludes system-level overhead

## TSOP PIN CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	6	7.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8.5	12	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	7.5	9	pF

Notes: Test conditions T<sub>A</sub> = 25° C, f=1.0 MHz.

## AC CHARACTERISTICS

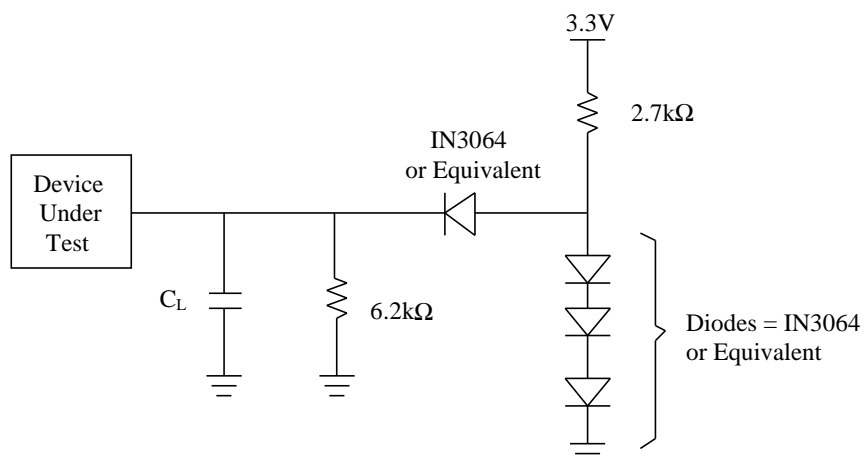
### ⌋ Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		-80	-90	UNIT
JEDEC	STANDARD				(NOTE1)	(NOTE1)	
t <sub>AVAV</sub>	t <sub>RC</sub>	Read Cycle Time		Min	80	90	ns
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	/CE = V <sub>IL</sub> /OE = V <sub>IL</sub>	Max	80	90	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	/OE = V <sub>IL</sub>	Max	80	90	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Chip Enable to Output Delay		Max	80	90	ns

$t_{EHQZ}$	$t_{DF}$	Chip Enable to Output High-Z		Max	25	30	ns
$t_{GHQZ}$	$t_{DF}$	Output Enable to Output High-Z		Max	25	30	ns
$t_{AXQX}$	$t_{QH}$	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	ns

**TEST CONDITIONS**

**Notes :** Test Conditions : Output Load : 1TTL gate and 100 pF  
 Input rise and fall times : 5 ns  
 Input pulse levels: 0V to 3.0V  
 Timing measurement reference level  
 Input : 1.5 V  
 Output : 1.5V



**Note :**  $C_L = 100\text{pF}$  including jig capacitance

**u Erase/Program Operations**

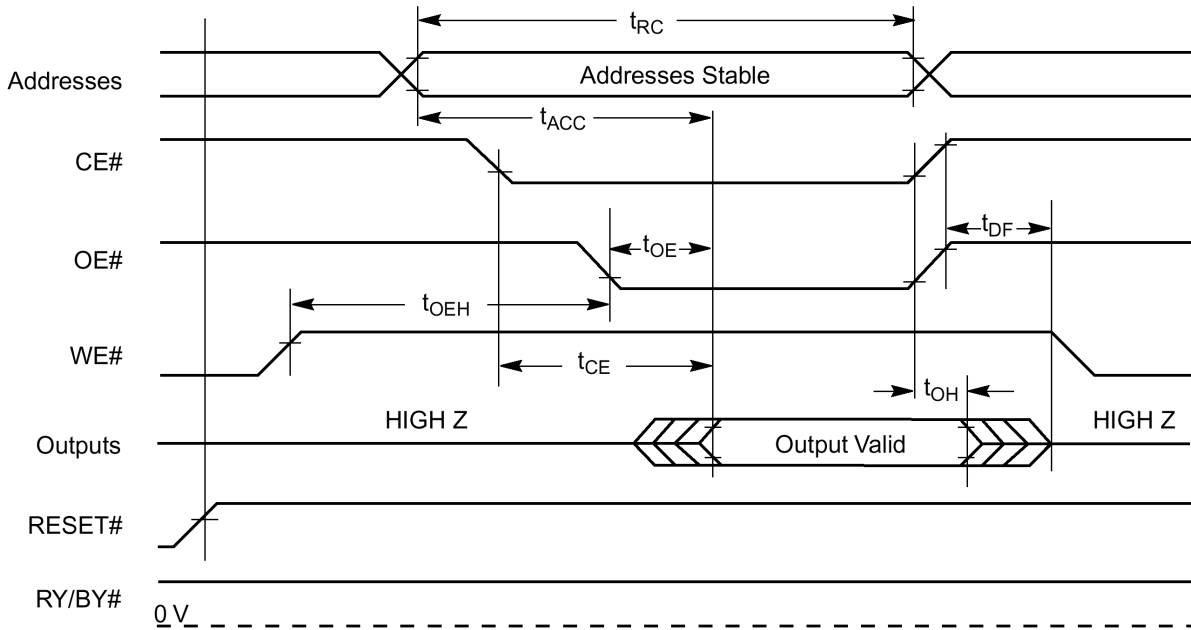
PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	STANDARD					
$t_{AVAV}$	$t_{WC}$	Write Cycle Time	Min	80	90	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	Min	0	0	ns
$t_{WLAX}$	$t_{AH}$	Address Hold Time	Min	45	45	ns
$t_{DVWH}$	$t_{DS}$	Data Setup Time	Min	35	45	ns
$t_{WHDX}$	$t_{DH}$	Data Hold Time	Min	0	0	ns

	t <sub>OES</sub>	Output Enable Setup Time	Min	0	0	ns
t <sub>GHWL</sub>	t <sub>GHWL</sub>	Read Recover Time Before Write	Min	0	0	ns
t <sub>ELWL</sub>	t <sub>CS</sub>	/CE Setup Time	Min	0	0	ns
t <sub>WHEH</sub>	t <sub>CH</sub>	/CE Hold Time	Min	0	0	ns
t <sub>WLWH</sub>	t <sub>WP</sub>	Write Pulse Width	Min	35	35	ns
t <sub>WHWL</sub>	t <sub>WPH</sub>	Write Pulse Width High	Min	30	30	ns
t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	Byte Programming Operation	Typ	9	9	μs
t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	Sector Erase Operation (Note1)	Typ	0.7	0.7	sec
			Max	50	50	sec
	t <sub>VCS</sub>	Vcc Setup Time	Min	50	50	μs
	t <sub>RB</sub>	Recovery time from RY/BY	Min	0	0	μs
	t <sub>BUSY</sub>	Program/Erase Valid to RY/BY Delay	Min	90	90	μs

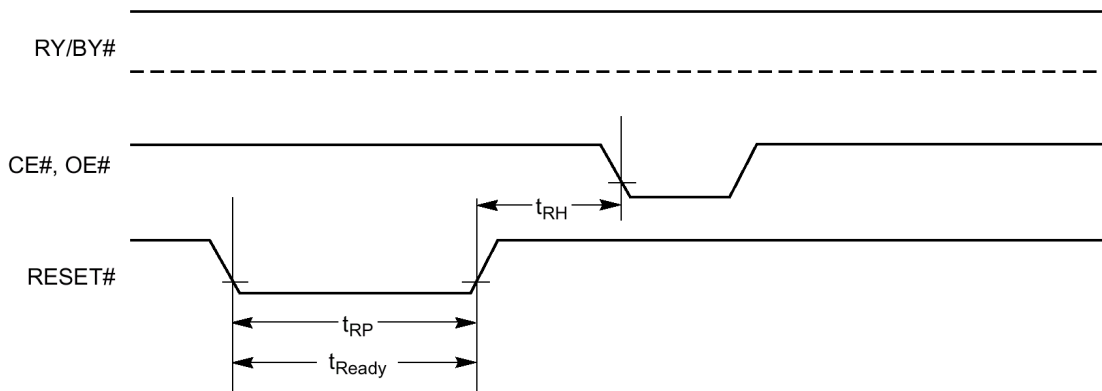
U Alternate /CE Controlled Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	STANDARD					
t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time	Min	80	90	ns
t <sub>AVEL</sub>	t <sub>AS</sub>	Address Setup Time	Min	0	0	ns
t <sub>ELAX</sub>	t <sub>AH</sub>	Address Hold Time	Min	45	45	ns
t <sub>DVEH</sub>	t <sub>DS</sub>	Data Setup Time	Min	35	45	ns
t <sub>EHDx</sub>	t <sub>DH</sub>	Data Hold Time	Min	0	0	ns
	t <sub>OES</sub>	Output Enable Setup Time	Min	0	0	ns
t <sub>GHEL</sub>	t <sub>GHEL</sub>	Read Recover Time Before Write /OE High to /WE Low	Min	0	0	ns
t <sub>WLEL</sub>	t <sub>WS</sub>	/WE Setup Time	Min	0	0	ns
t <sub>EHWH</sub>	t <sub>WH</sub>	/WE Hold Time	Min	0	0	ns
t <sub>ELEH</sub>	t <sub>CP</sub>	/CE Pulse Width	Min	35	35	ns
t <sub>EHEL</sub>	t <sub>CPH</sub>	/CE Pulse Width High	Min	30	30	ns
t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	Byte Programming Operation	Typ	9	9	μs
t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	Sector Erase Operation (Note)	Typ	0.7	0.7	sec

**u READ OPERATIONS TIMING**

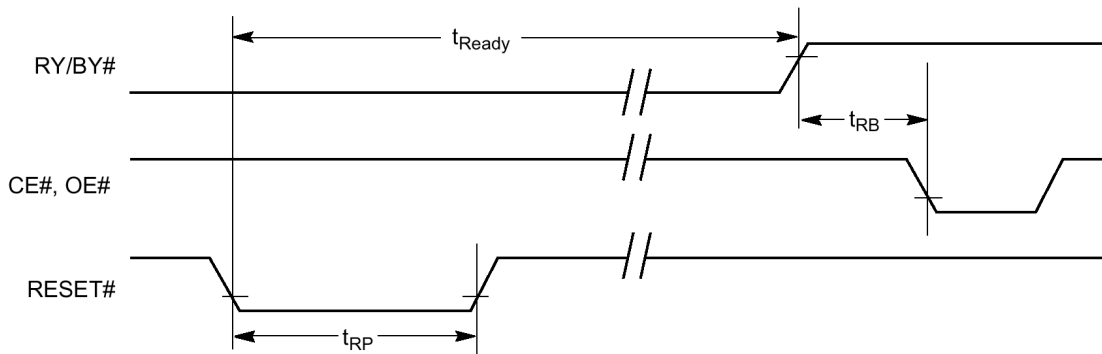


**u RESET TIMING**

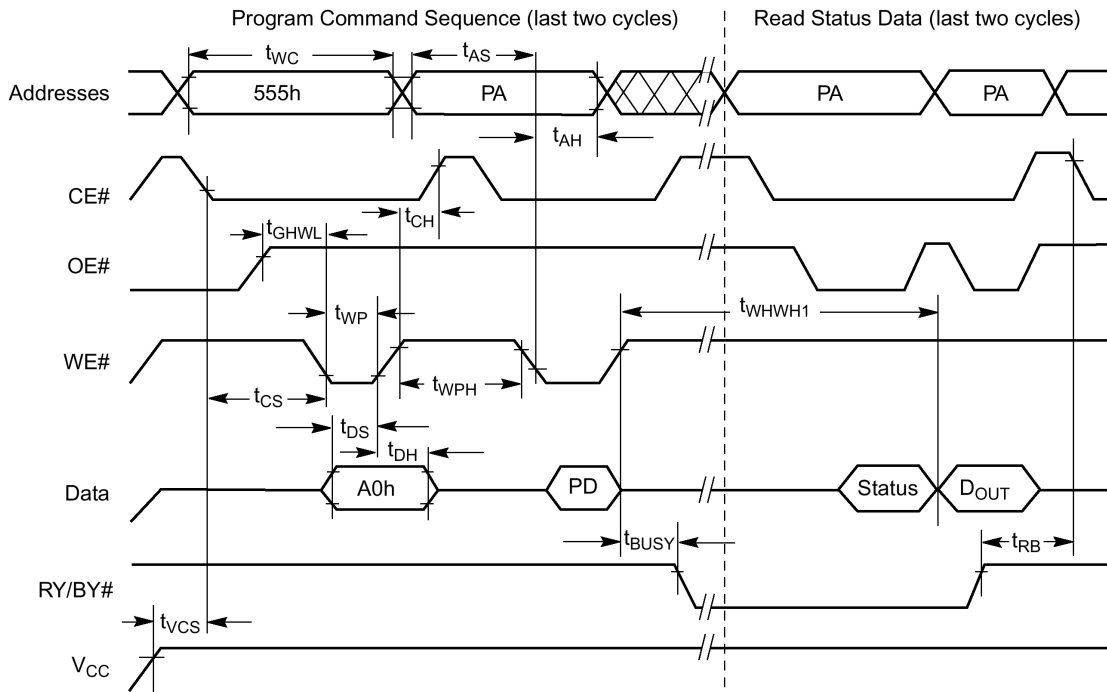


Reset Timings NOT during Embedded Algorithms

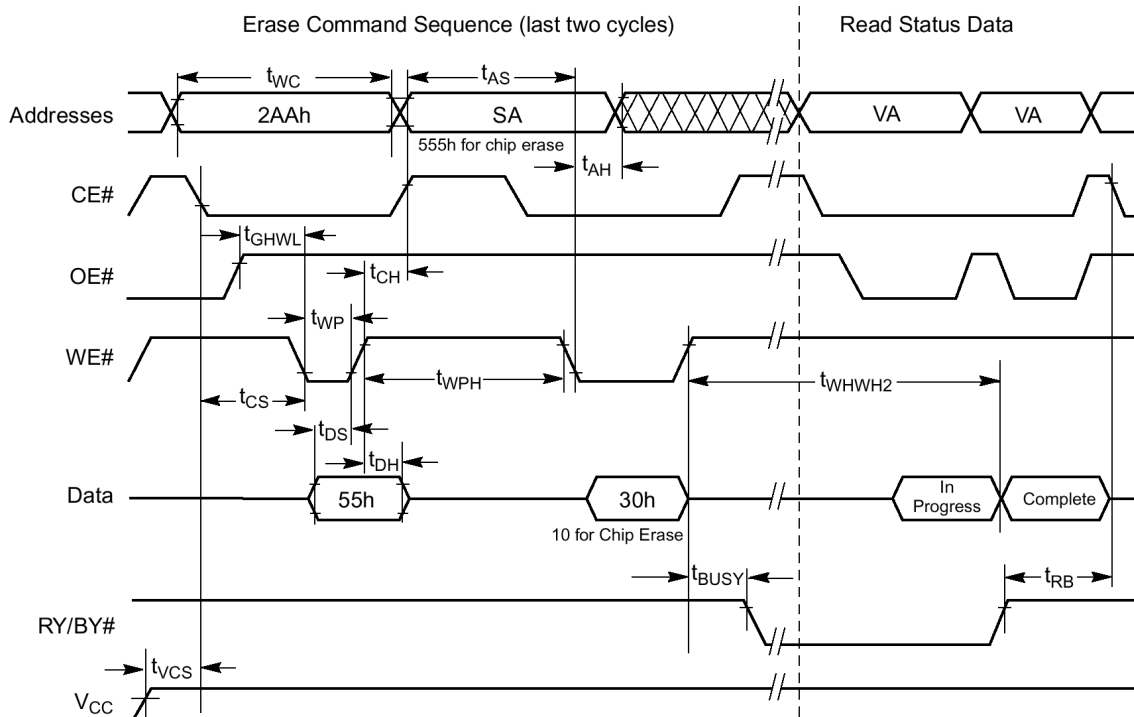
Reset Timings during Embedded Algorithms



U PROGRAM OPERATIONS TIMING

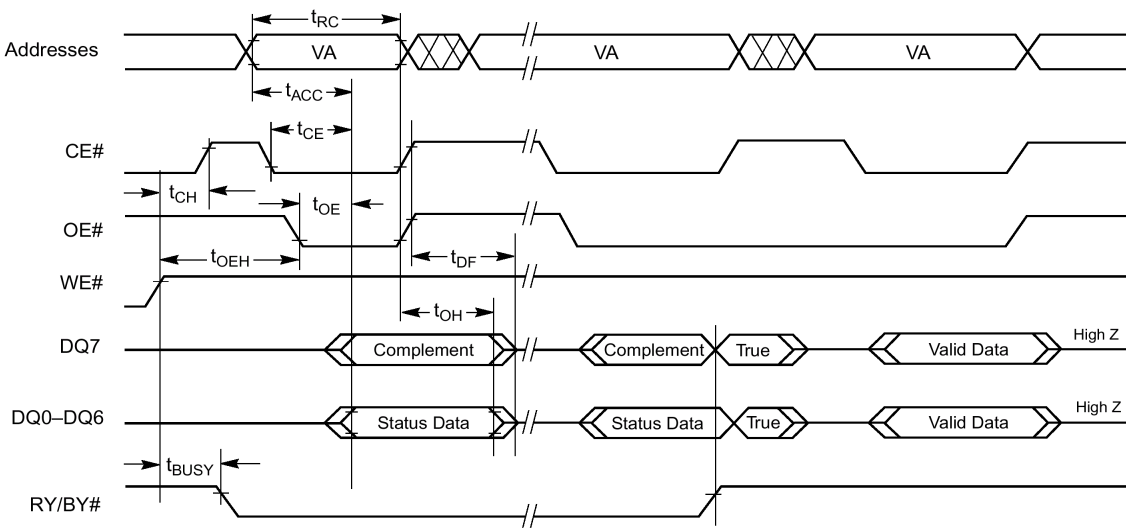


U CHIP/SECTOR ERASE OPERATION TIMINGS

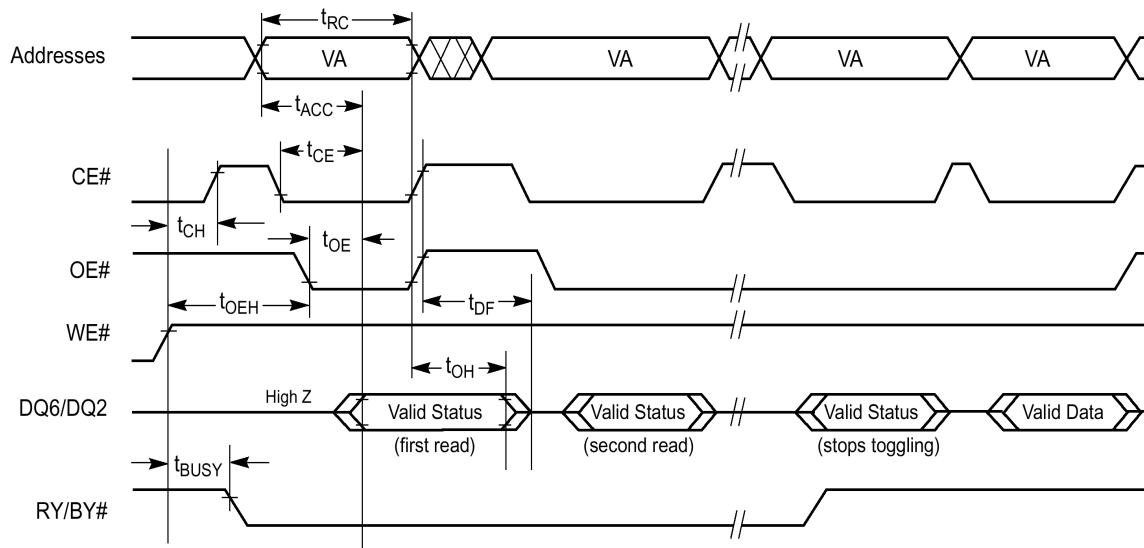




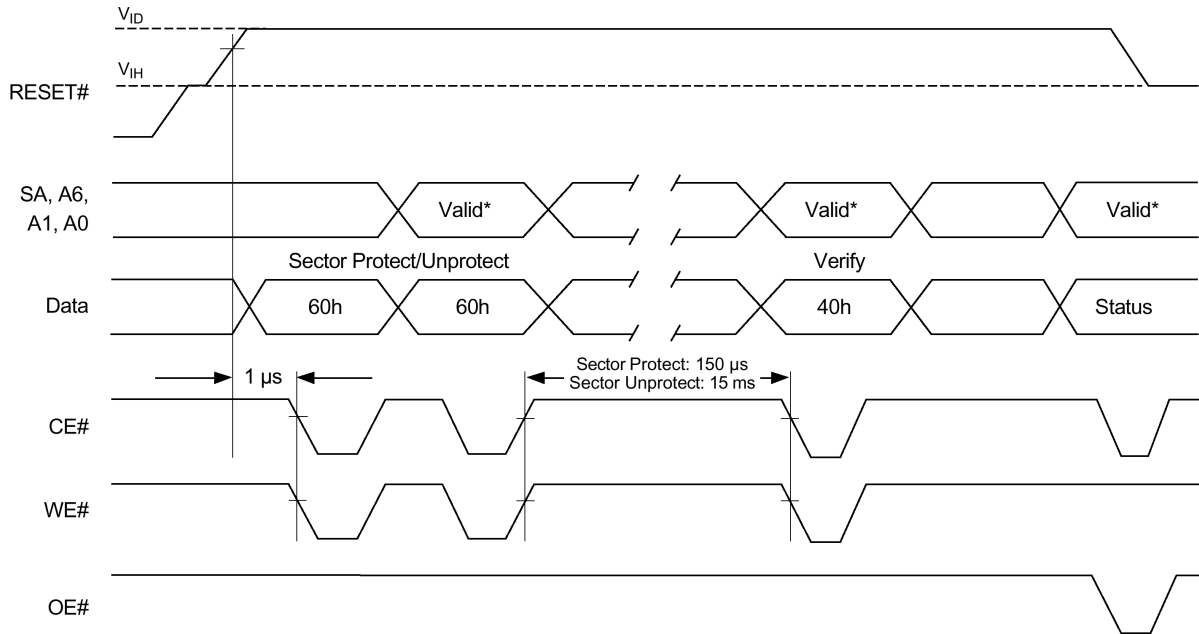
**U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)**



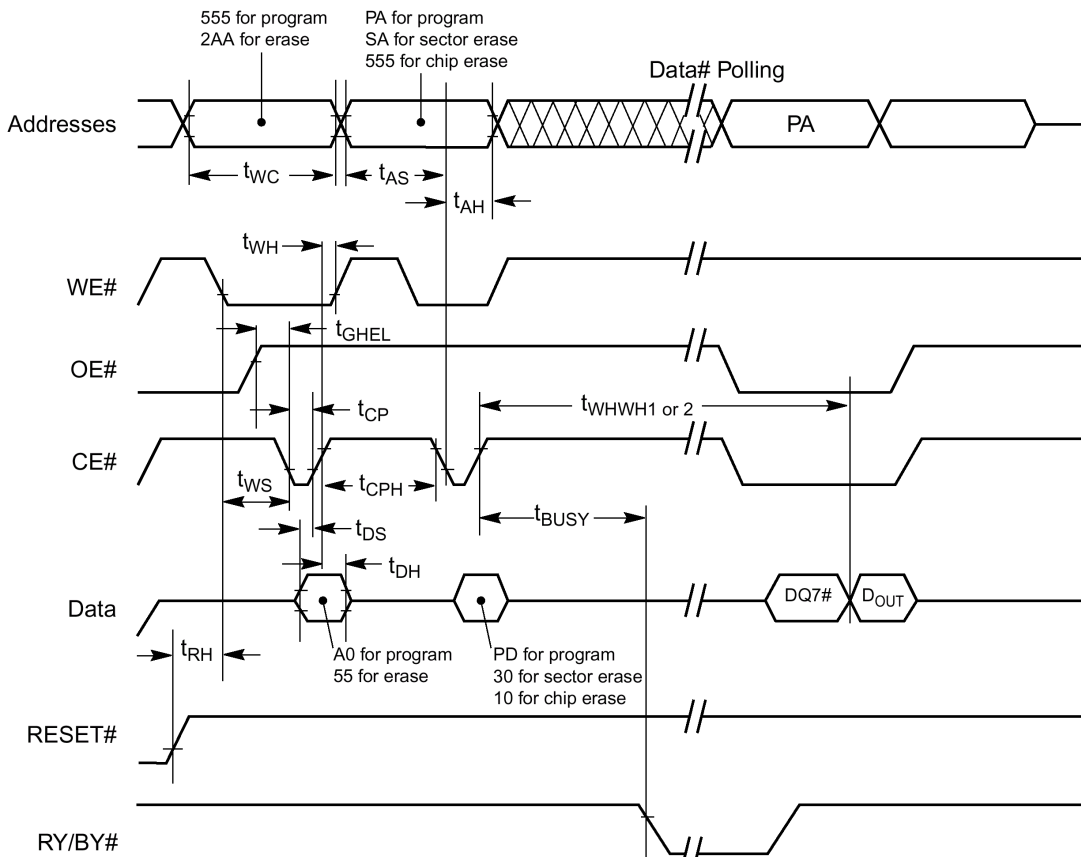
**U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)**



**U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM**

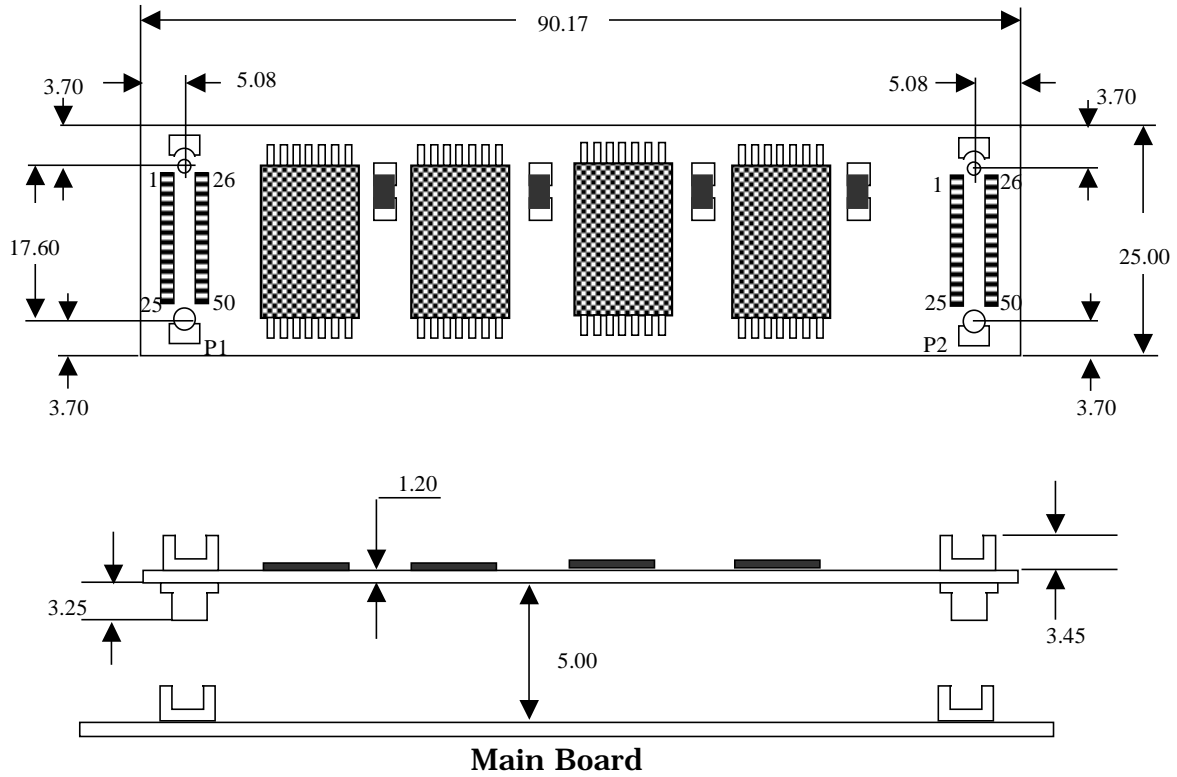


**U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS**



PACKAGE DIMENSIONS

UNIT: mm



-Connector

Part No. HMF8M8F4V

Top: 50-pin 0.6mm Pitch Free Height Plugs, AMP Part No. 316076-3

Bottom: 50-pin 0.6mm Pitch Free Height Receptacles, AMP Part No. 316077-3

**ORDERING INFORMATION**

Part Number	Density	Org.	Package	Speed	Vcc	Function
HMF8M8F4V	8MByte	8MX 8bit	100 Pin-MMC	80,90,120(ns)	3V	Bottom
HMF8M8F4VT	8MByte	8MX 8bit	100 Pin-MMC	80,90,120(ns)	3V	Top