APRIL 1997
Revision 2.0

LXT905

Universal Ethernet Interface Adapter

General Description

The LXT905 Universal Ethernet Interface Adapter is designed for IEEE 802.3 physical layer applications. It provides, in a single CMOS device, all the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.

LXT905 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link integrity testing and reversed polarity detection/correction. The LXT905 drives the 10BASE-T twisted-pair cable with only a simple isolation transformer. Integrated filters simplify the design work required for FCC compliant EMI performance.

The LXT905 is fabricated with an advanced process and requires only a single 5 or 3.3 volt power supply.

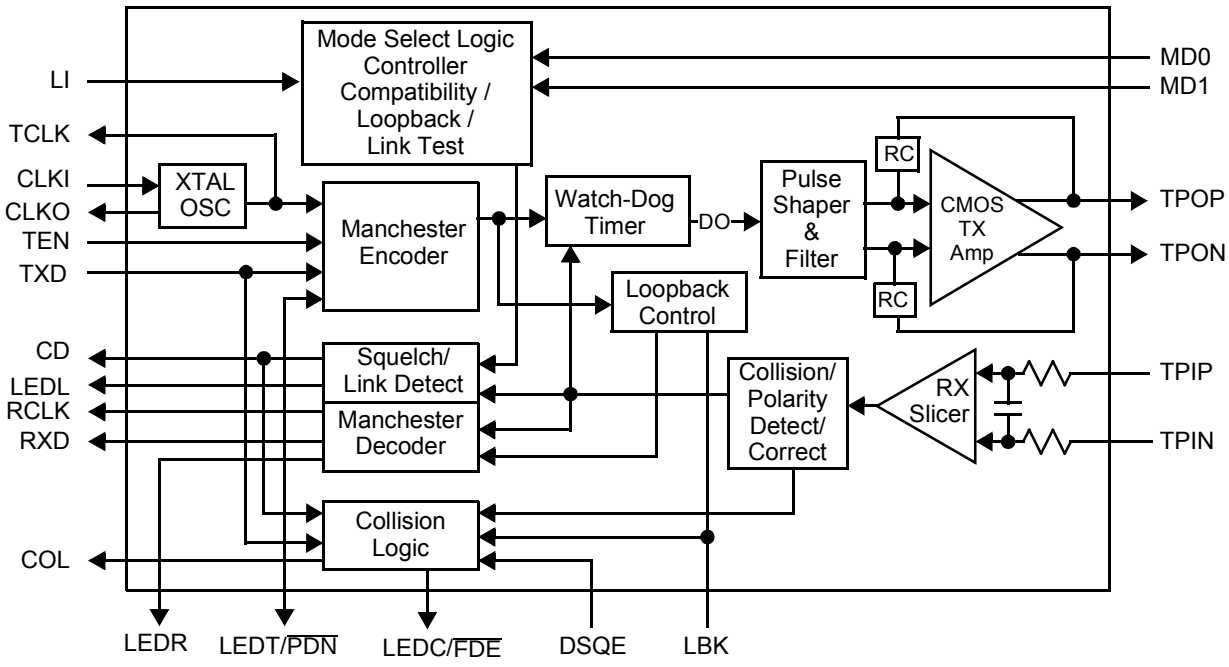
Applications

- Hub/Switched Dedicated LANs for 10BASE-T
- Desktop 10BASE-T LAN adapter boards
- Laptop and Portable applications

Features

- Transparent 3.3 V or 5 V operation
- Integrated filters – Simplifies FCC compliance
- Integrated Manchester encoder/decoder
- 10BASE-T compliant transceiver
- Automatic polarity correction
- Available in 28-pin PLCC and 32-pin LQFP packages
- SQE enable/disable
- Four LED drivers
- Full duplex capability
- Power-down mode with tristate

LXT905 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT905 Pin Assignments

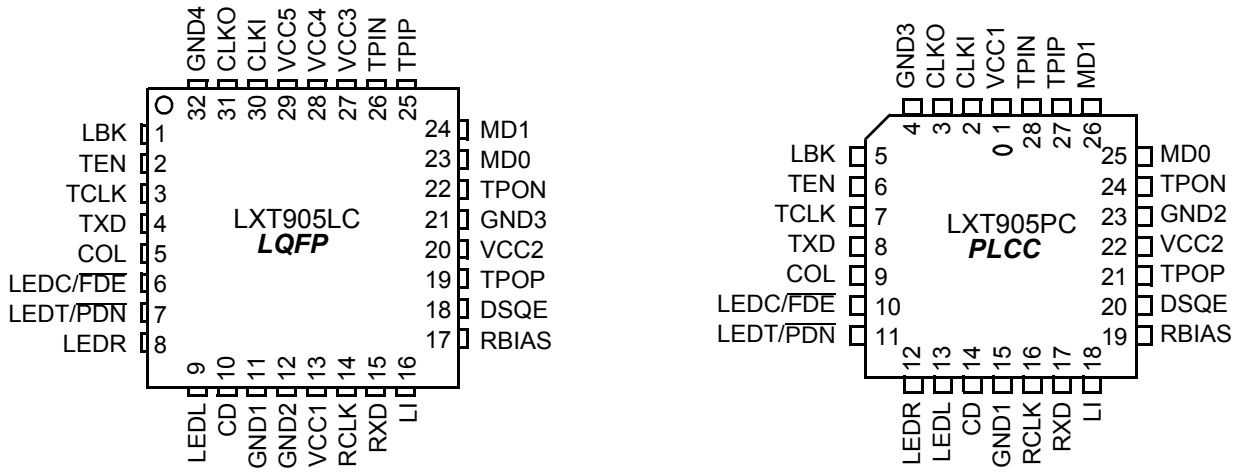


Table 1: LXT905 Signal Descriptions

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
13 20 27 28 29	1 22 – – –	VCC1 VCC2 VCC3 VCC4 VCC5	– – – – –	**Power Inputs 1 thru 5.** Power supply inputs of +5 volts or +3.3 volts.
30 31	2 3	CLKI CLKO	I O	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
11 12 21 32	15 23 4 –	GND1 GND2 GND3 GND4	– – – –	**Ground.**
1	5	LBK	I	**Loopback.** When High, forces internal loopback. Disables collision and the transmission of both data and link pulses. Pulled Low internally.
2	6	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK. Pulled Low internally.
3	7	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.
4	8	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD should be connected directly to the transmit data output of the controller. Pulled Low internally.
5	9	COL	O	**Collision Signal.** Output that drives the collision detect input of the controller.

Table 1: LXT905 Signal Descriptions – continued

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
6	10	LEDC/ FDE	O I	**LED Collision or Full Duplex Enable.** **LEDC** is an open drain driver for the collision indicator pulls Low during collision. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. **FDE** enables full duplex mode (external loopback) if tied Low externally. Pulled high internally.
7	11	LEDT/ $\overline{\text{PDN}}$	O I	**LED Transmit or Power Down.** **LEDT** is an open drain driver for the transmit indicator. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. Output is pulled Low during transmit. If externally tied Low, the LXT905 goes to power down state ($\overline{\textbf{PDN}}$). In Power-down Mode, all logic inputs and outputs are tristated.
8	12	LEDR	O	**LED Receive.** Open drain driver for the receive indicator LED. LED "on" (*i.e.*, Low output) time is extended by approximately 100 ms. Output is pulled Low during receive. Pulled High internally.
9	13	LEDL	O	**LED Link.** Open drain driver for link integrity indicator. Output is pulled Low during link test pass. Pulled High internally.
10	14	CD	O	**Carrier Detect.** An output for notifying the controller that activity exists on the network.
14	16	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
15	17	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller.
16	18	LI	I	**Link Enable.** Controls link integrity test; enabled when LI is High, disabled when LI is Low.
17	19	RBIAS	I	**Bias Circuitry.** A 7.5 kΩ 1% resistor to ground at this pin controls operating circuit bias.
18	20	DSQE	I	**SQE Disable.** When DSQE is High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled. SQE should be disabled for normal operation in Hub/Switch/Repeater applications. Pulled Low internally.
19 22	21 24	TPOP TPON	O O	**Twisted Pair Outputs.** Differential outputs to the twisted-pair cable. The outputs are pre-equalized.
23 24	25 26	MDO MDI	I I	**Mode Select 0 and 1.** Mode select pins determine controller compatibility mode in accordance with Table 2. Pulled Low internally.
25 26	27 28	TPIP TPIN	I I	**Twisted-Pair Inputs.** A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.

FUNCTIONAL DESCRIPTION

Introduction

The LXT905 Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with 10BASE-T twisted-pair networks.

The LXT905 interfaces a back end controller to a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the two basic interfaces, the LXT905 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT905 Transmit function refers to data transmitted by the back end to the twisted-pair network. The LXT905 Receive function refers to data received by the back end from the twisted-pair network. The LXT905 performs all required functions defined by the IEEE 802.3 10BASE-T MAU specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback.

Controller Compatibility Modes

The LXT905 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq, Motorola and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins MD0 and MD1 determine controller compatibility modes as listed in Table 2. Refer to the Test Specifications section for timing diagrams and parameters.

Transmit Function

The LXT905 receives NRZ data from the controller at the TXD input as shown in the block diagram, and passes it through a Manchester encoder. The encoded data is then transferred to the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure . The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT905 transmits link integrity test pulses on the TPO circuit (if LI is enabled and LBK is disabled).

Figure 2: LXT905 TPO Output Waveform

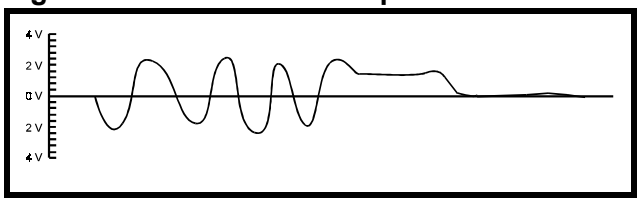


Table 2: Controller Compatibility Mode Options

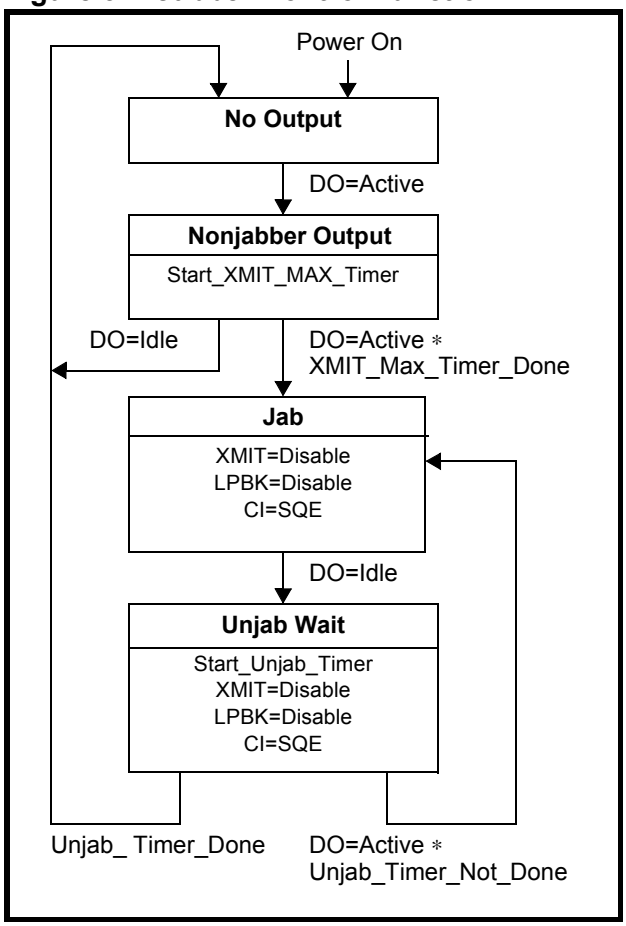
Controller Mode	MD1	MD0
Mode 1 - For Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2 - For Intel 82596 or compatible controllers[1]	High	Low
Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005)[2]	Low	High
Mode 4 - For National Semiconductor 8390 or compatible controllers (TI TMS380C26)	High	High

2. Refer to Level One Application Note 51 when designing with Intel controllers.
3. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL.

Jabber Control Function

Figure 3 is a state diagram of the LXT905 jabber control function. The LXT905 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions and activates the COL pin. Once the LXT905 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: Jabber Control Function

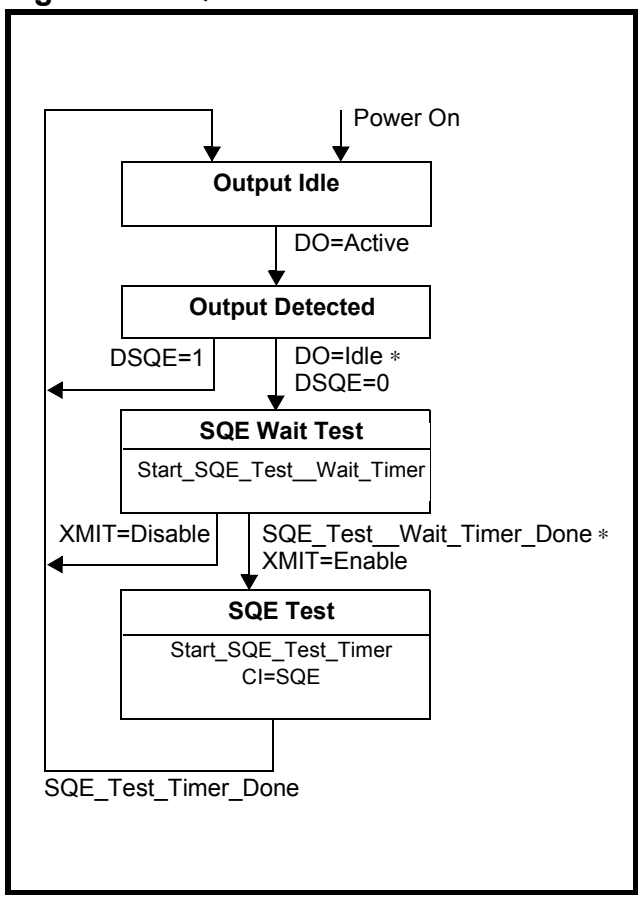


SQE Function

The LXT905 supports the signal quality error (SQE) function as shown in Figure 4. After every successful transmission on the 10BASE-T network, the LXT905 transmits the SQE signal for 10 bit times (BT) ± 5BT on the COL pin of the device.

The SQE can be disabled for repeater/switch applications. When DSQE is set High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled.

Figure 4: SQE Function



Receive Function

The LXT905 receive function acquires timing and data from the twisted-pair network (the TPI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level with proper timing.

If the differential signal at the TPI circuit inputs falls below 85% of the threshold level (unsquelched) for 8 bit times (typical), the LXT905 receive function enters the idle state. The LXT905 automatically corrects reversed polarity on the TPI circuit.

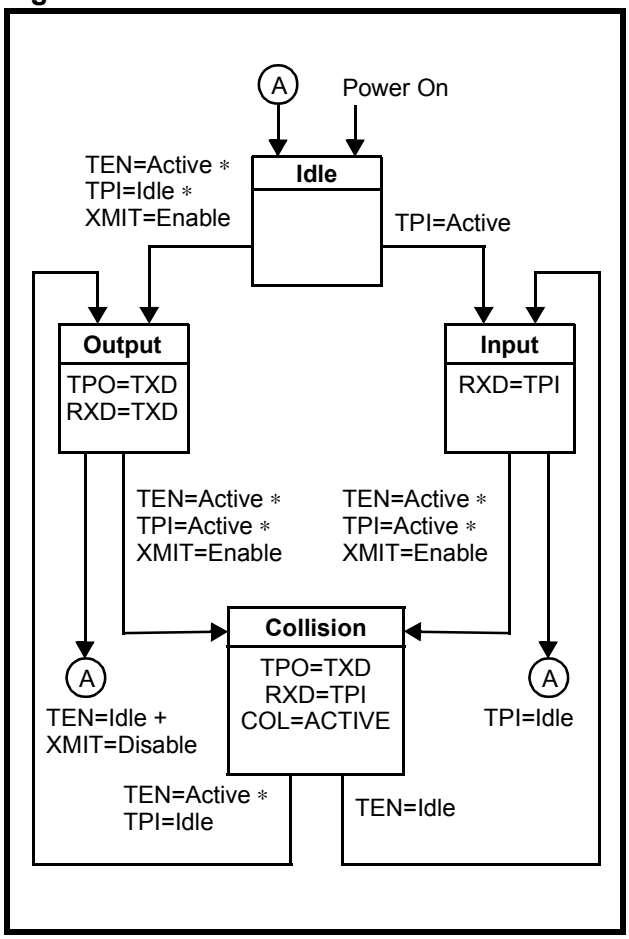
Polarity Reverse Function

The LXT905 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. If Link Integrity testing is disabled, polarity detection is based only on received data. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle. Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT905 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. Polarity correction is always enabled.

Collision Detection Function

A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT905 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT905 collision detection function.

Figure 5: Collision Detection Function



Loopback Function

The LXT905 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port, as well as a forced loopback function. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT905 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail, jabber, and full duplex states. Loopback is always enabled during the forced loopback state.

The LXT905 provides an additional loopback function. External loopback mode, useful for system-level testing, is controlled by the LEDC/$\overline{\text{FDE}}$ pin. With both LEDC/$\overline{\text{FDE}}$ and LBK Low, the LXT905 device:

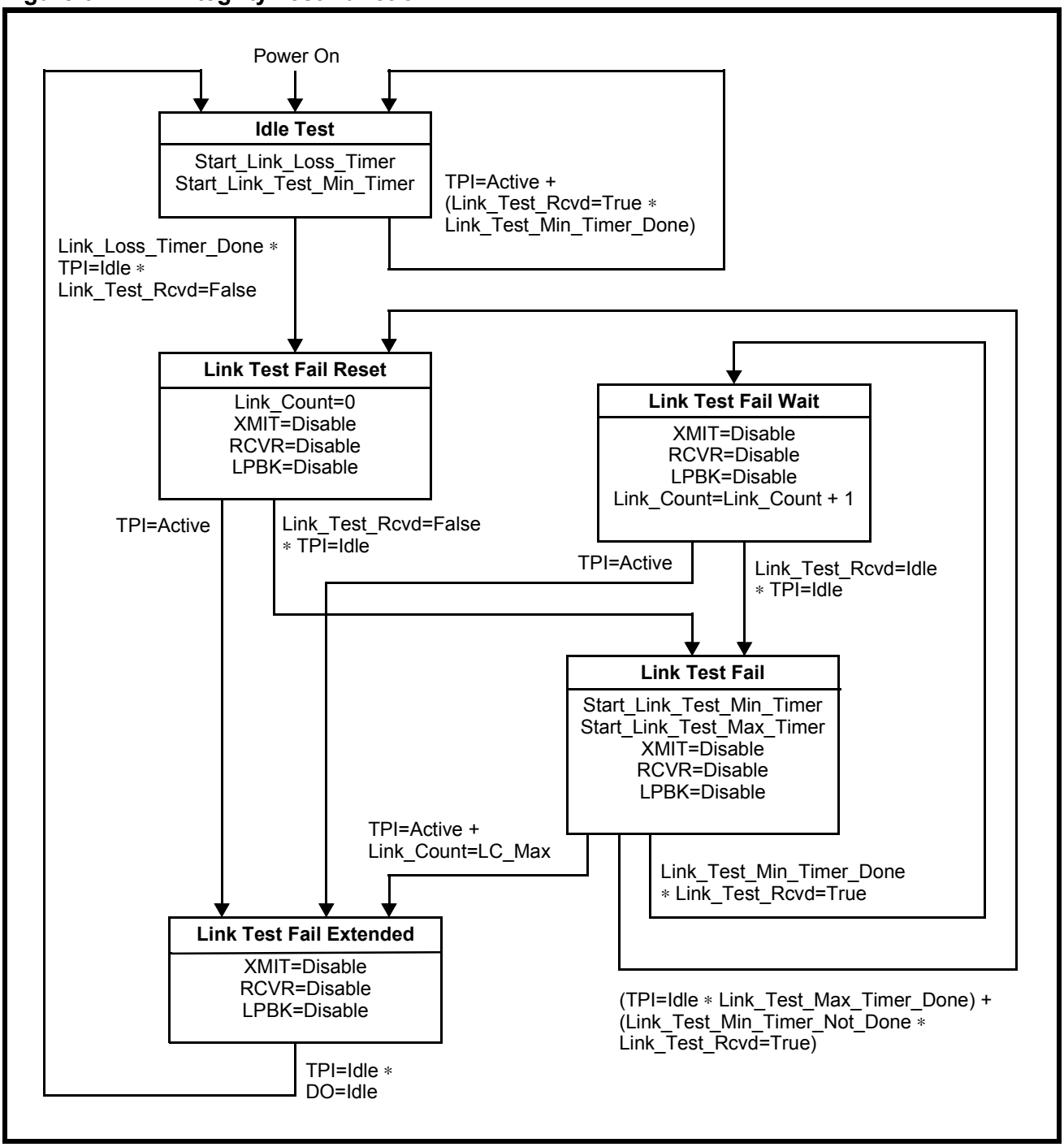
- disables internal loopback circuits
- disables SQE
- disables Collision Detection
- enables Full Duplex Mode

This allows external loopback testing.

Link Integrity Test Function

Figure 6 is a state diagram of the LXT905 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 18 (LI) is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50~150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT905 ignores any link integrity pulse with interval less than 2~7 ms. The LXT905 will remain in the Link Fail State until it detects either a serial data packet or two or more link integrity pulses.

Figure 6: Link Integrity Test Function



APPLICATION INFORMATION

Introduction

Figures 7 through 9 show typical LXT905 applications. These diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins; Transmit Data (TXD), Transmit Clock (TCLK) Transmit Enable (TEN), Receive Data (RXD), Receive Clock (RCLK), Collision Signal (COL) and Carrier Detect (CD) pins are at the upper left.

Power and ground pins are at the bottom of each diagram. VCC1 and VCC2 use a single power supply with decoupling capacitors installed between the power and ground busses. VCC may be powered by a 5V or 3.3V supply.

Twisted-Pair Interface

The Twisted-Pair interface (TPOP/N and TPIP/N) is at the upper right. The I/O pairs have impedance matching resistors for 100Ω UTP but no external filters are required.

RBIAS Pin

The RBIAS pin sets the levels for the LXT905 output drivers. The LXT905 requires a 7.5kΩ, 1% resistor directly connected between the RBIAS pin and ground. This resistor should be located as close to the device as possible. Keep the traces as short as possible and isolated from all other high speed signals.

Crystal Information

Based on limited evaluation, Table 3 lists some of the suitable crystals. Designers should test and validate all crystals before committing to a specific component.

Table 3: Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

Magnetic Information

The LXT905 requires a 1:1 turns ratio for the receive transformer and a 1:2 turns ratio for the transmit transformer. Table 4 lists transformers suitable for the applications described in this data sheet. Designers are advised to test and validate all magnetics before committing to a specific component.

Table 4: Suitable Magnetics

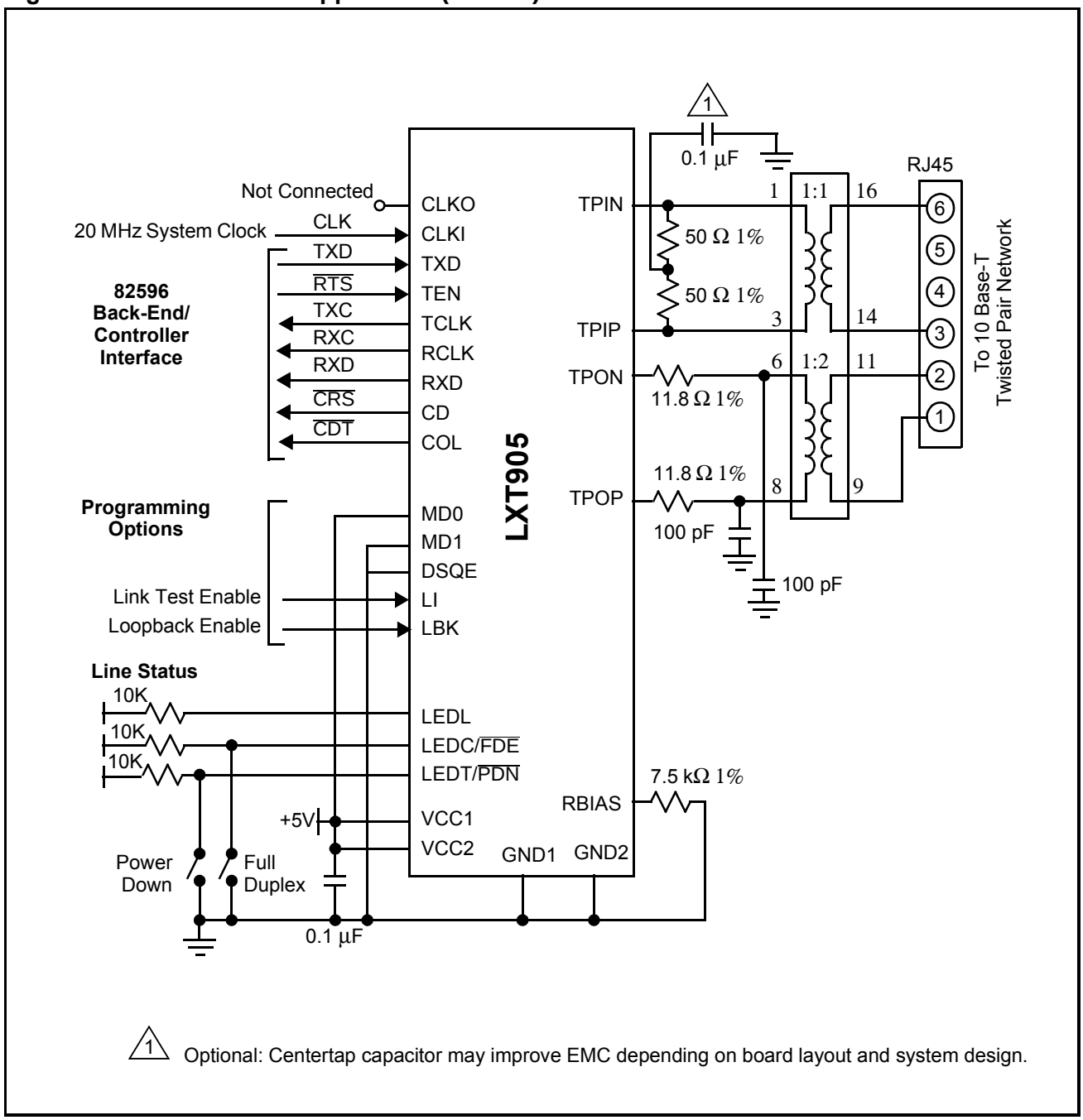
Manufacturer	Part Number	
	Surface Mount	Thru-hole
Valor	ST4160	–
	ST4202	–
	ST4167	–
HALO	TG74-1406N1	TG74-1406Q
	TG75-1406N	TG74-1406K
Fil-Mag	23Z441SM	23Z441

Typical 10BASE-T Application

Figure 7 is a typical LXT905 application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. With MD0 tied high and MD1 grounded, the LXT905 logic and framing are set to Mode 2 (compatible with Intel 82596 controllers*). Connect 20 MHz system clock input at CLKI. (Leave CLKO open.) The LI pin externally controls the link test function.

*Refer to Level One Application Note 51 when designing with Intel controllers.

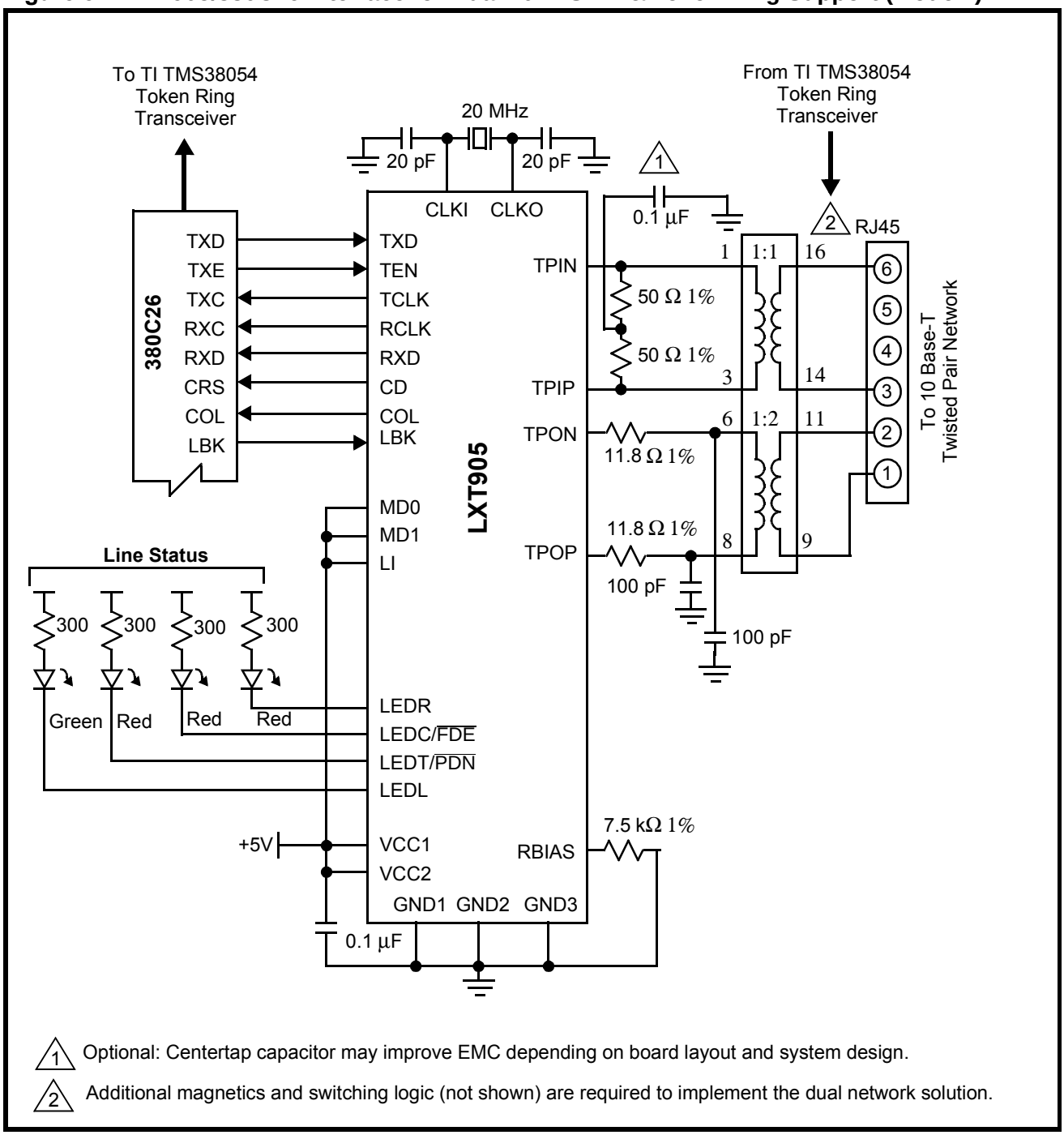
Figure 7: Intel Controller Application (Mode 2)



Dual Network Support - 10BASE-T and Token Ring

Figure 8 shows the LXT905 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C26, both the LXT905 and a TMS38054 Token Ring transceiver can be tied to a single RJ45 allowing dual network support from a single connector.

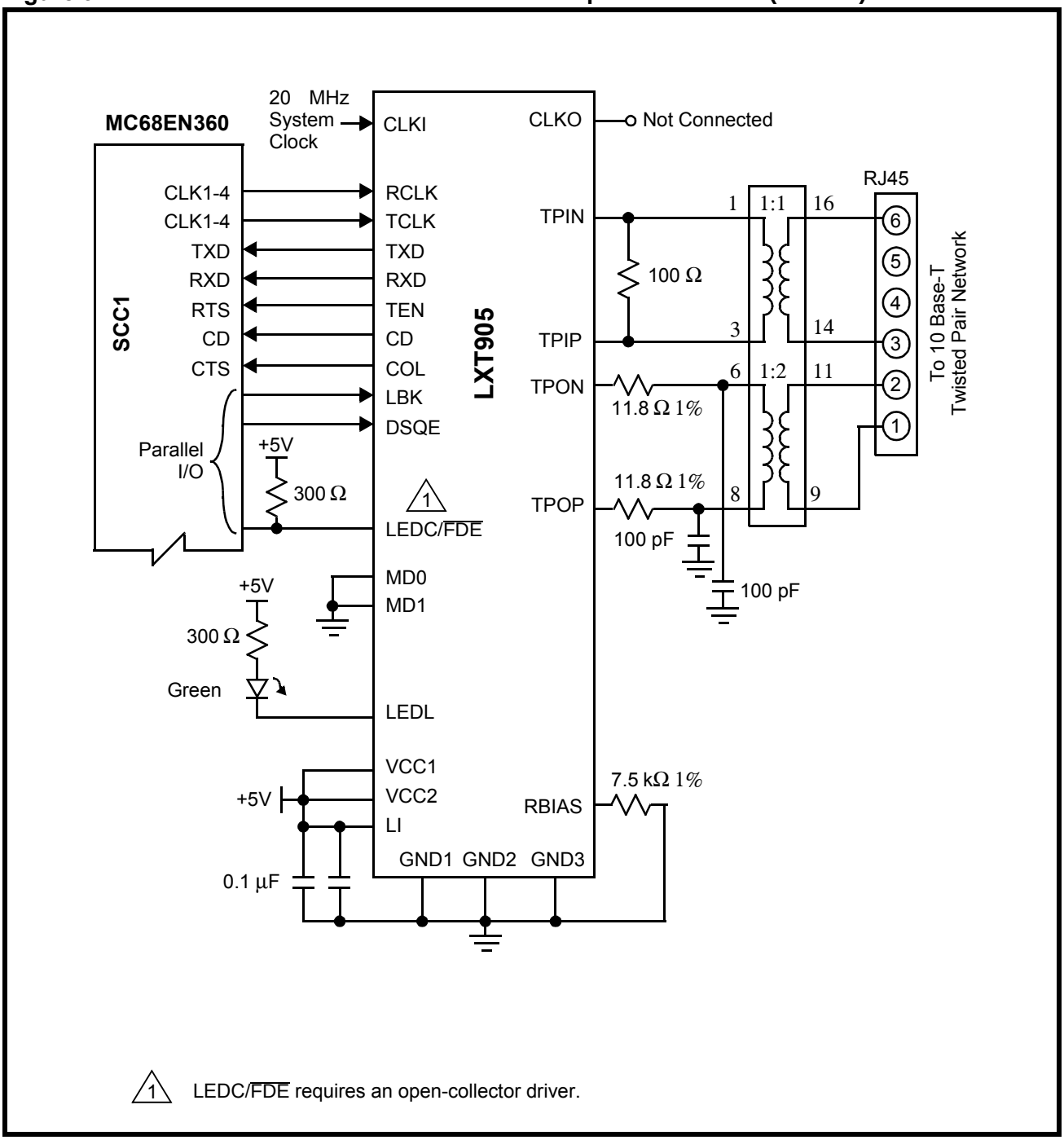
Figure 8: LXT905/380C26 Interface for Dual 10BASE-T & Token Ring Support (Mode 4)



Simple 10BASE-T Connection

Figure 9 shows a simple 10BASE-T application using an LXT905 transceiver and a Motorola MC68EN360. The MC68EN360 is compatible with Mode 1 (MD0 and MD1 both low).

Figure 9: LXT905/MC68EN360 Interface for Full Duplex 10BASE-T (Mode 1)



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 13 and Figures 10 through 25 represent the performance specifications of the LXT905 and are guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	+6	V
Ambient operating temperature	TOP	0	+70	ºC
Storage temperature	TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	3.135	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	ºC	

1. Voltage is with respect to ground unless specified otherwise.

Table 7: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage[2]	VIL	–	–	0.8	V	
Input high voltage[2]	VIH	2.0	–	–	V	
Output low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
	VOL	–	–	10	%VCC	IOL < 10 µA
Output low voltage (Open drain LED driver)	VOLL	–	–	0.7	%VCC	IOLL = 10 mA
Output high voltage	VOH	2.4	–	–	V	IOH = 40 µA
	VOH	90	–	–	%VCC	IOH < 10 µA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 7: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output rise time TCLK & RCLK	CMOS	–	–	3	15	ns	CLOAD = 20 pF
	TTL	–	–	2	15	ns	
Output fall time TCLK & RCLK	CMOS	–	–	3	15	ns	CLOAD= 20 pF
	TTL	–	–	2	15	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	
Supply current	Normal Mode	ICC	–	40	80	mA	Idle Mode
		ICC	–	70	100	mA	Transmitting on TP
	Power Down Mode	ICC	–	0.01	1	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 8: TP Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance	ZIN	–	24	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	VDS	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 9: Switching Characteristics (Over Recommended Range)

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 10: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units
Decoder acquisition time		tDATA	–	1300	1500	ns
CD turn-on delay		tCD	–	400	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3 and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3 and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3)		tsws	–	±100	–	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	–	5	bit times
Rcv data through-put delay	Max	tRD	400	375	375	375	ns
CD turn-off delay [2]	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off [3]	Typical[1]	tIFG	5	50	–	–	bit times
RCLK switching delay after CD off	Typical[1]	tswe	–	–	120 (±80)	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. CD Turnoff delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.
3. Blocking of Carrier Detect is disabled during full duplex operation.

Table 12: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay	tSTUD	–	350	450	ns
Transmit through-put delay	tTPD	–	338	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

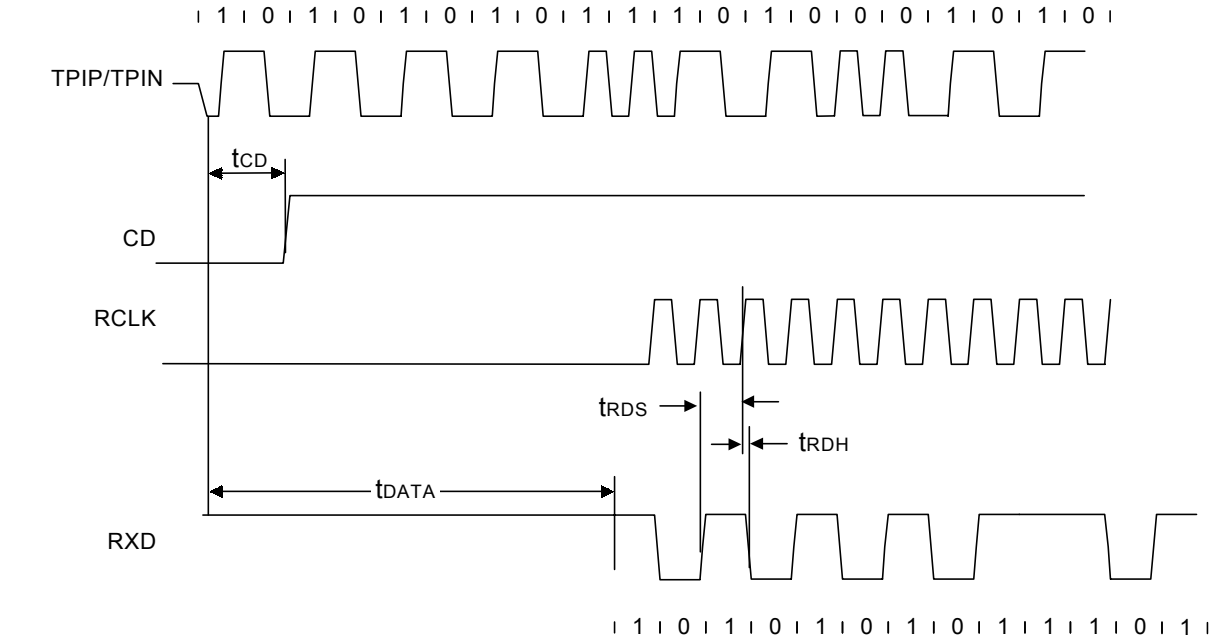
Table 13: Miscellaneous Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL (SQE) Delay after TEN off [2]	tSQED	0.65	–	1.6	µs
COL (SQE) Pulse Duration[2]	tSQEP	500	–	1500	ns
Power Down recovery time	tPDR	–	25	–	ms

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. When SQE is enabled (DSQE is Low).

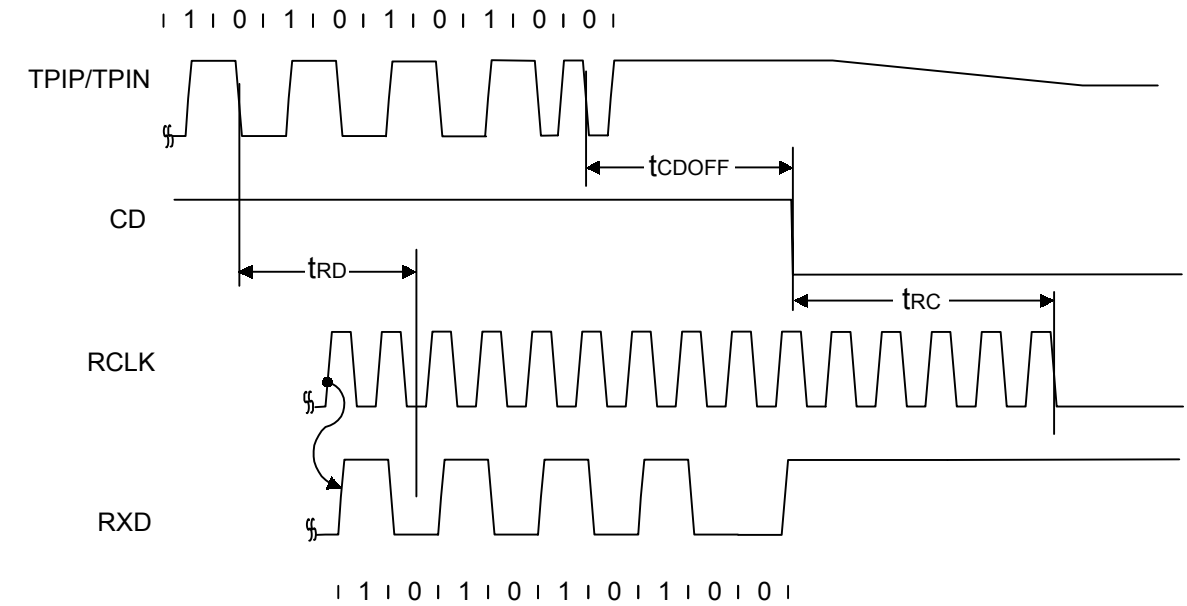
Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low) *Figures 10 through 13*

Figure 10: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 11: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 12: Mode 1 Transmit Timing

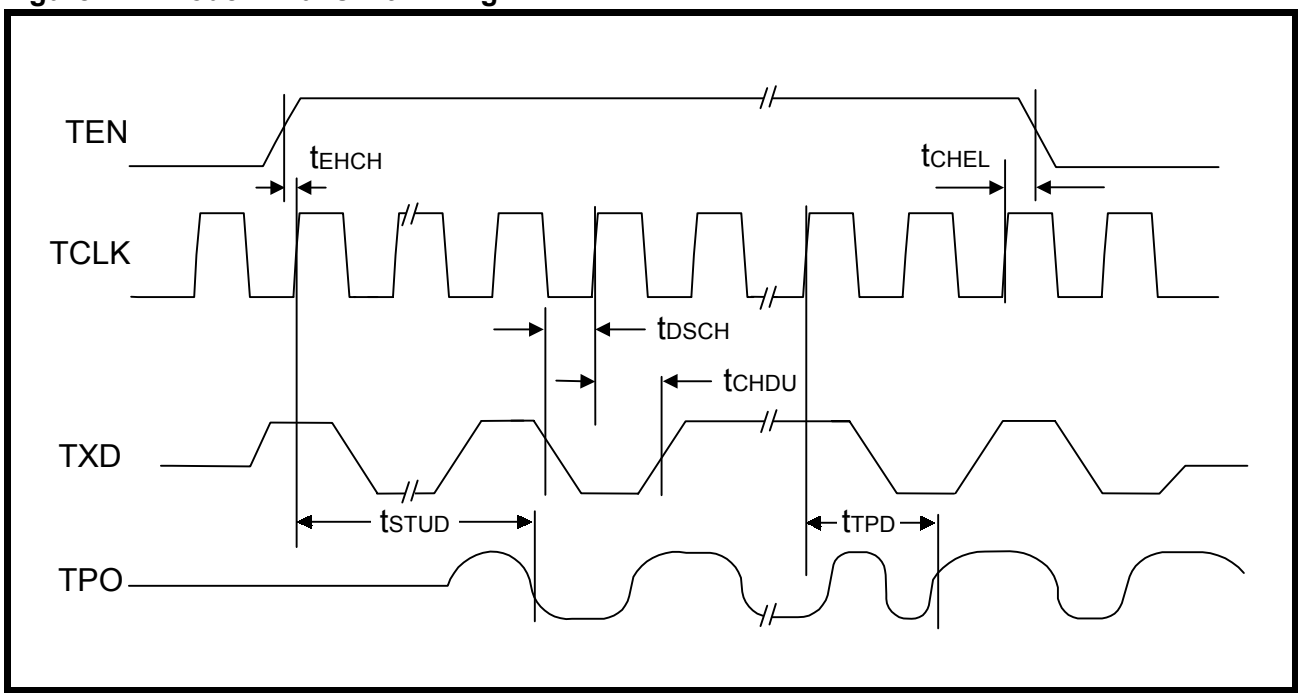
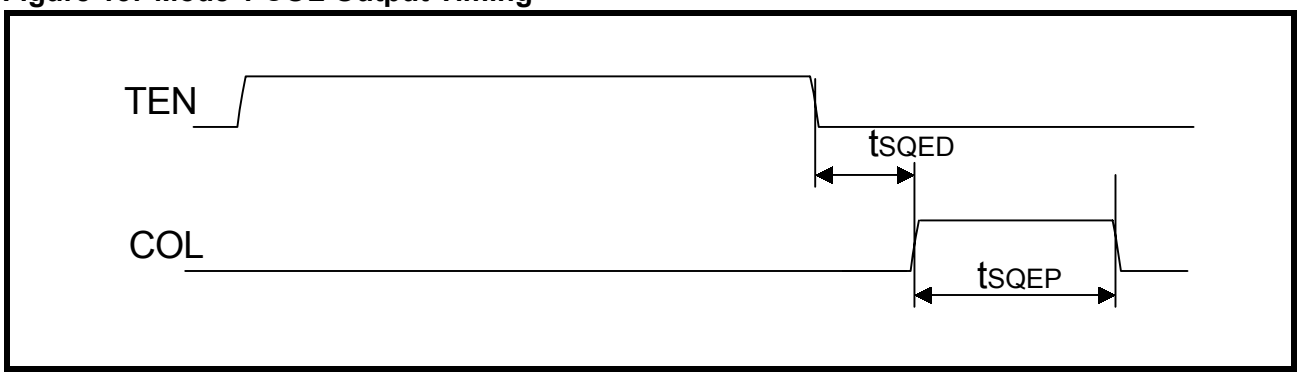
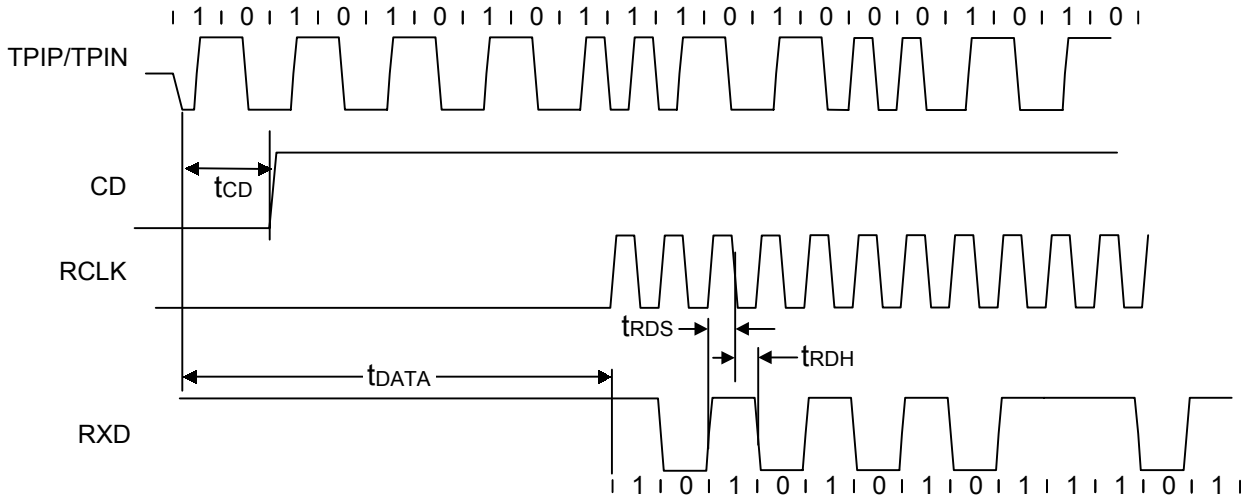


Figure 13: Mode 1 COL Output Timing



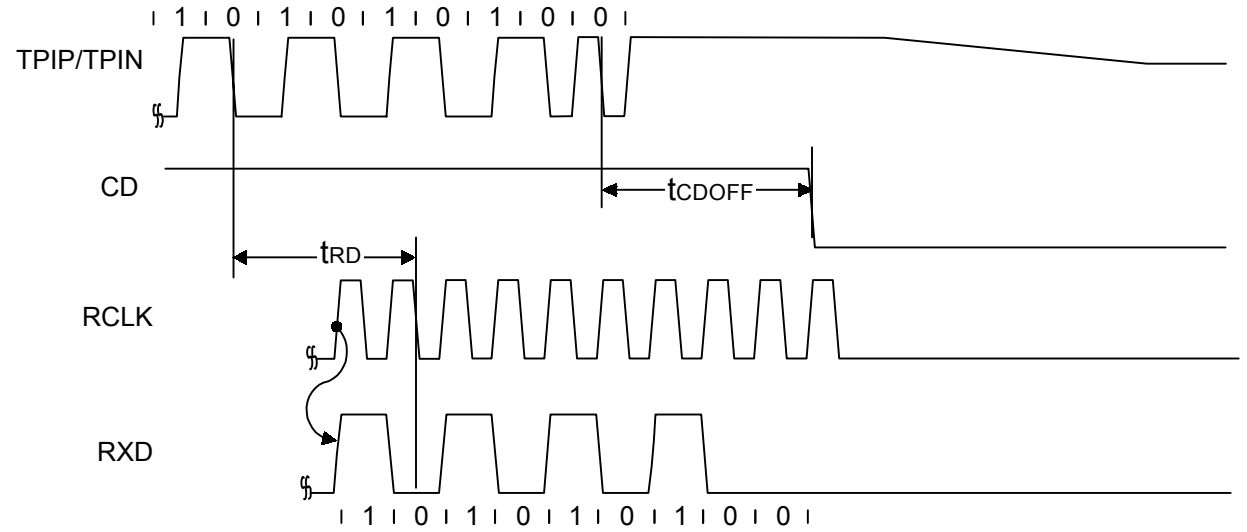
Timing Diagrams for Mode 2 (MD1=Low, MD0=High) *Figures 14 through 17*

Figure 14: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 15: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 2 Transmit Timing

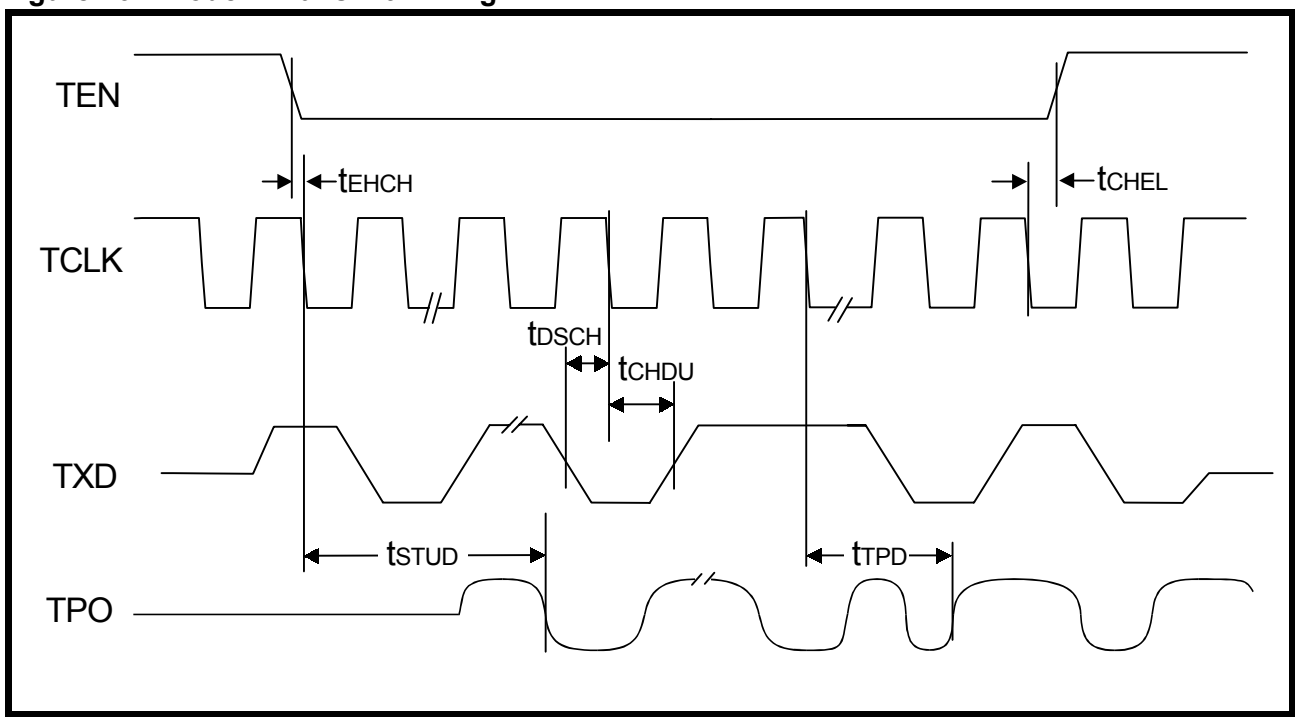
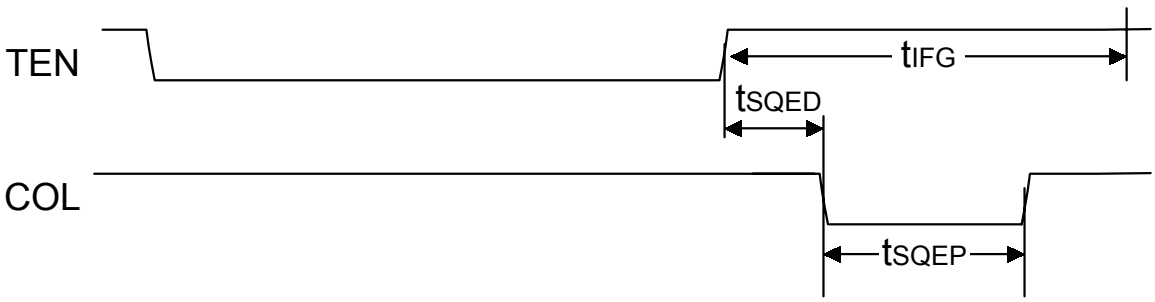


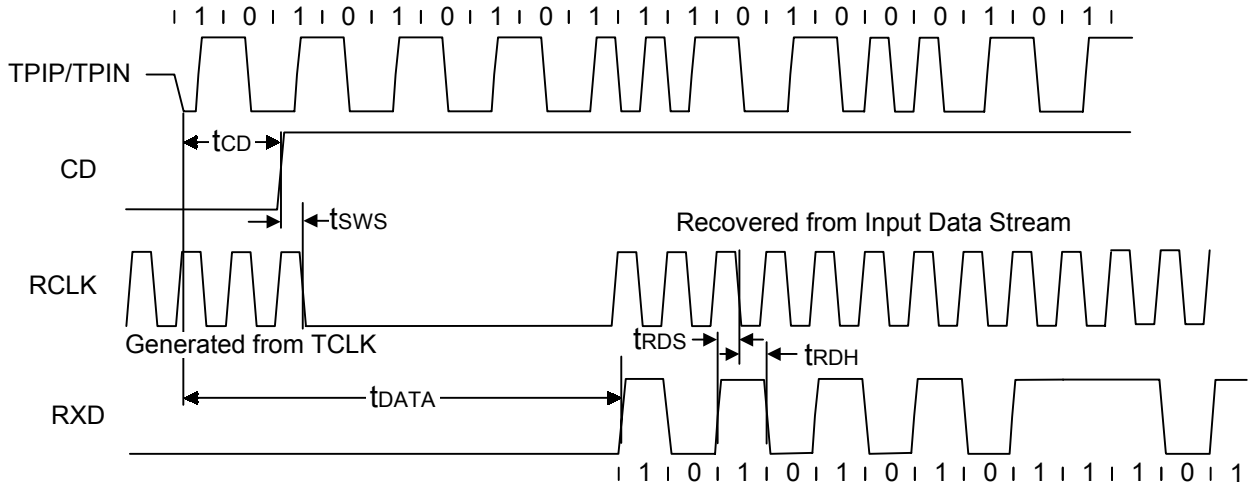
Figure 17: Mode 2 COL Output Timing



NOTE:
1. CD output is disabled for a maximum of 55 bit times after TEN turns off.

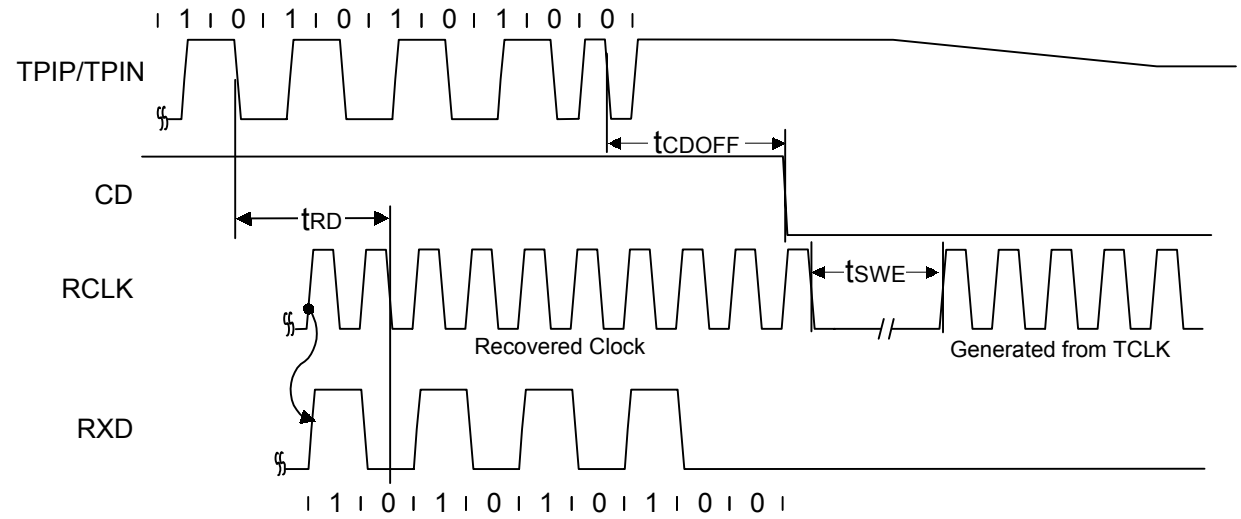
Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low) *Figures 18 through 21*

Figure 18: Mode 3 RCLK/Start-of-Frame Timing



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 19: Mode 3 RCLK/End-of-Frame Timing



Note:
1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 20: Mode 3 Transmit Timing

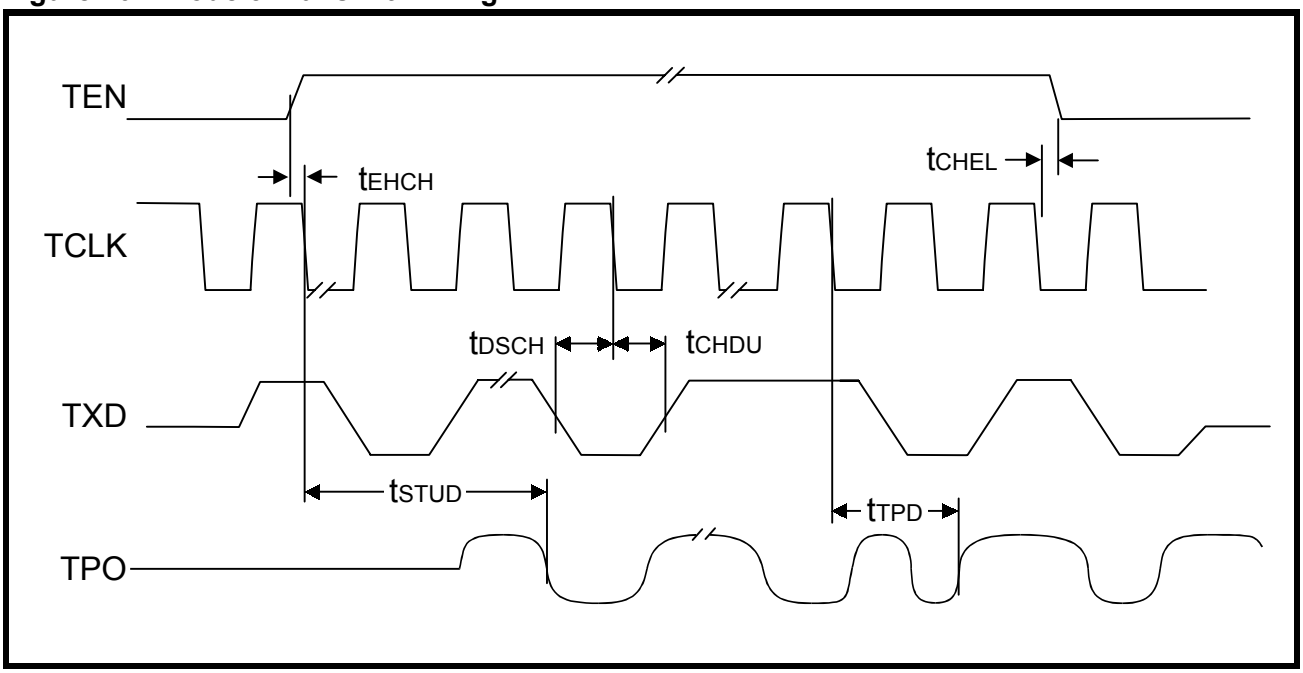
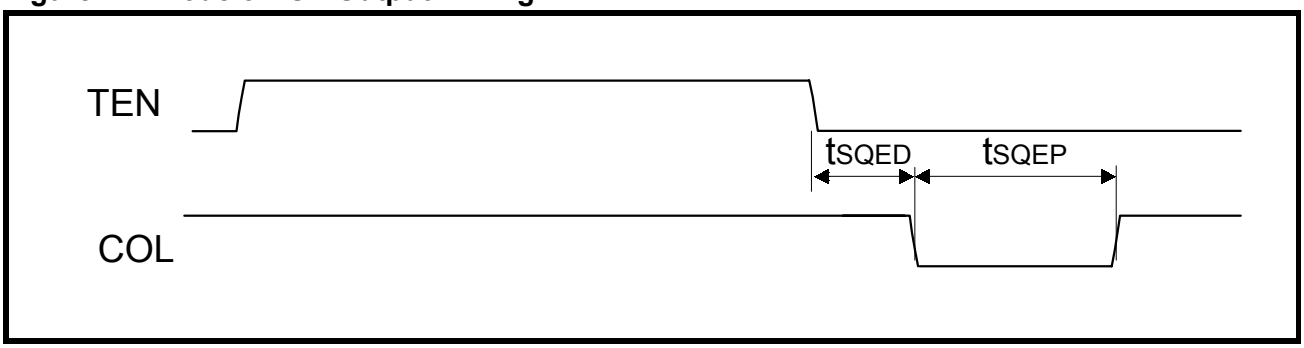
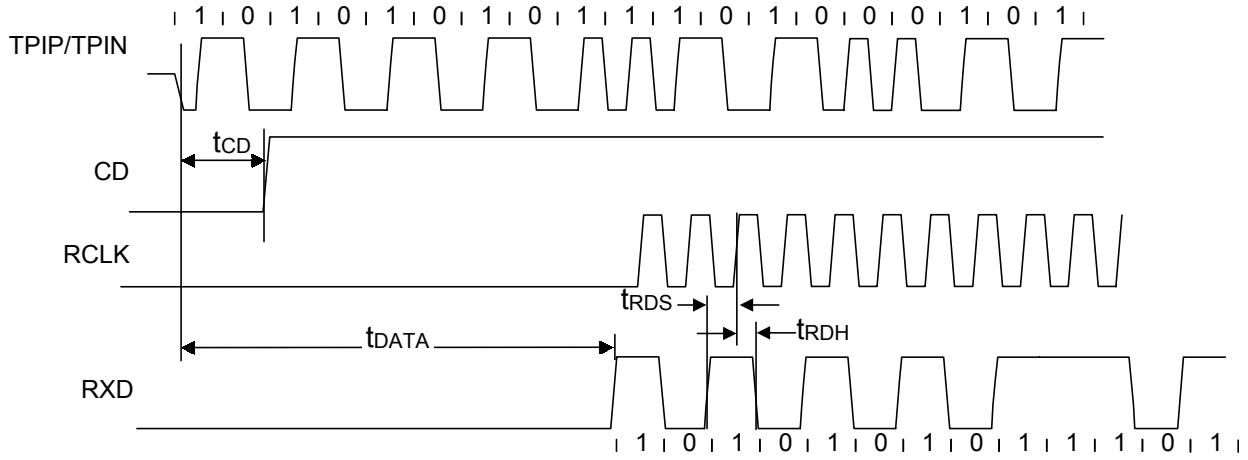


Figure 21: Mode 3 COL Output Timing



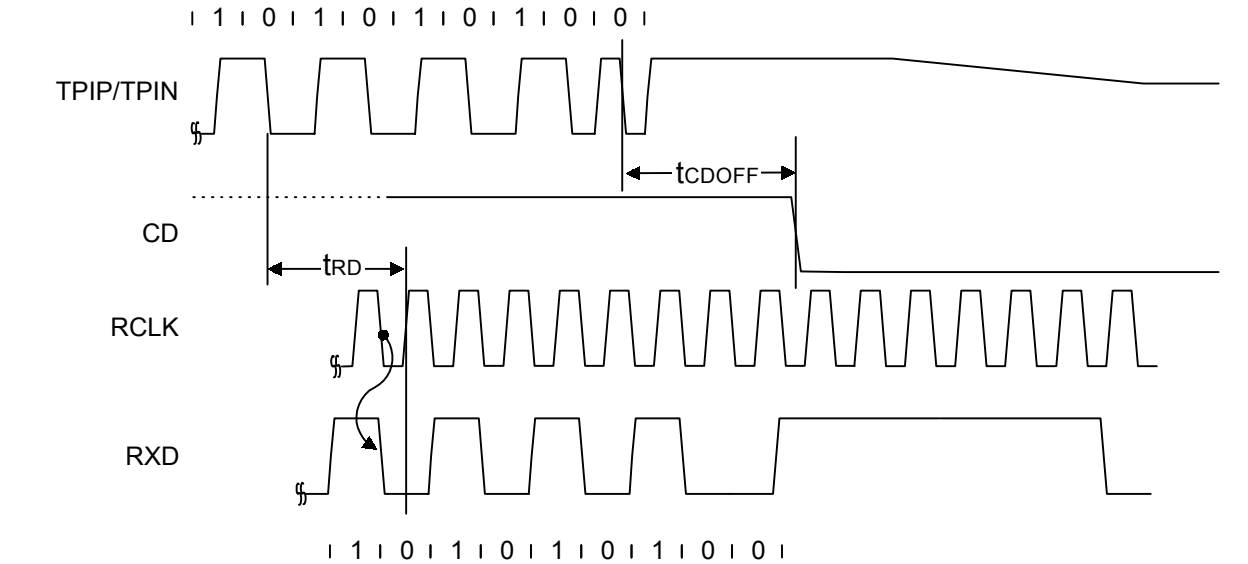
Timing Diagrams for Mode 4 (MD1 = High, MD0 = High) *Figures 22 through 25*

Figure 22: Mode 4 RCLK/Start-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 23: Mode 4 RCLK/End-of-Frame Timing



Note:
1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 24: Mode 4 Transmit Timing

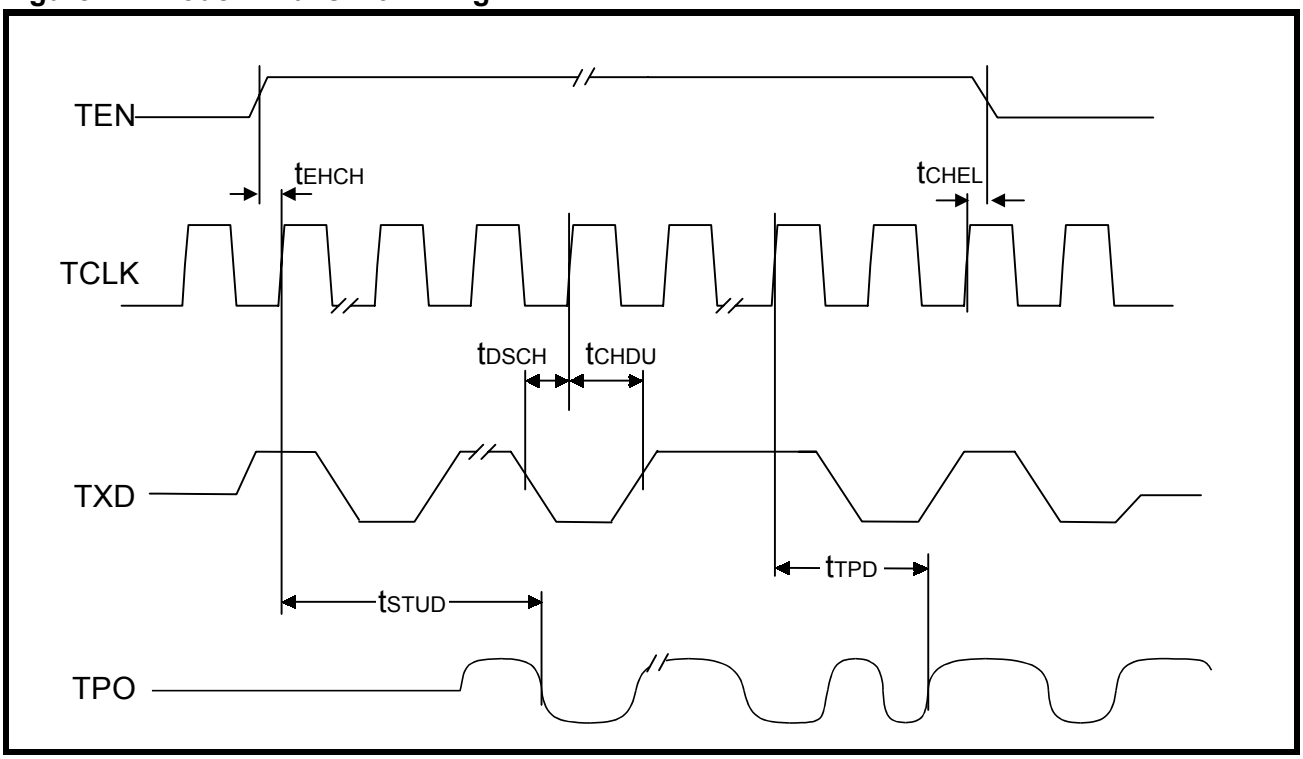
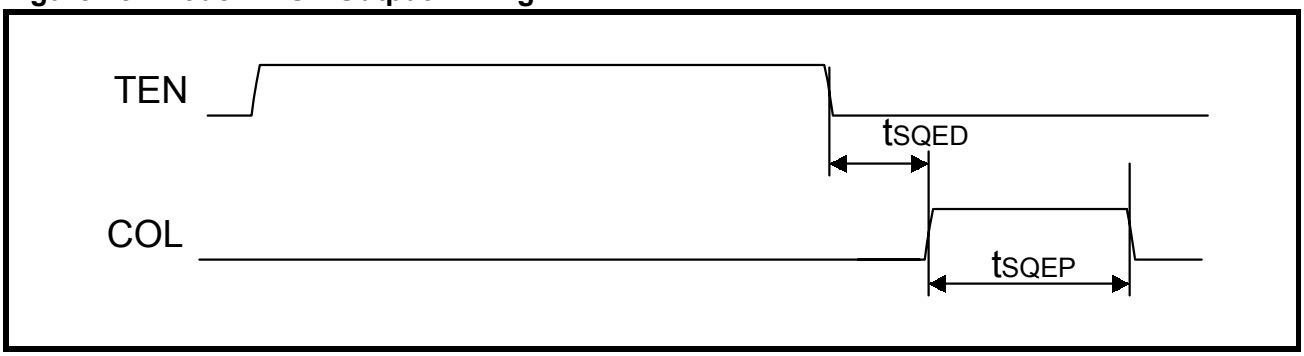


Figure 25: Mode 4 COL Output Timing



NOTES