# 256MB - 32Mx72 SDRAM UNBUFFERED

## FEATURES

- PC100 and PC133 Compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 144 Pin SO-DIMM JEDEC
  - Package height options:
    AD1: 27.94 (1.1")

## DESCRIPTION

The W3DG7232V is a 32Mx72 synchronous DRAM module which consists of nine 32Mx8 SDRAM components in TSOP II package, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

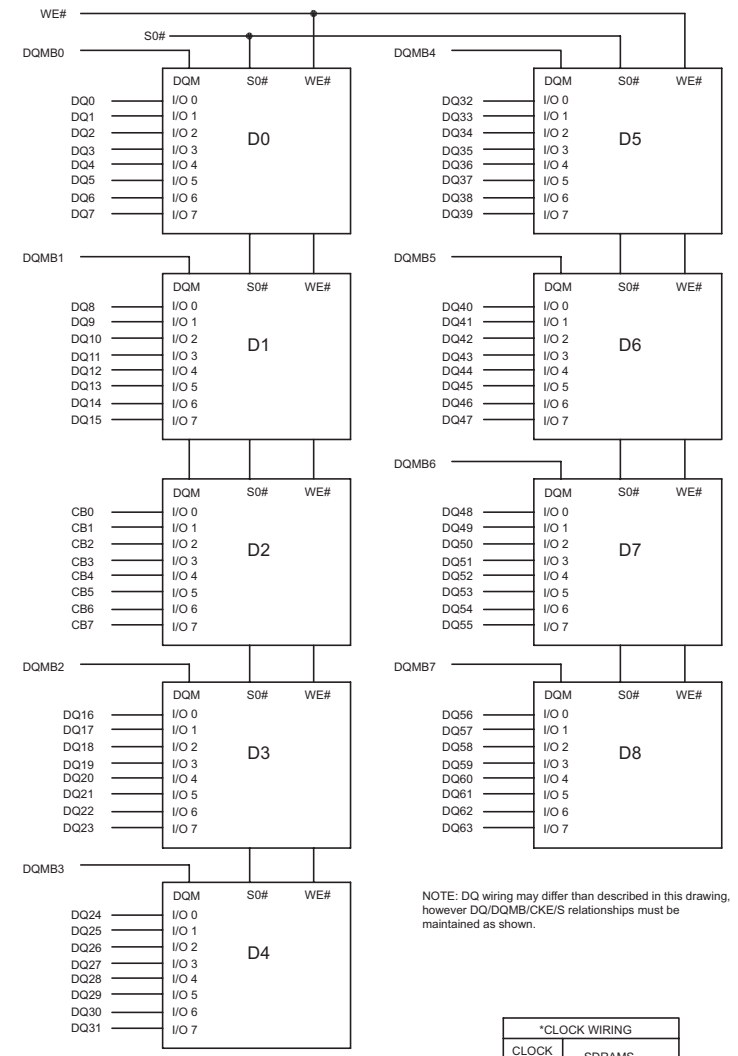
### PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

| PIN | FRONT | PIN | BACK | PIN | FRONT | PIN | BACK | PIN | FRONT | PIN | BACK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Vss | 2 | Vss | 49 | DQ13 | 50 | DQ45 | 97 | DQ22 | 98 | DQ54 |
| 3 | DQ0 | 4 | DQ32 | 51 | DQ14 | 52 | DQ46 | 99 | DQ23 | 100 | DQ55 |
| 5 | DQ1 | 6 | DQ33 | 53 | DQ15 | 54 | DQ47 | 101 | Vcc | 102 | Vcc |
| 7 | DQ2 | 8 | DQ34 | 55 | Vss | 56 | Vss | 103 | A6 | 104 | A7 |
| 9 | DQ3 | 10 | DQ35 | 57 | CB0 | 58 | CB4 | 105 | A8 | 106 | BA0 |
| 11 | Vcc | 12 | Vcc | 59 | CB1 | 60 | CB5 | 107 | Vss | 108 | Vss |
| 13 | DQ4 | 14 | DQ36 | 61 | CLK0 | 62 | CKE0 | 109 | A9 | 110 | BA1 |
| 15 | DQ5 | 16 | DQ37 | 63 | Vcc | 64 | Vcc | 111 | A10 | 112 | A11 |
| 17 | DQ6 | 18 | DQ38 | 65 | RAS# | 66 | CAS# | 113 | Vcc | 114 | Vcc |
| 19 | DQ7 | 20 | DQ39 | 67 | WE# | 68 | NC | 115 | DQMB2 | 116 | DQMB6 |
| 21 | Vss | 22 | Vss | 69 | SO# | 70 | A12 | 117 | DQMB3 | 118 | DQMB7 |
| 23 | DQMB0 | 24 | DQB4 | 71 | NC | 72 | NC | 119 | Vss | 120 | Vss |
| 25 | DQMB1 | 26 | DQB5 | 73 | NC | 74 | CLK1 | 121 | DQ24 | 122 | DQ56 |
| 27 | Vcc | 28 | Vcc | 75 | Vss | 76 | Vss | 123 | DQ25 | 124 | DQ57 |
| 29 | A0 | 30 | A3 | 77 | CB2 | 78 | CB6 | 125 | DQ26 | 126 | DQ58 |
| 31 | A1 | 32 | A4 | 79 | CB3 | 80 | CB7 | 127 | DQ27 | 128 | DQ59 |
| 33 | A2 | 34 | A5 | 81 | Vcc | 82 | Vcc | 129 | Vcc | 130 | Vcc |
| 35 | Vss | 36 | Vss | 83 | DQ16 | 84 | DQ48 | 131 | DQ28 | 132 | DQ60 |
| 37 | DQ8 | 38 | DQ40 | 85 | DQ17 | 86 | DQ49 | 133 | DQ29 | 134 | DQ61 |
| 39 | DQ9 | 40 | DQ41 | 87 | DQ18 | 88 | DQ50 | 135 | DQ30 | 136 | DQ62 |
| 41 | DQ10 | 42 | DQ42 | 89 | DQ19 | 90 | DQ51 | 137 | DQ31 | 138 | DQ63 |
| 43 | DQ11 | 44 | DQ43 | 91 | VSS | 92 | Vss | 139 | Vss | 140 | Vss |
| 45 | Vcc | 46 | Vcc | 93 | DQ20 | 94 | DQ52 | 141 | SDA | 142 | SCL |
| 47 | DQ12 | 48 | DQ44 | 95 | DQ21 | 96 | DQ53 | 143 | Vcc | 144 | Vcc |

### PIN NAMES

| | |
|---|---|
| A0 – A12 | Address input (Multiplexed) |
| BA0-1 | Select Bank |
| DQ0-63 | Data Input/Output |
| CB0-7 | Check bit (Data-in/data-out) |
| CLK0,CK1 | Clock input |
| CKE0 | Clock Enable input |
| CS0# | Chip select Input |
| RAS# | Row Address Strobe |
| CAS# | Column Address Strobe |
| WE# | Write Enable |
| DQMB0-7 | DQM |
| Vcc | Power Supply (3.3V) |
| Vss | Ground |
| SDA | Serial data I/O |
| SCL | Serial clock |
| DNU | Do not use |
| NC | No Connect |

## FUNCTIONAL BLOCK DIAGRAM




NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

| *CLOCK WIRING | |
|---|---|
| CLOCK INPUT | SDRAMS |
| *CLK0 | 4 OR 5 SDRAMS |
| *CLK1 | 4 OR 5 SDRAMS |

*Wire per Clock Loading Table/Wiring Diagrams

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$, $V_{CCQ}$ | -1.0 ~ 4.6 | V |
| Storage Temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power Dissipation | $P_D$ | 9 | W |
| Short Circuit Current | $I_{OS}$ | 50 | mA |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: $V_{SS}$ = 0V, 0°C ≤ $T_A$ ≤ +70°C

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{CCQ+0.3}$ | V | 1 |
| Input Low Voltage | $V_{IL}$ | -0.3 | — | 0.8 | V | 2 |
| Output High Voltage | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$= -2mA |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$= -2mA |
| Input Leakage Current | $I_{LI}$ | -10 | — | 10 | µA | 3 |

Note:
1. $V_{IH}$ (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. $V_{IL}$ (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ $V_{IN}$ ≤ $V_{CCQ}$
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

$T_A$ = 25°C, f = 1MHz, $V_{CC}$ = 3.3V, $V_{REF}$ = 1.4V ± 200mV

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Input Capacitance (A0-A12) | $C_{IN1}$ | 50 | pF |
| Input Capacitance (RAS#,CAS#,WE#) | $C_{IN2}$ | 50 | pF |
| Input Capacitance (CKE0) | $C_{IN3}$ | 50 | pF |
| Input Capacitance (CK0) | $C_{IN4}$ | 22 | pF |
| Input Capacitance (CS0#) | $C_{IN5}$ | 50 | pF |
| Input Capacitance (DQM0-DQM7) | $C_{IN6}$ | 8 | pF |
| Input Capacitance (BA0-BA1) | $C_{IN7}$ | 50 | pF |
| Data Input/Output Capacitance (DQ0-DQ63) | $C_{OUT}$ | 9.5 | pF |
| Data input/output capacitance (CB0-CB7) | $C_{OUT1}$ | 9.5 | pF |

## OPERATING CURRENT CHARACTERISTICS

$V_{CC}$ = 3.3V, 0°C ≤ $T_A$ ≤ +70°C

| | | | Version | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **100/133** | **Units** | **Note** |
| Operating Current (One bank active) | $I_{CC1}$ | Burst Length = 1<br>$t_{RC} \leq t_{RC}$(min)<br>$I_{OL}$ = 0mA | 900 | mA | 1 |
| Precharge Standby Current in Power Down Mode | $I_{CC2P}$ | CKE ≤ $V_{IL}$(max), $t_{CC}$ = 10ns | 18 | mA | |
| | $I_{CC2PS}$ | CKE & CK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | 18 | | |
| Precharge Standby Current in Non-Power Down Mode | $I_{CC2N}$ | CKE ≥ $V_{IH}$(min), CS ≥ $V_{IH}$(min), tcc =10ns<br>Input signals are charged one time during 20 | 180 | mA | |
| | $I_{CC2NS}$ | CKE ≥ $V_{IH}$(min), CK ≥$V_{IL}$(max), $t_{CC}$ = ∞<br>Input signals are stable | 90 | | |
| Active Standby Current in Power-Down Mode | $I_{CC3P}$ | CKE ≥ $V_{IL}$(max), $t_{CC}$ = 10ns | 54 | mA | |
| | $I_{CC3PS}$ | CKE & CK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | 54 | | |
| Active Standby Current in Non-Power Down Mode | $I_{CC3N}$ | CKE ≥ $V_{IH}$(min), CS ≥ $V_{IH}$(min), tcc = 10ns Input signals are changed one time during 20ns | 270 | mA | |
| | $I_{CC3NS}$ | CKE ≥ $V_{IH}$(min), CK ≤ $V_{IL}$(max), tcc = ∞<br>Input signals are stable | 225 | mA | |
| Operating Current (Burst mode) | $I_{CC4}$ | Io = mA<br>Page burst<br>4 Banks activated<br>$t_{CCD}$ = 2CK | 990 | mA | 1 |
| Refresh Current | $I_{CC5}$ | $t_{RC} \geq t_{RC}$(min) | 1980 | mA | 2 |
| Self Refresh Current | $I_{CC6}$ | CKE ≤ 0.2V | 27 | mA | |

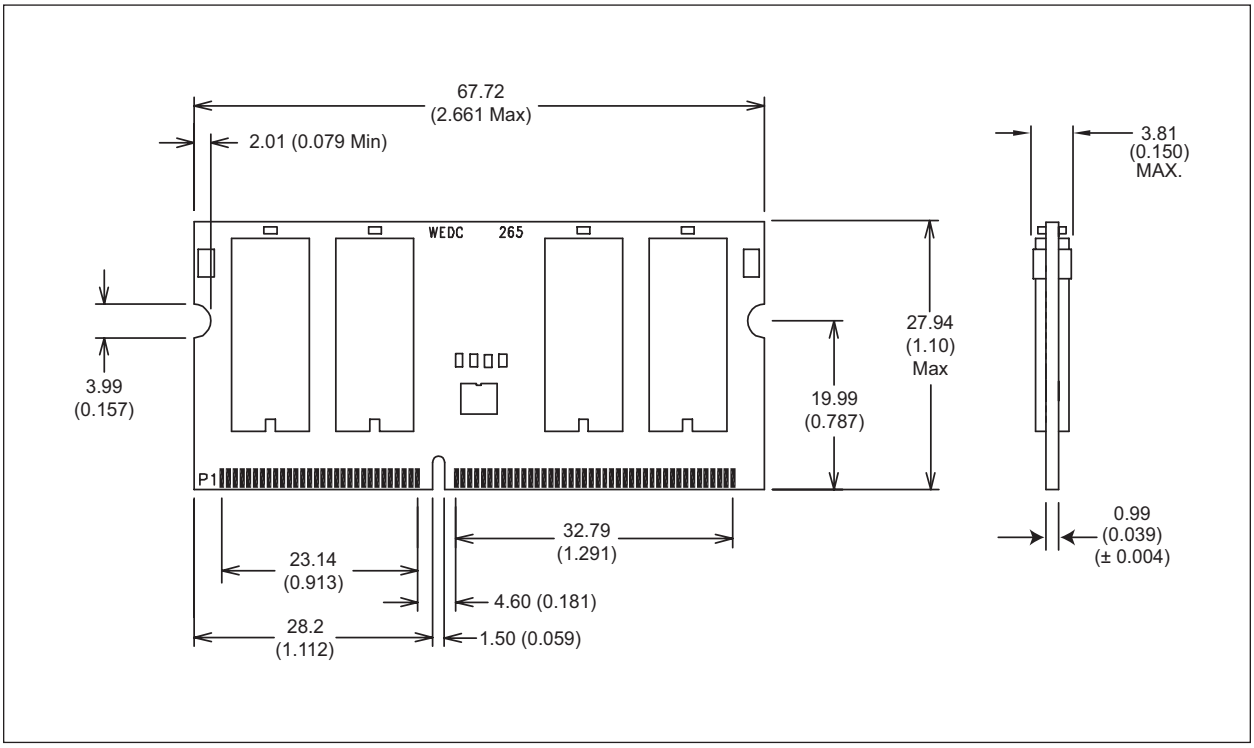
Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

## PACKAGE DIMENSIONS FOR AD1

| Ordering Information | Speed | CAS Latency | Height* |
|---|---|---|---|
| W3DG7232V10AD1 | 100MHz | CL=2 | 27.94 (1.1") MAX |
| W3DG7232V7AD1 | 133MHz | CL=2 | 27.94 (1.1") MAX |
| W3DG7232V75AD1 | 133MHz | CL=3 | 27.94 (1.1") MAX |

Note: For industrial temperature range product, add an "I" to the end of the part number.

## PACKAGE DIMENSIONS FOR AD1




*** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).**

## Document Title

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## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev A | A.1 Changed the module height to 1.095"<br>A.2 Changed part number to WED3DG7232V-AD1 | 6-2-03 | Advanced |
| Rev 0 | 0.1 Updated CAP and $I_{DD}$ Spec.<br>0.2 Created document title page<br>0.3 Moved from Advanced to Preliminary<br>0.4 Removed "ED" from part number | 6-04 | Preliminary |