**ILA8138A**

# 5.1V +12V REGULATOR WITH DISABLE AND RESET

The ILA8138A is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.
Output 2 can be disabled by TTL input.
Short circuit and thermal protections are included in all the versions.

- Output currents up to 1 A
- Fixed precision OUTPUT 1 voltages 5.1 V ± 2%
- Fixed precision OUTPUT 2 voltages 12 V ± 2%
- OUTPUT 1 with RESET facility
- OUTPUT 2 with DISABLE by TTL input
- Short circuit protection at both outputs
- Thermal protection
- Low drop output voltage

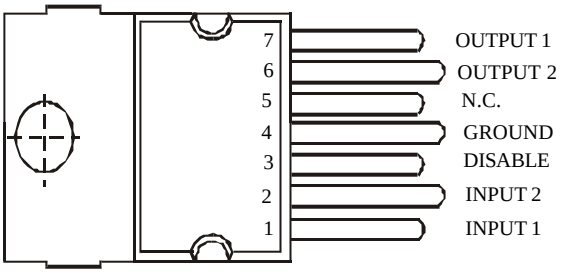
**TO-220AB/7**
**HEPTAWAT**
(Plastic Package)

**ORDERING INFORMATION**

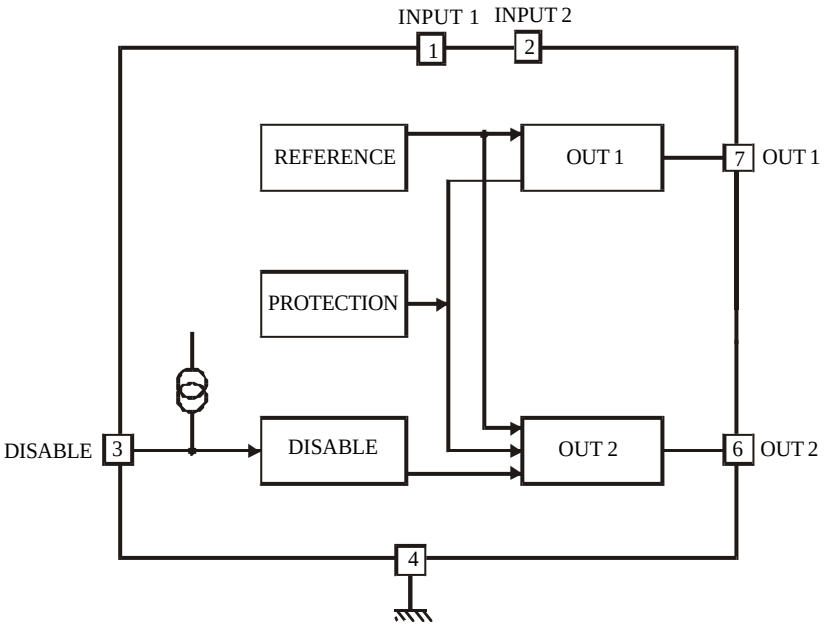
| | |
|---|---|
| **ILA8138A** | Plastic Package |
| **IZ8138A** | chip |

$T_J$ = -0° to 130°C

## PIN ASSIGNMENT




## BLOCK DIAGRAM



## MAXIMUM RATINGS*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN1}$ | DC Input Voltage Pin 1 | 0 | 20 | V |
| $V_{IN2}$ | DC Input Voltage Pin 2 | 0 | 20 | V |
| $V_{DIS}$ | Disable Input Voltage Pin 3 | 0 | 20 | V |
| $I_{O1,2}$ | Output Currents | 0 | 1.6 | A |
| Tstg | Storage Temperature | -65 | 150 | °C |
| $T_J$ | Junction Temperature | 0 | 150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN1}$ | DC Input Voltage Pin 1 | 7.0 | 16 | V |
| $V_{IN2}$ | DC Input Voltage Pin 2 | 14 | 18 | V |
| $V_{DIS}$ | Disable Input Voltage Pin 3 | 0 | 7.0 | V |
| $I_{O1,2}$ | Output Currents | 0 | 1.6 | A |
| $T_J$ | Junction Temperature | 0 | 130 | °C |

## THERMAL DATA

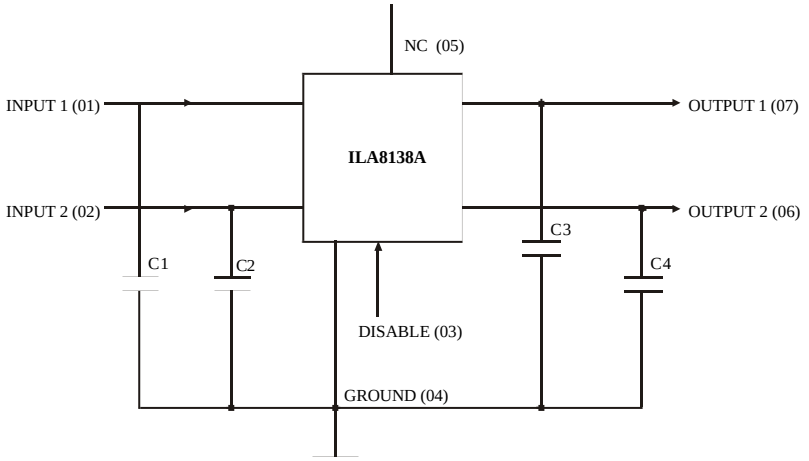
| Symbol | Parameter | Vlalue | Unit |
|---|---|---|---|
| Rth (j-c) | Maximum Thermal Resistance Junction-case | 6 | °C/W |
| Rth (j-a) | MaximumThermal Resistance Junction-ambient | 60 | °C/W |

**ELECTRICAL CHRACTERISTICS** ($V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, $T_J$ = 25°C, unless otherwise specified)

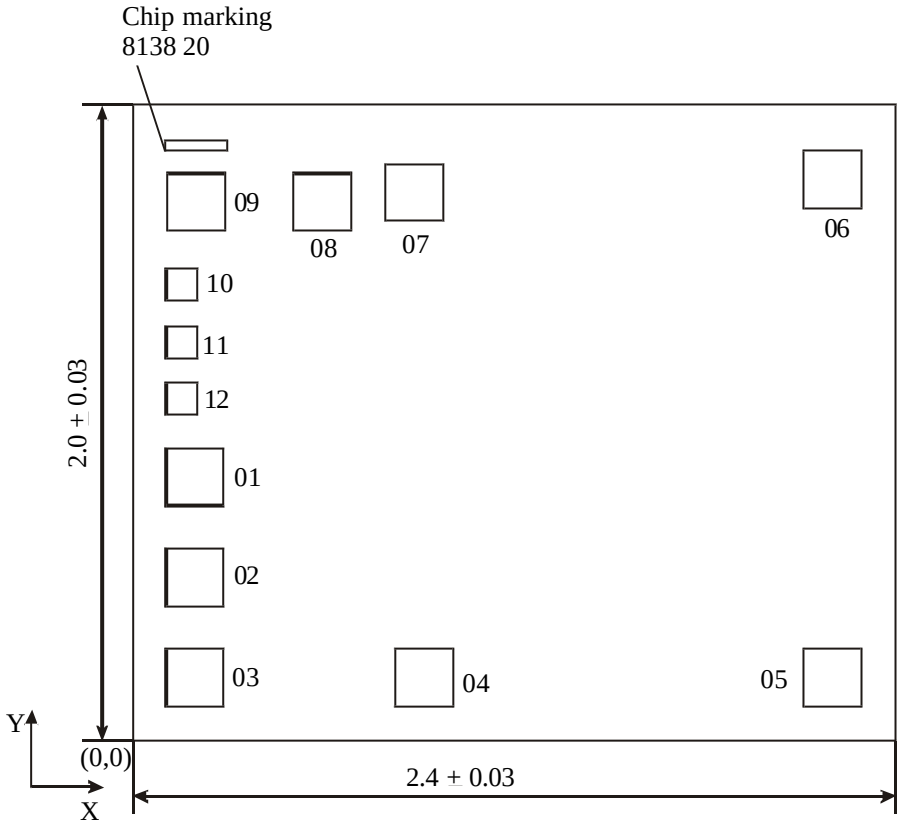
| Symbol | Parameter | Test Conditions | Guaranteed Limit | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{O1}$ | Output Voltage | $V_{IN1}$ = 7 V, $I_{O1}$= -10 mA | 5.0 | 5.2 | V |
| $V_{O2}$ | | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, $I_{O2}$= -10 mA | 11.76 | 12.24 | V |
| $V_{O1}$ | | -5 mA ≤ $I_{O2}$ ≤ -750 mA, 7 V ≤ $V_{IN1}$ ≤ 14 V | 4.9 | 5.3 | V |
| $V_{O2}$ | | -5 mA ≤ $I_{O2}$ ≤ -750 mA, 14 V ≤ $V_{IN2}$ ≤ 18 V, $V_{IN1}$ = 7 V | 11.5 | 12.5 | V |
| $\Delta V_{O1\ LI}$ | Line Regulation | 7 V ≤ $V_{IN2}$ ≤ 14 V, $I_{O1}$ = -200 mA | | 50 | mV |
| $\Delta V_{O2\ LI}$ | | 14 V ≤ $V_{IN2}$ ≤ 18 V, $I_{O1}$ = -200 mA, $V_{IN1}$ = 7 V | | 120 | |
| $\Delta V_{O1\ LO}$ | Load Regulation | $V_{IN1}$ = 7 V, -5 mA ≤ $I_{O1}$ ≤ -0.6 mA | | 100 | mV |
| $\Delta V_{O2\ LO}$ | | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, -5 mA ≤ $I_{O2}$ ≤ -0.6 mA | | 250 | |
| $V_{IO1}$ | Dropout Voltage | $V_{IN1}$ = 7 V, $I_{O1}$ = -750 mA | | 1.4 | V |
| | | $V_{IN1}$ = 7 V, $I_{O1}$ = -1.0 mA | | 2.0 | |
| $V_{IO2}$ | Dropout Voltage | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, $I_{O1}$ = -750 mA | | 1.4 | V |
| | | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, $I_{O1}$ = -1.0 mA | | 2.0 | |
| $I_Q$ | Quiescent Current | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V, $V_{DIS}$ = 0.8 V, $I_{O1}$= -10 mA | | 2.0 | mA |
| $I_{O1,2\ SC}$ | Short Circuit Output Current | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V | | 1.6 | A |
| | | $V_{IN1}$ = 16 V, $V_{IN2}$ = 16 V | | 1.0 | |
| $I_{DIS}$ | Disable Bias Current | 0 V ≤ $V_{DIS}$ ≤ 7 V, $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V | -100 | 2.0 | µA |
| $V_{DISH}$ | Disable Voltage High (out 2 active) | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V | 2 | | V |
| $V_{DISL}$ | Disable Voltage Low (out 2 disabled) | $V_{IN1}$ = 7 V, $V_{IN2}$ = 14 V | | 0.8 | V |

## TYPICAL APPLICATION

C1 to C4 = 10 µF



## CHIP PAD DIAGRAM




**Location of marking (mm):** left lower corner x=0.100, y=1.854.

**Chip thickness:** 0.35 ± 0.02 mm.

**PAD LOCATION**

| Pad No | Symbol | Location (left lower corner), mm | | Pad size, mm |
|---|---|---|---|---|
| | | X | Y | |
| 01 | GND | 0.105 | 0.740 | 0.18 x 0.18 |
| 02 | - | 0.105 | 0.425 | 0.18 x 0.18 |
| 03 | - | 0.105 | 0.110 | 0.18 x 0.18 |
| 04 | OUTPUT 2 | 0.825 | 0.110 | 0.18 x 0.18 |
| 05 | OUTPUT 1 | 2.110 | 0.110 | 0.18 x 0.18 |
| 06 | INPUT 1 | 2.110 | 1.675 | 0.18 x 0.18 |
| 07 | INPUT 2 | 0.795 | 1.635 | 0.18 x 0.18 |
| 08 | - | 0.505 | 1.605 | 0.18 x 0.18 |
| 09 | DISABLE | 0.110 | 1.605 | 0.18 x 0.18 |
| 10 | - | 0.105 | 1.385 | 0.10 x 0.10 |
| 11 | - | 0.105 | 1.205 | 0.10 x 0.10 |
| 12 | - | 0.105 | 1.025 | 0.10 x 0.10 |

Note: Pad location is given as per passivation layer