mosaic

Mosaic
Semiconductor
Inc.

1 Meg x 1 CMOS SRAM

MSM11000-020/025

Issue 1.0 : February 1993

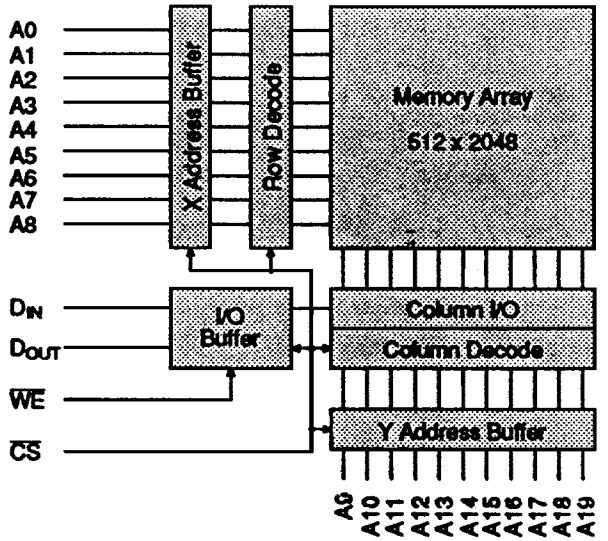
ADVANCE PRODUCT INFORMATION

1,048,576 x 1 CMOS High Speed Static RAM

Features

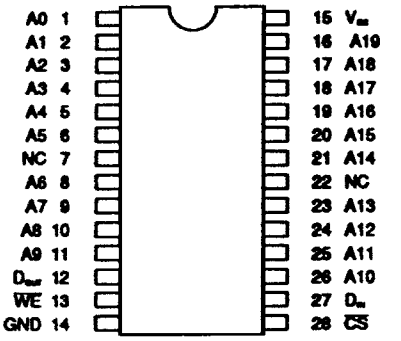
- Fast Access Times of 020/025 ns
- JEDEC Standard 28 Pin Footprint
- VIL™ High Density Package Available
- Low Power Operation 852.5mW (max)
- Low Power Standby 2.5mW (max) -L Version
- Completely Static Operation
- Separate Inputs and Outputs
- Equal Access and Cycle Times
- Battery Back-up Version Available
- Directly TTL Compatible
- May be processed to MIL-STD-883, non-compliant

Block Diagram

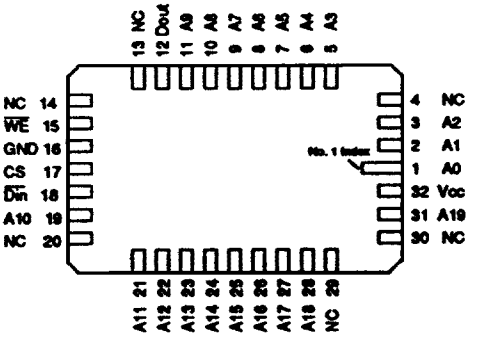


Pin Definition

Package Type: 'K','V'



Package Type: 'WX','JX'



Pin Functions

A0-A19	Address Inputs
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details Package details and dimensions on page 6,7, 8.

Pin Count	Description	Package Type	Material	Pin Out
28	0.4" Dual-in-Line (DIP)	K	Ceramic	JEDEC
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
28	Bottom Brazed Flatpack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	WX	Ceramic	ASIC
28	Leadless Small Outline Package	W	Ceramic	JEDEC
32	'J' Leaded Chip Carrier (JLCC)	JX	Ceramic	ASIC
28	Small Outline 'J' Bend (SOJ)	J	Ceramic	JEDEC

VIL is a trademark of Mosaic Semiconductor, Inc. Patent 316251.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5* to +7	V
Power Dissipation	P_T	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

Note: V_{IL} min. = -2.0V pulse of less than 10ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (11000I)
	T_{AM}	-55	-	125	°C (11000M, 11000MB)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-5	-	5	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=Gnd to V_{CC}	-5	-	5	µA
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	-	155	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, I/P's static	-	-	40	mA
	I_{SB1} (1)	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥Vcc-0.2V	-	-	10	mA
-L Version	I_{SB1} (1)	CMOS Levels	-	-	5	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Notes: (1) V_{IL} min = -0.3V
(2) Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	-	10	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

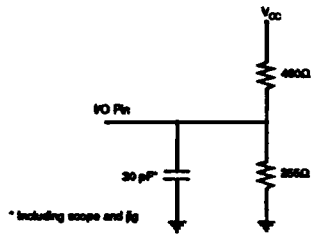
Note: This parameter is guaranteed, not tested.

AC Test Conditions

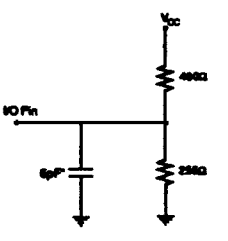
* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Load Circuit

Load A



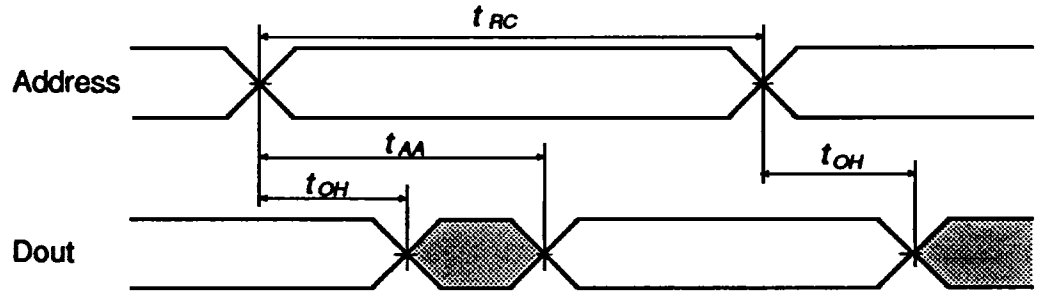
Load B



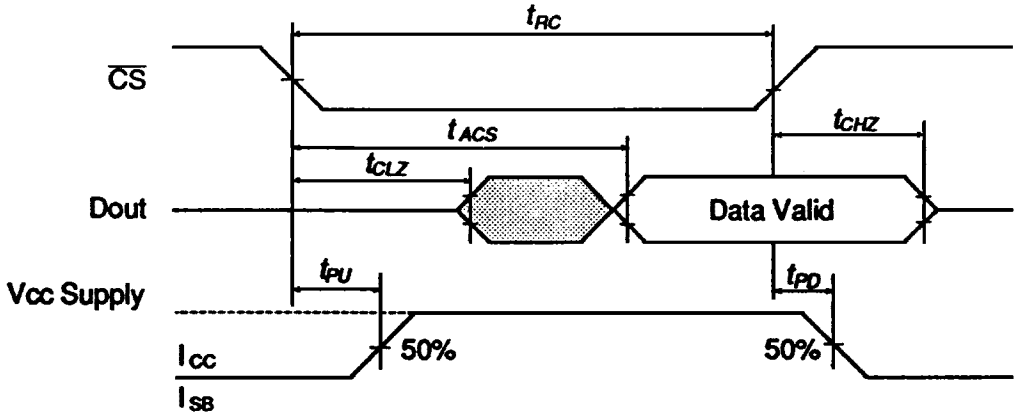
Read Cycle Timing

Parameter	Symbol	-020 min	-020 max	-025 min	-025 max	Unit	Note
Read Cycle Time	t_{RC}	20	-	25	-	ns	
Address Access Time	t_{AA}	-	20	-	25	ns	
Chip Select Access Time	t_{ACS}	-	20	-	25	ns	
Output Hold from Address Change	t_{OH}	3	-	3	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	1
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	ns	5
Chip Deselection to Power Down Time	t_{PD}	-	20	-	25	ns	5

Read Cycle No. 1 Timing Waveform (2,3)



Read Cycle No. 2 Timing Waveform (2,4)



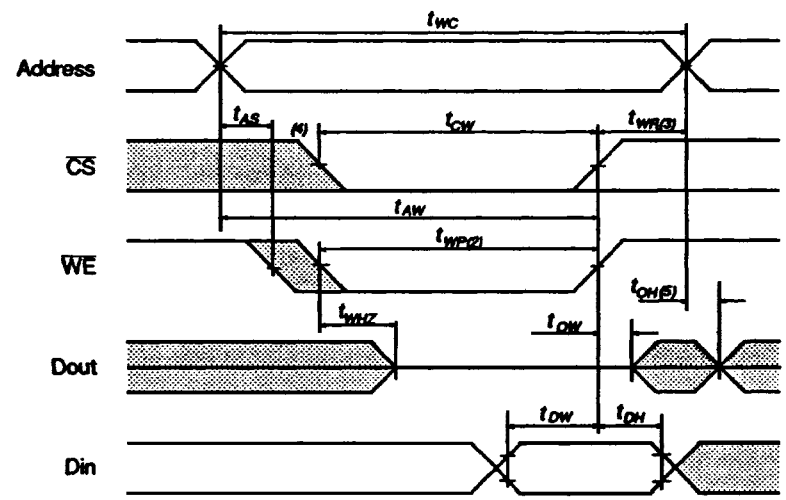
Notes: (1) Transition is measured ±200mV from steady voltage with Load B. This parameter is guaranteed and not 100% tested.
(2) $\overline{WE}$ is High for Read Cycle.
(3) Device is continuously selected, $\overline{CS}$=V_{IL}.
(4) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(5) This parameter is guaranteed, and not 100% tested.

Write Cycle Timing

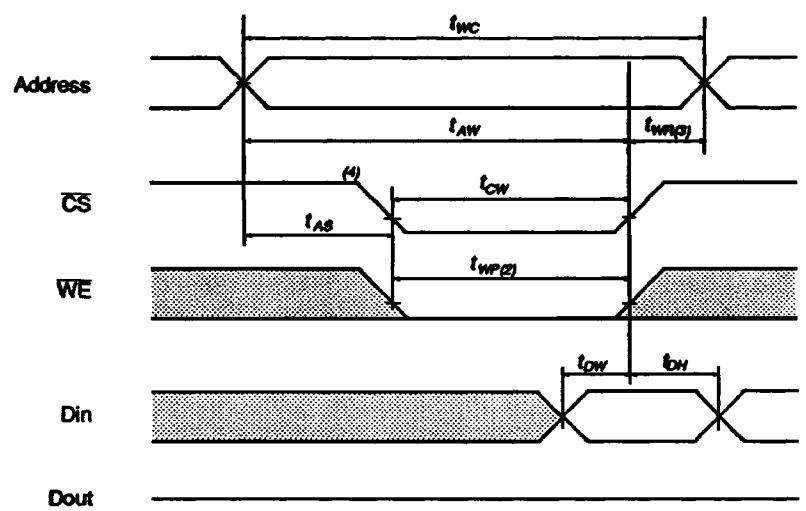
Parameter	Symbol	-020 min	-020 max	-025 min	-025 max	Unit	Note
Write Cycle Time	t_{WC}	20	-	25	-	ns	
Chip Selection to End of Write	t_{CW}	15	-	17	-	ns	
Address Valid to End of Write	t_{AW}	16	-	20	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	ns	
Write Pulse Width	t_{WP}	15	-	17	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	ns	
Write to Output in High Z	t_{WHZ}	0	12	0	15	ns	1
Data to Write Time Overlap	t_{DW}	12	-	15	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	0	-	0	-	ns	1

Notes: (1) Transition is measured ±200mV from steady state voltage with Load B. This parameter is guaranteed and not 100% tested.

Write Cycle No.1 Timing Waveform ($\overline{WE}$ Controlled)



Write Cycle No.2 Timing Waveform ($\overline{CS}$ Controlled)



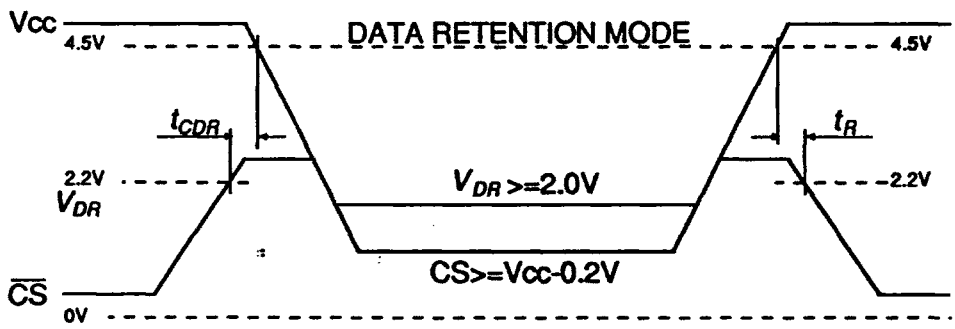
AC Characteristics Notes

Notes: (1) Transition is measure ±200mV from high impedance voltage with load B. This parameter is not 100% tested.
(2) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) Dout is in the same phase as written data of this write cycle.

Low V_{CC} Data Retention Characteristics - L Version Only (T_A= 0°C to 70°C)

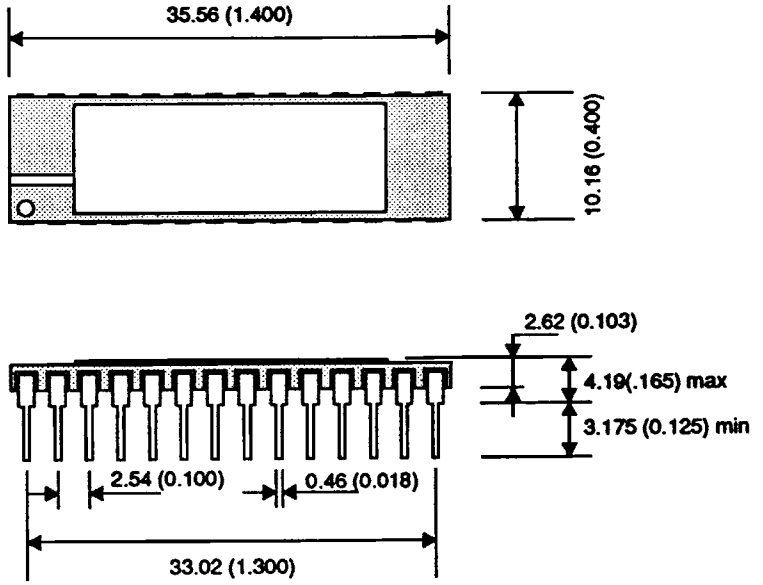
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2, $V_{IN} \geq V_{CC}$-0.2V 0V≤V_{IN}≤0.2V, $T_{OP}=T_A$	-	2	100	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Low V_{CC} Data Retention Timing Waveform

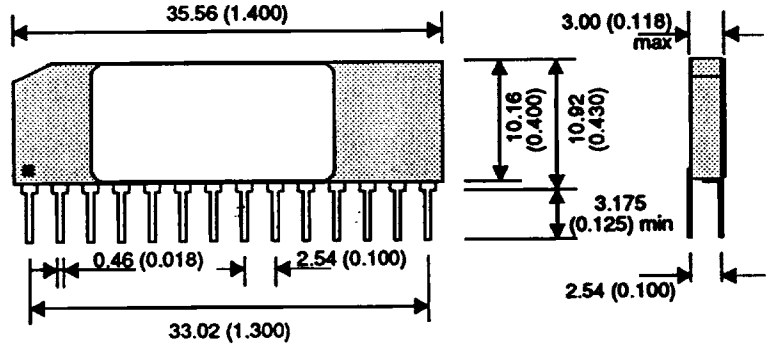


Package Details All dimensions in mm (inches). Tolerance on all dimensions ±0.254(0.010).

28 Pin 0.4" Dual-in-Line (DIP) - 'K' Package

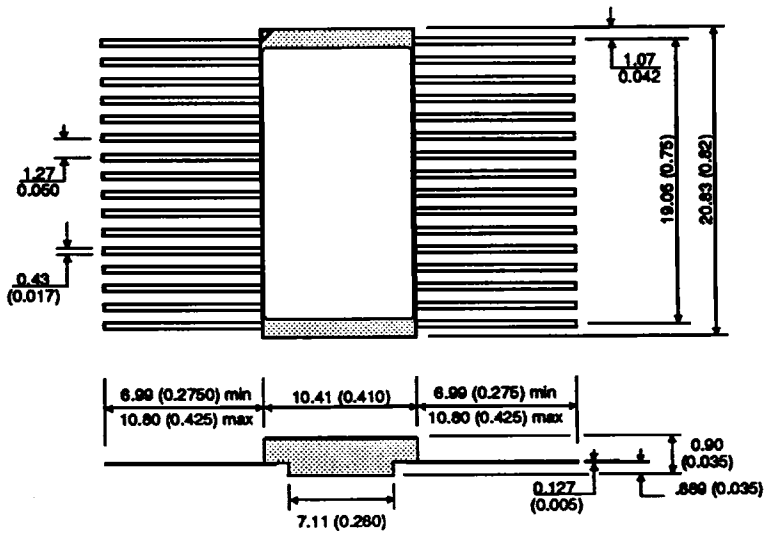


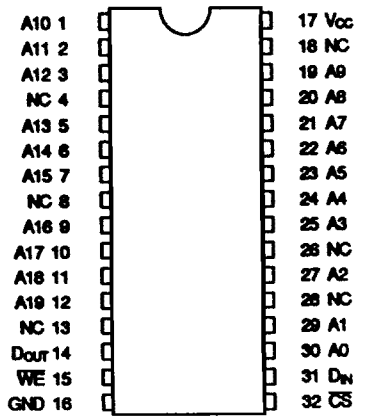
28 Pin 0.1" Vertical-In-Line (VIL™) - 'V' Package



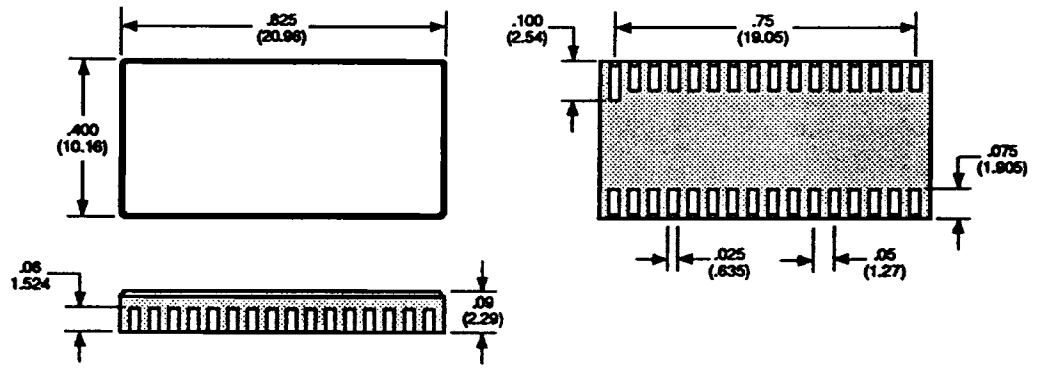
32 Pin Ceramic Flatpack - 'G' Package

Pinout for Package Type: 'G', 'W', 'J'

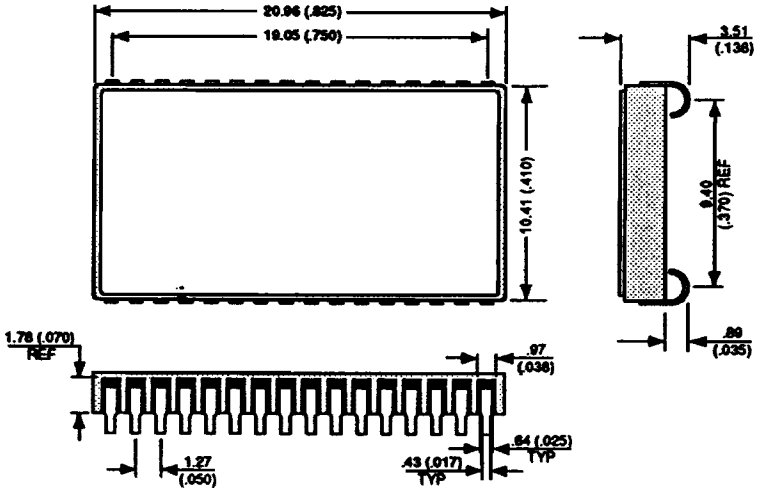




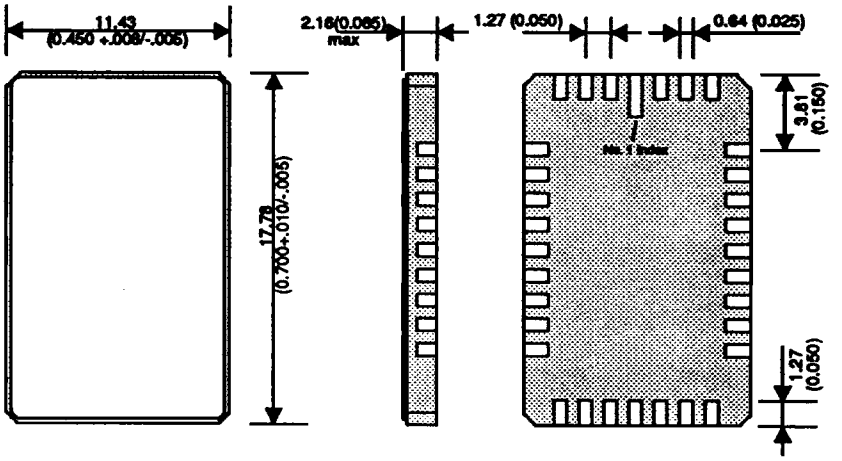
32 Pin Dual-in-Line Leadless Chip Carrier (LCC) - 'w' Package



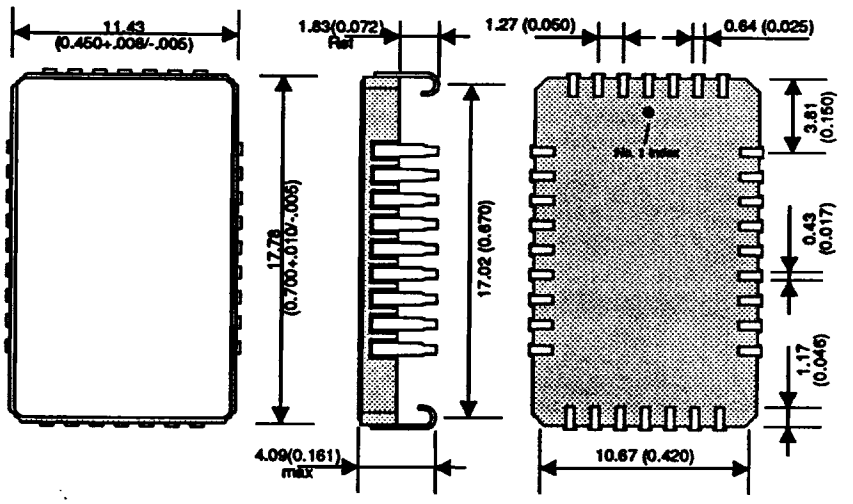
32 Pad Dual-in-Line 'J' Leaded Chip Carrier (JLCC) - 'J' Package



32 Pad Extended Leadless Chip Carrier (LCC) - 'WX' Package

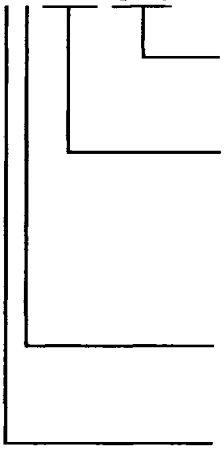


32 Pin Extended 'J'Leaded Chip Carrier (JLCC) - 'JX' Package



Ordering Information

MSM11000KLMB-020



Speed	020	= 20 ns
	025	= 25 ns
Temp. Range/Screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military.
	MB	= Processed to MIL-STD 883 Method 5004, non-compliant
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part **(025 ns only)**
Package	K	= 28 Pin 400 mil DIP
	V	= 28 Pin 100 mil VIL
	G	= 28 Pin Ceramic Flatpack
	WX	= 32 Pad Extended LCC
	W	= 32 Pad Leadless DIL
	JX	= 32 Pin Extended JLCC
	J	= 32 Pin JLCC DIL

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

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