Preliminary

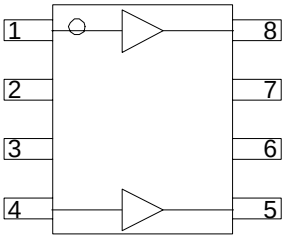
CGA-6618

Dual CATV Broadband High Linearity GaAs HBT Amplifier

Product Description

Stanford Microdevice's CGA-6618 is a high performance GaAs HBT MMIC Amplifier. Designed with the InGaP process technology for excellent reliability. A Darlington configuration is utilized for broadband performance. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. The amplifier contains two amplifiers for use in wideband Push-Pull CATV amplifiers requiring excellent second order performance. The second and third order non-linearities are greatly improved in the push pull configuration.

Amplifier Configuration



Product Features

- Excellent CSO/CTB/XMOD Performance at +34 dBmV Output Power per Tone
- Dual Devices in each SOIC-8 Package simplify Push-Pull configuration PC board layout
- Operates from a single supply
- Dropping Resistor provides Temperature Compensation

Applications

- CATV Head End Driver and Predriver Amplifier
- CATV Line Driver Amplifier

Key 75 Ohm Parameters at Room Temperature 50-860MHz CATV Band Data

	Test Conditions: V_s = 8.0 V R_{BIAS}=39 Ohms T_L = 25°C I_D = 160mA $Z_S = Z_L$ = 75 Ohms	Freq.	Units	Min.	Typ.	Max.
Gain		50 MHz 500 MHz 860 MHz	dB		14.0 14.1 14.0	
Output IP2	Tone spacing = 1 MHz Pout/Tone = +6 dBm	50 MHz 500 MHz 860 MHz	dBm		72 82 74	
Output IP3	Tone spacing = 1 MHz Pout/Tone = +6 dBm	50 MHz 500 MHz 860 MHz	dBm		38 40 40	
Output P1dB		50 MHz 500 MHz 860 MHz	dBm		21.5 21.5 21.0	
Input Return Loss		50 MHz 500 MHz 860 MHz	dB		12.5 17.0 13.5	
Output Return Loss		50 MHz 500 MHz 860 MHz	dB		10.0 19.0 13.5	
Noise Figure	Average of 3 devices Balun Insertion Loss Included	50 MHz 500 MHz 860 MHz	dB		3.9 4.1 4.4	
CSO	Worst Case Over Band 79 Ch., Flat, +34dBmV		dBc		81	
CTB	Worst Case Over Band 79 Ch., Flat, +34dBmV		dBc		70	
XMOD	Worst Case Over Band 79 Ch., Flat, +34dBmV		dBc		65	
Vd			V		4.7	

Note: Measured in Push-Pull Application test board

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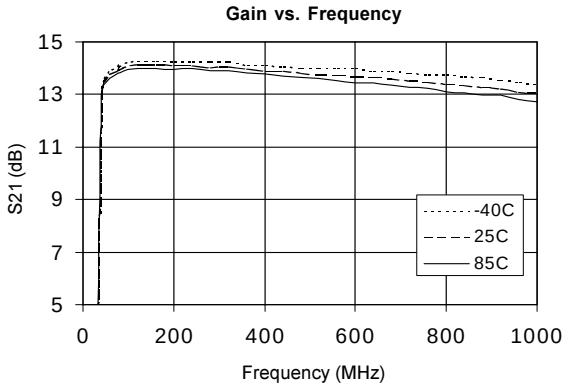
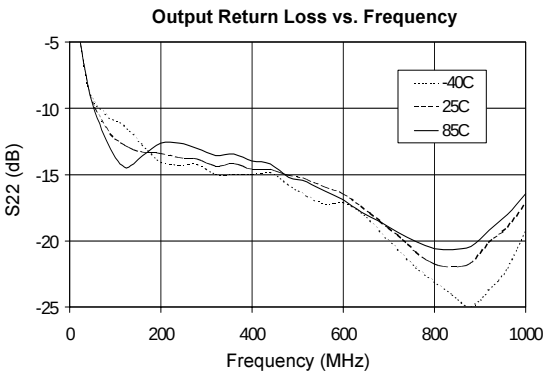
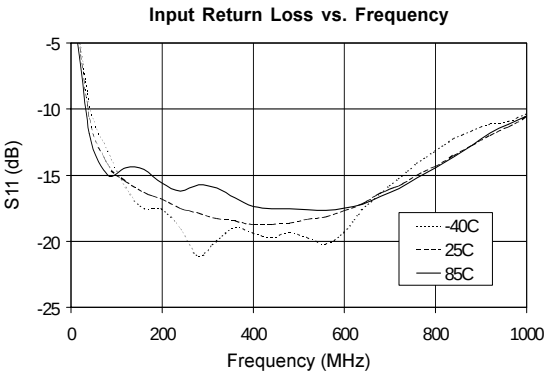
Typical S-Parameters @ V_S=8V, I_D=160mA, R_{BIAS}=39 Ohms, T_L=+25°C







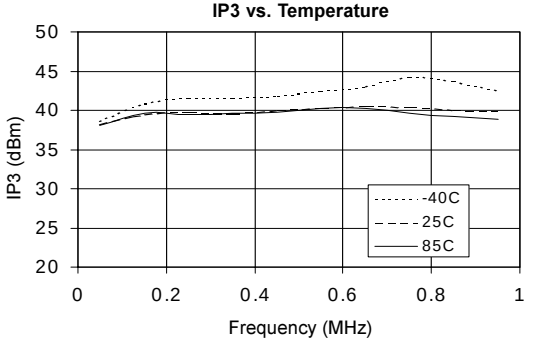
Absolute Maximum Ratings

Parameter	Absolute Limit
Max. Device Current (I_D)	240 mA
Max. RF Input Power	+16 dBm
Max. Junction Temp. (T_J)	+150ºC
Operating Temp. Range (T_L)	-40ºC to +85ºC
Max. Storage Temp.	+150ºC
Operation of this device beyond any of these limits may cause permanent damage.	

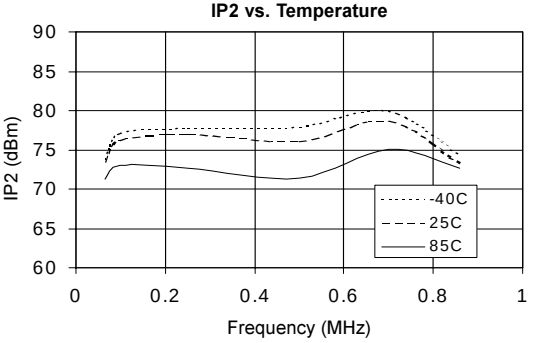
Bias Conditions should also satisfy the following expression: $I_D V_D$ (max) < (T_J - T_L)/R_{th},j-l

Typical RF Performance @ V_S=8V, I_D=160mA, R_{BIAS}=39 Ohms, T_L=+25°C

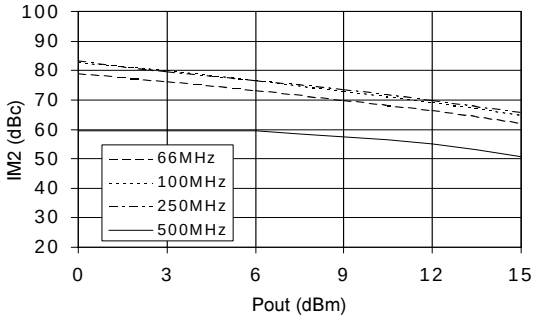
IP3 vs. Temperature



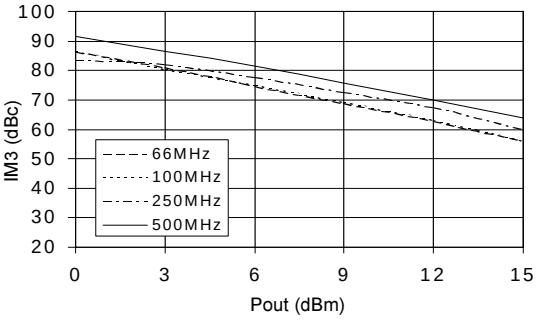
IP2 vs. Temperature



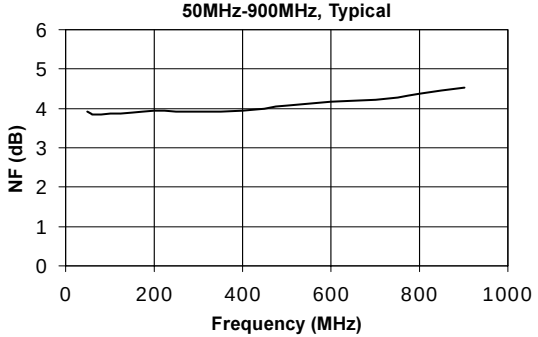
Second Harmonic vs. Pout and Freq.
Data shown is typical at 25C



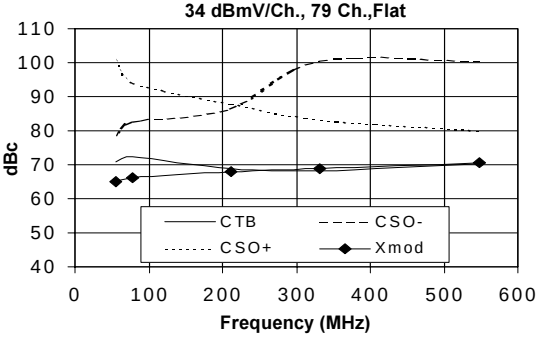
Third Harmonic vs. Pout and Freq.
Data shown is typical at 25C

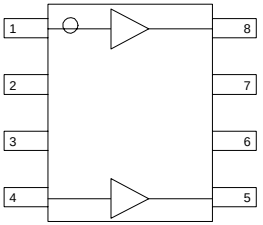


Push-Pull CGA-6618 Noise Figure
50MHz-900MHz, Typical

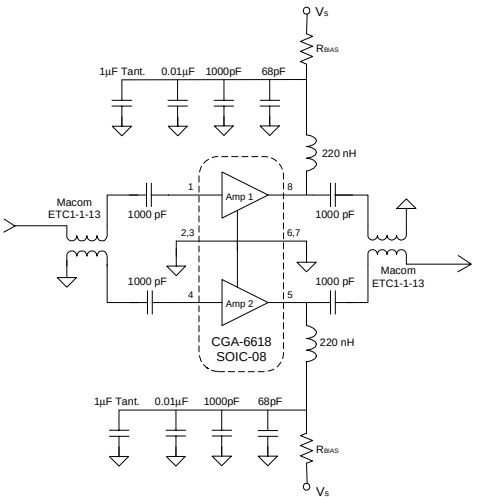


Push-Pull CGA-6618 CTB/CSO/XMOD
34 dBmV/Ch., 79 Ch.,Flat

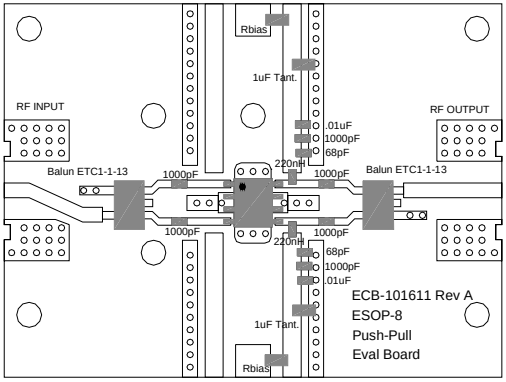


Pin #	Function	Description	Device Pin Out
1	RF IN Device 1	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the schematic.	
2,3	Ground	Connection to ground. Use via holes for best performance to reduce lead inductance as close to ground leads as possible.	
4	RF IN Device 2	Same as pin 1	
5	RF OUT / Vcc Device 2	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
6,7	Ground	Same as pins 2 and 3	
8	RF OUT / Vcc Device 1	Same as pin 5	
EPAD	Ground	Exposed area on the bottom side of the package must be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern below.	

Basic Application Schematic 50-860 MHz



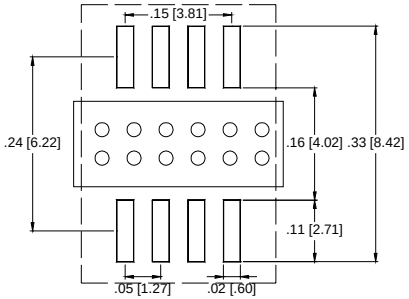
Evalution Board Layout 50-860 MHz



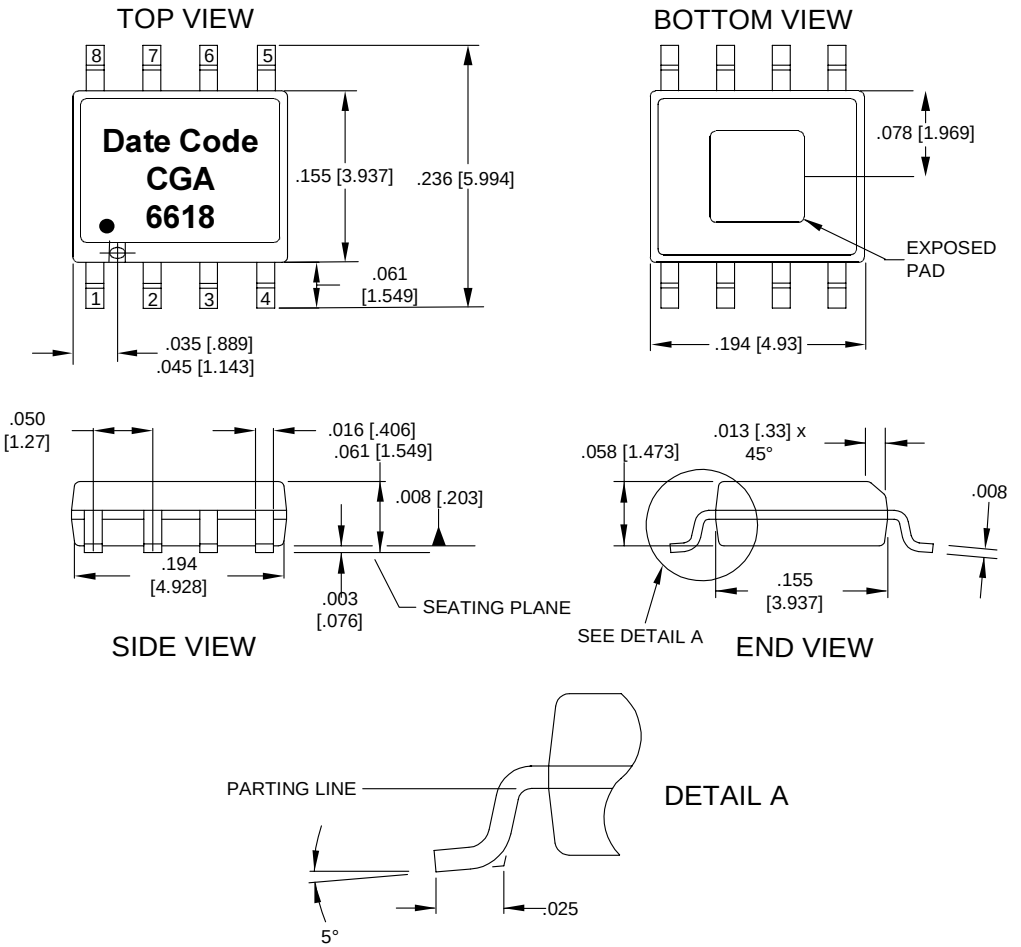
Recommended Bias Resistor Values for I_D=160mA				
Supply Voltage(V_S)	8V	9V	12V	15V
R_{BIAS}	39 Ω	56 Ω	91 Ω	130 Ω
R_{BIAS} Power Rating	1/2W	1/2W	1W	1W

$$R_{BIAS} = \frac{2(V_S - V_D)}{I_D}$$

Recommended Land Pattern



Package Outline Drawing



Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
CGA-6618	500	7"

Note: Parts need to be baked prior to use as discussed in application note EAN-101472 (Special handling information for Exposed Pad ™ SOIC-8 products) to ensure no moisture is trapped in the encapsulated package. In production, this baking procedure is not necessary if parts are used within 24 hours of opening the sealed shipping materials.