



**N-Channel Enhancement-Mode  
Vertical DMOS FET**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package
			TO-92
60V	5.0Ω	75mA	2N7000

**7**

**Features**

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

**Advanced DMOS Technology**

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Applications**

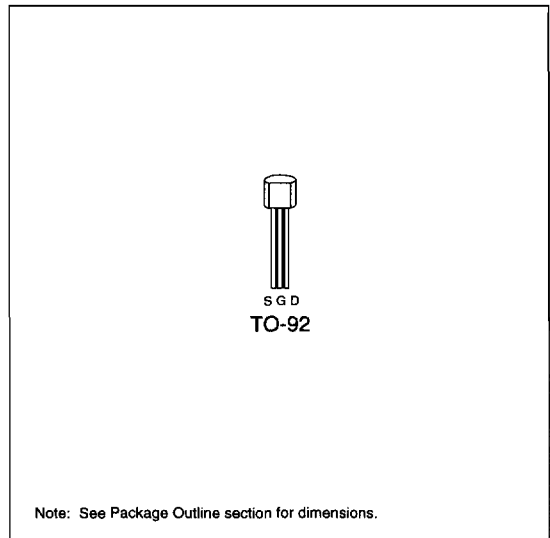
- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

**Package Options**



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jC}$ $^\circ\text{C/W}$	$\theta_{jA}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-92	200mA	500mA	1W	125	170	200mA	500mA

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

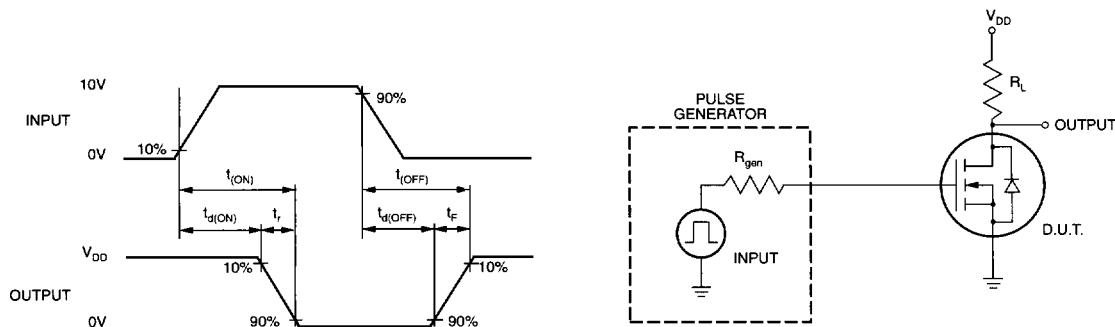
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	60			V	$I_D = 10\mu\text{A}$ , $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		3.0	V	$V_{GS} = V_{DS}$ , $I_D = 1\text{mA}$
$I_{GSS}$	Gate Body Leakage			10	nA	$V_{GS} = \pm 15\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current			1	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 48\text{V}$
				1	mA	$V_{GS} = 0\text{V}$ , $V_{DS} = 48\text{V}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	75			mA	$V_{GS} = 4.5\text{V}$ , $V_{DS} = 10\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.3	$\Omega$	$V_{GS} = 4.5\text{V}$ , $I_D = 75\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0	$\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 0.5\text{A}$
$G_{FS}$	Forward Transconductance	100			$\text{m}\Omega$	$V_{DS} = 10\text{V}$ , $I_D = 0.2\text{A}$
$C_{ISS}$	Input Capacitance			60	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			25		
$C_{RSS}$	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 15\text{V}$ , $I_D = 0.5\text{A}$ , $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
$V_{SD}$	Diode Forward Voltage Drop		0.85		V	$I_{SD} = 0.2\text{A}$ , $V_{GS} = 0\text{V}$

### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

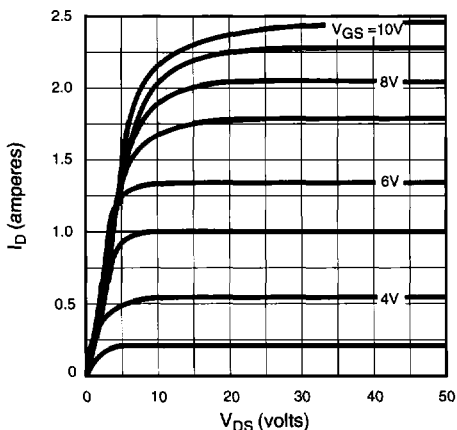
## Switching Waveforms and Test Circuit



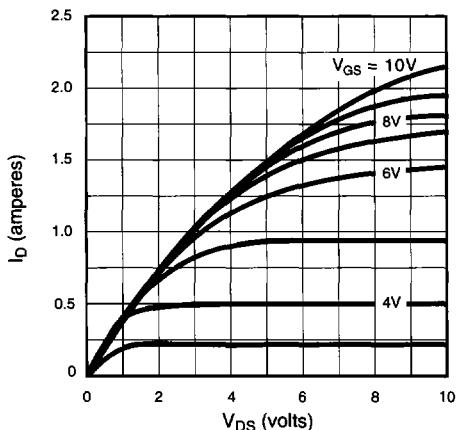
# Typical Performance Curves

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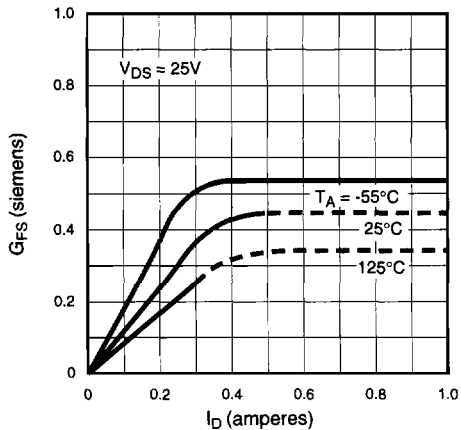
Output Characteristics



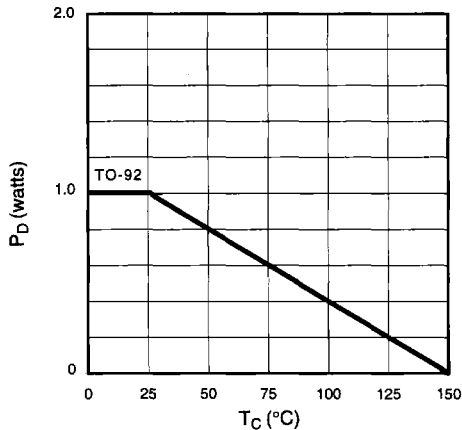
Saturation Characteristics



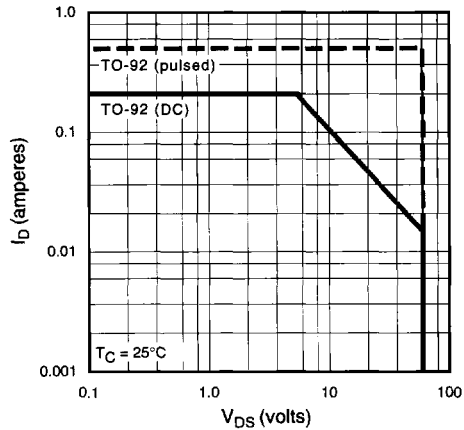
Transconductance vs. Drain Current



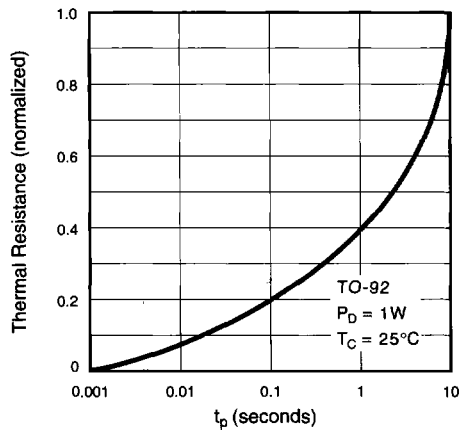
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

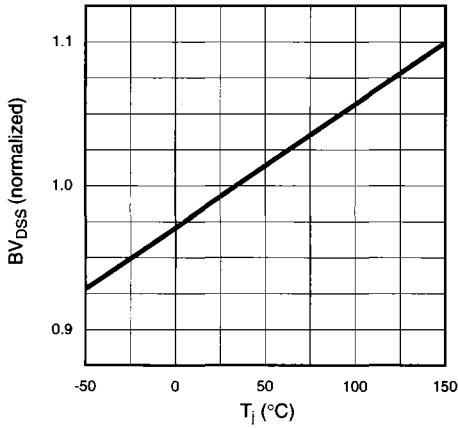


Thermal Response Characteristics

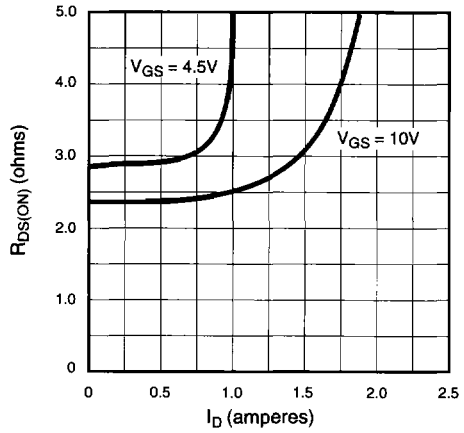


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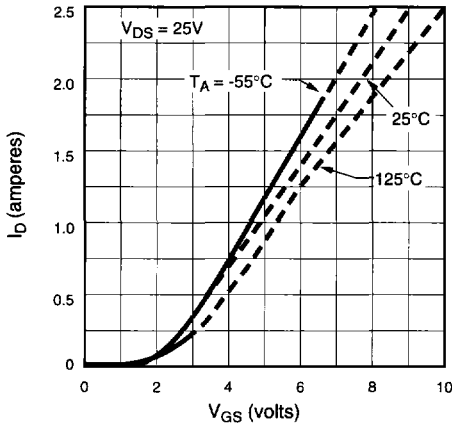
BV<sub>DSS</sub> Variation with Temperature



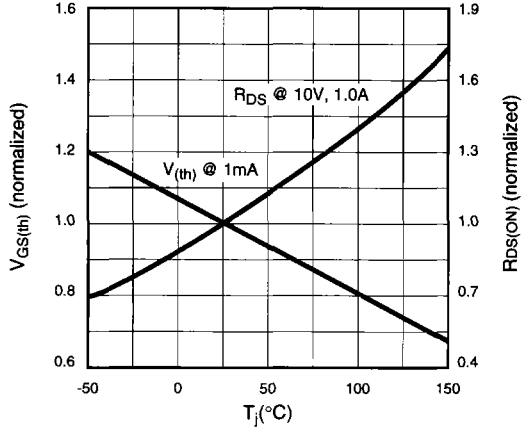
On-Resistance vs. Drain Current



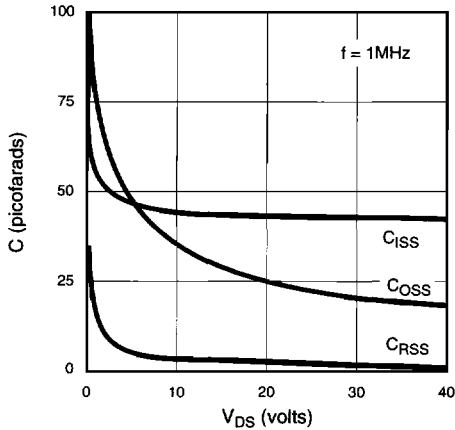
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

