SP9588

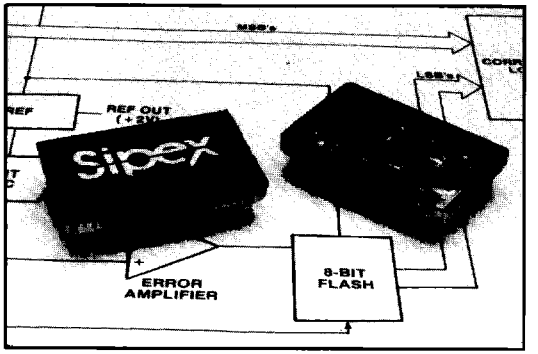
500 kHz, MULTIPASS™ 14-BIT A/D CONVERTER

DESCRIPTION

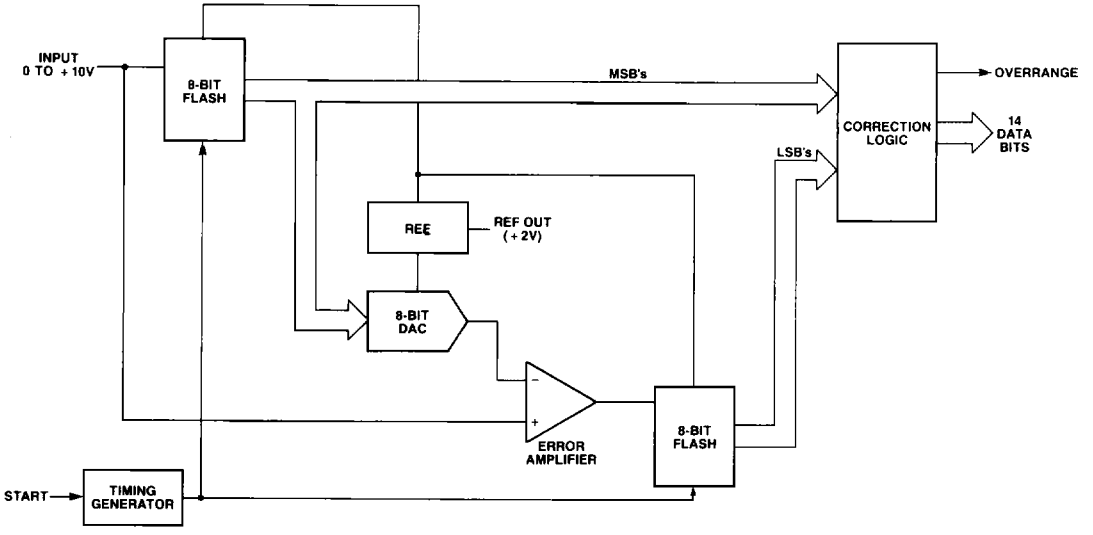
The SP9588 is a 14-bit, 2.0 microsecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology. The subranging Multipass process is optimized for high accuracy operation by using two 8-bit Flashes in a feed-forward error correction scheme to yield a final resolution of 14 bits while consuming less than 3 watts.

The SP9588 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on its rising edge and completes the conversion on its falling edge. Total conversion can be completed in less than 2.0 microseconds. By repeating the START command every 2.0 microseconds, the SP9588 will operate in a continuous mode at a maximum of 500 kHz.

The SP9588 input range, 0 to +10V, has been optimized for high accuracy applications such as high speed, high accuracy data acquisition systems. The SP9588 is ideal in all applications that require 14-bit performance at relatively high speed with moderately low power consumption.



FUNCTIONAL DIAGRAM



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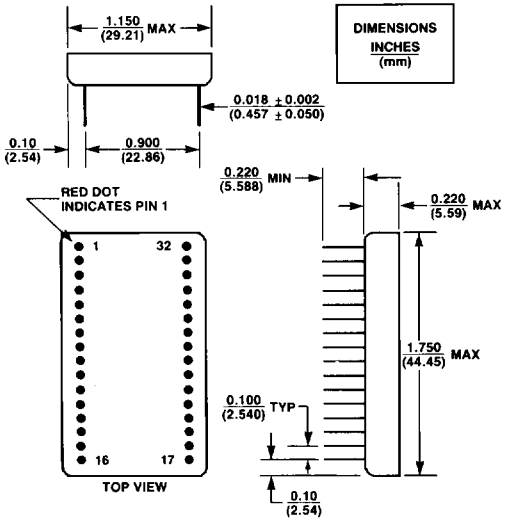
SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9588
RESOLUTION	14-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +10V
Input Impedance	5kΩ
DIGITAL INPUTS	
Logic Levels: Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity @25°C	±1 LSB max
Differential Linearity @25°C	±½ LSB
No Missing Codes 0 to 70°C	Guaranteed
Offset Error	0.1% of FSR typ, 0.3% max
Gain Error	0.1% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	2.0μ sec
STABILITY	
Integral Linearity Tempco	2.5 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	1 ppm/°C
Gain Error Drift	25 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	3 TTL Loads
REFERENCE	
Voltage	+2.0V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	25mA
−15V (±10%)	25mA
+5V Digital (±10%)	300mA
+5V Analog (±1%)	30mA
−5V (±1%)	30mA
Dissipation	2.5W typ, 3.0W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START (CLOCK)	32	8/14 SELECT
2	BIT 14 (LSB)	31	+5V DIGITAL
3	BIT 13	30	DIGITAL GND*
4	BIT 12	29	+5V ANALOG
5	BIT 11	28	−5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	−15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	ANALOG GND
13	BIT 3	20	TEST POINT
14	BIT 2	19	ANALOG GND
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

*Internally connected to case.

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9588 is designed primarily for high accuracy applications that require a conversion time as low as 2.0 microseconds. The SP 9588 will also operate at slower conversion times with no degradation. The rate of conversion is set by the START signal that is applied to it. The rising edge of the START signal initiates the conversion process and the falling edge of the START signal completes the process.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 5K ohm input impedance at 14-bit accuracy. This requires a careful selection of appropriate S/H amplifiers and fast operational amplifiers.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is directed to the input of the first 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 2.0 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is generated for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 14-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" signal to be converted by the Flash.

The "second pass" occurs when the ERROR AMPLIFIER output is directed to the input of the second FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is now ready for further processing by the CORRECTION LOGIC.

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 14-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which only requires a START signal as previously described. The falling edge of the START signal indicates that the digital data is ready.

SINGLE CONVERSION MODE

The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required.

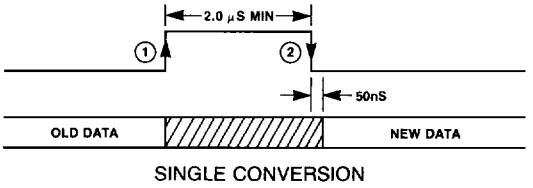
Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion is no longer valid.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

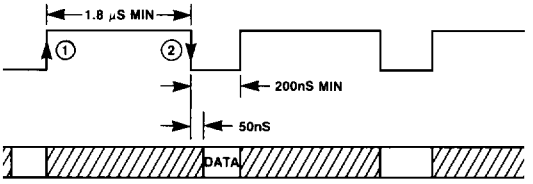
CONTINUOUS CONVERSION MODE

The SP 9588 will be in the continuous conversion mode as long as the START signal is repeated. This mode is used to follow high speed input signals and is capable of a 500 kHz converting rate. However, an external S/H amplifier is required...the time necessary for the S/H amplifier to acquire and settle must be taken into consideration. If the S/H amplifier requires 500 nanoseconds then the throughput rate is 400 kHz.

Referring to the timing diagram, the process is as follows:



SINGLE CONVERSION



CONTINUOUS CONVERSION

SP 9588 Timing Diagram

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion is no longer valid.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

The process is repeated continuously as shown in the timing diagram. When operating at the maximum rate of 500 kHz, the START signal should be high for only 1.8 microseconds and low for 0.2 microseconds. When using an external S/H amplifier, the START signal should be high for the full 2.0 microseconds and low for the time required for the S/H amplfier to acquire and settle. The resulting conversion rate will be proportional to the total time required for both the S/H amplifier and the SP 9588.

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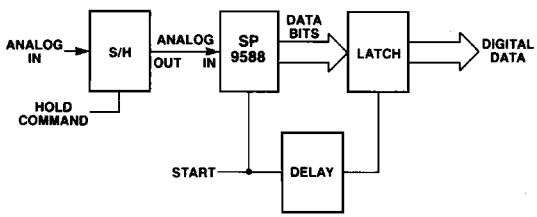
INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00061		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
4.99939		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 F F F
5.00000		1	0	0	0	0	0	0	0	0	0	0	0	0	0	2 0 0 0
5.00061		1	0	0	0	0	0	0	0	0	0	0	0	0	1	2 0 0 1
9.99939		1	1	1	1	1	1	1	1	1	1	1	1	1	1	3 F F F
10.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4 0 0 0
10.00061	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4 0 0 1
10.11658	1	0	0	0	0	0	0	1	0	1	1	1	1	1	1	4 0 B F
1.17%	Overrange															

SP 9588 Coding Table @10 Volt Full Scale

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9588 with an external S/H amplifier and an external latch for the data bits. Since the data is valid 50 nanoseconds after the falling edge of the START signal, the START signal needs to be delayed by more than 50 nanoseconds if it is to be used as the strobe for the latch.

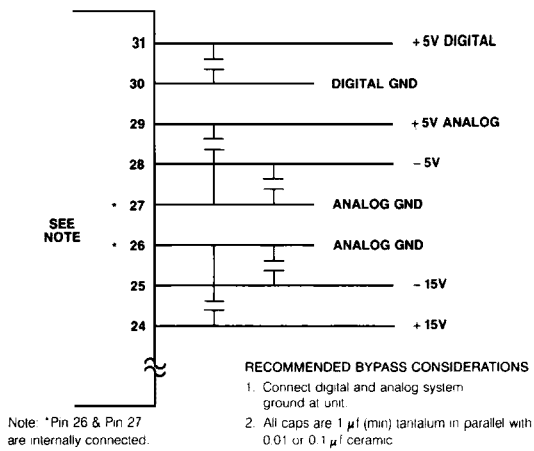
The SP 9588 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 300 Hz.



Typical Application: SP 9588 With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

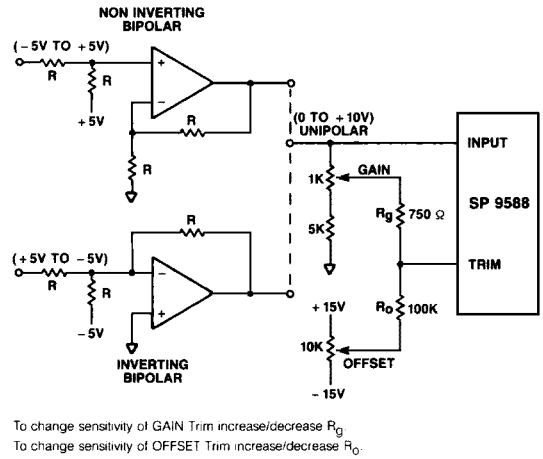
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9588. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9588. Also, the analog and digital +5V supplies should be separate for optimum performance.



SP 9588 Power Supply Connections

TRIM ADJUSTMENTS

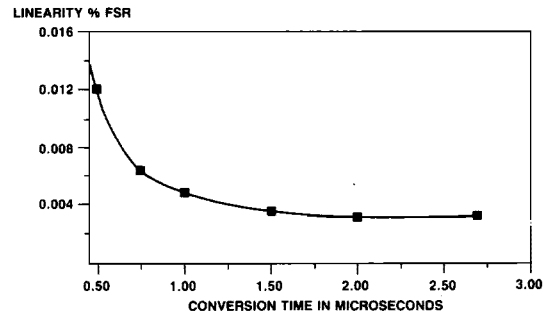
The SP 9588 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (750 ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_o (100k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.



SP 9588 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9588 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.



SP 9588 Linearity Vs. Conversion Time

SUMMARY

The SP 9588 has been designed to simplify high speed, high accuracy conversion and operate at reasonable power levels. The subranging technique and correction logic have been optimized to provide the high accuracy. With this in mind, the SP 9588 is then the solution to most high speed, high accuracy data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9588C	0 to +70°C	—
SP 9588B	-55°C to +125°C	MIL-STD-883C