



3584

High Voltage, High Speed OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY VOLTAGE:
 $\pm 70V$ to $\pm 150V$
- GAIN-BANDWIDTH PRODUCT: 50MHz
- SLEW RATE: 150V/ μ s
- FET INPUT: $I_B = 20pA$ max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

APPLICATIONS

- PROGRAMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- ELECTROSTATIC TRANSDUCER DRIVER
- CRT DEFLECTION

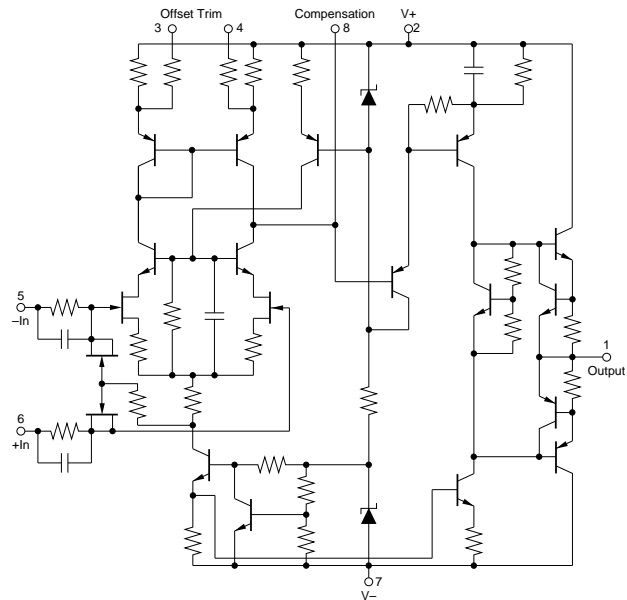
DESCRIPTION

The 3584 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3584 operates over a wide power supply range ($\pm 70V$ to $\pm 150V$) and provides outputs up to 15mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

The 3584 provides a gain-bandwidth product of 20MHz min (50MHz typical). External frequency compensation (series R/C) allows the user to optimize the bandwidth and slew rate for a particular application.

Specified temperature range is 0°C to +70°C. The 3584's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.



SPECIFICATIONS

ELECTRICAL

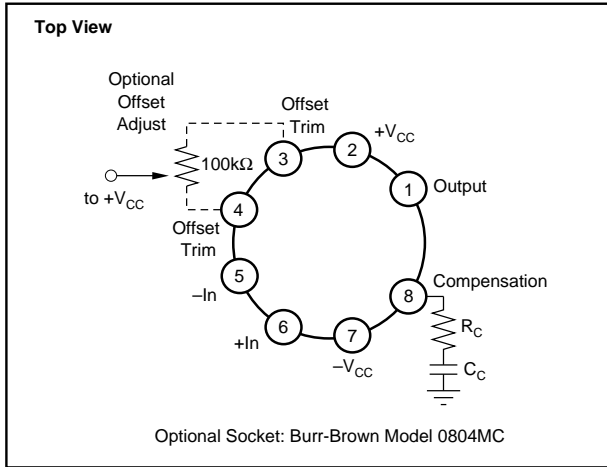
T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

PARAMETER	CONDITIONS	3584JM			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply vs Time	Specified Temperature Range		20 50	±3 ±25	mV μV/°C μV/V μV/month
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature vs Power Supply Input Offset Current vs Temperature vs Power Supply	V _{CM} = 0V V _{CM} = 0V		Doubles Every 10°C 0.2 Doubles Every 10°C 0.2	-20 ±20	pA pA/V pA pA/V
NOISE Voltage, 0.01Hz to 10Hz 10Hz to 1kHz Current, 0.01Hz to 10Hz			5 1.7 0.3		μVp-p μVrms pAp-p
INPUT VOLTAGE RANGE Maximum Safe Differential Input Maximum Safe Common-Mode Input Common-Mode Input Range Common-Mode Rejection	Linear Operation		(V+) + V- V- to V+ V _S - 10 110		V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹¹ 10 10 ¹¹		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain Open-Loop Voltage Gain	No Load, DC Rated Load, DC	100	120		dB dB
FREQUENCY RESPONSE Unity-Gain Bandwidth Gain-Bandwidth Product Full-Power Bandwidth Slew Rate Settling Time: 0.1%	Small-Signal f = 1kHz, G = 100 G = 100 G = 100 G = 100	20	7 135 150 12		MHz MHz kHz V/μs μs
OUTPUT Voltage Output Current Output Short Circuit Current Load Capacitance (Maximum)		V _S - 5 ±15	±25 10		V mA mA nF
POWER SUPPLY Operating Voltage Range Quiescent Current	I _O = 0	±70		±150 ±6.5	V mA
TEMPERATURE RANGE Specification Operating Storage		0 -55 -55		+70 +125 +150	°C °C °C

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/μs. Inputs can be protected from signals exceeding 1000V/μs by limiting input current to 150mA with external series resistors (pins 5 and 6).

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CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
3584JM	8-Pin TO-3	0°C to +70°C

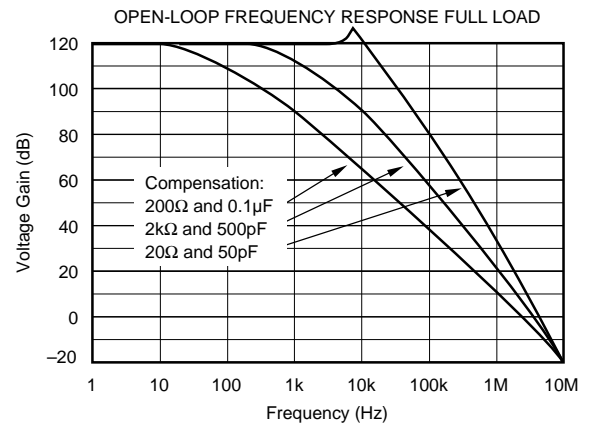
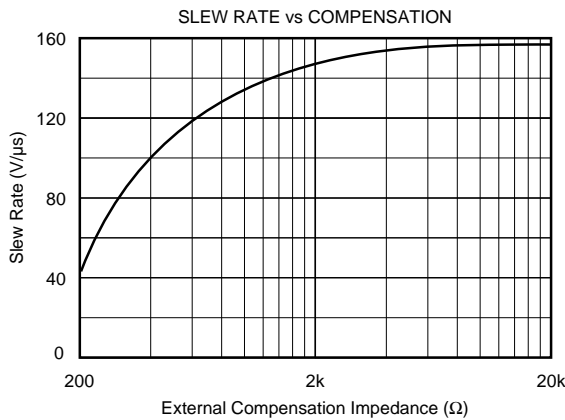
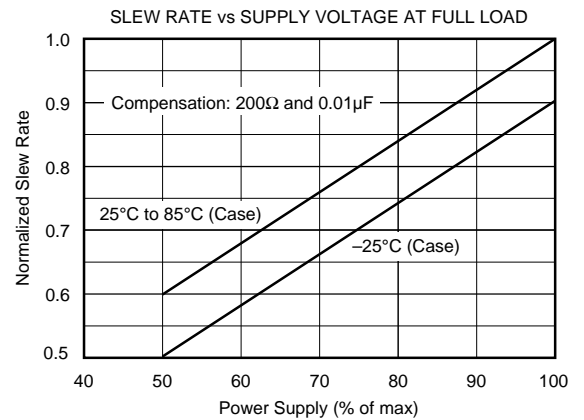
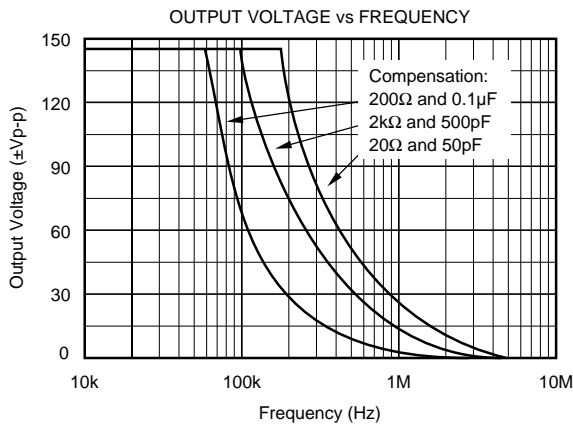
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
3584JM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

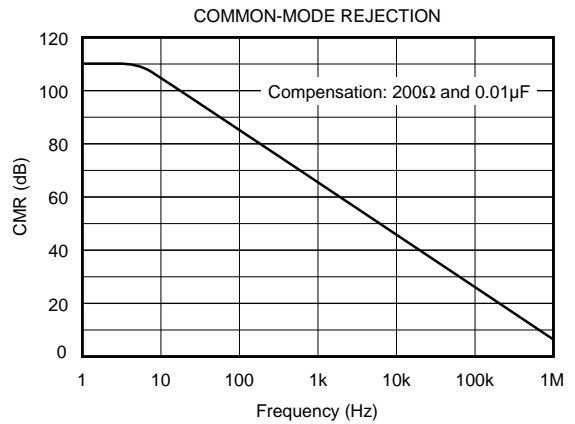
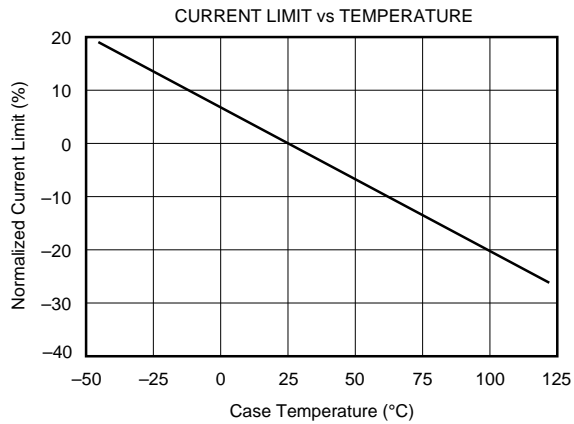
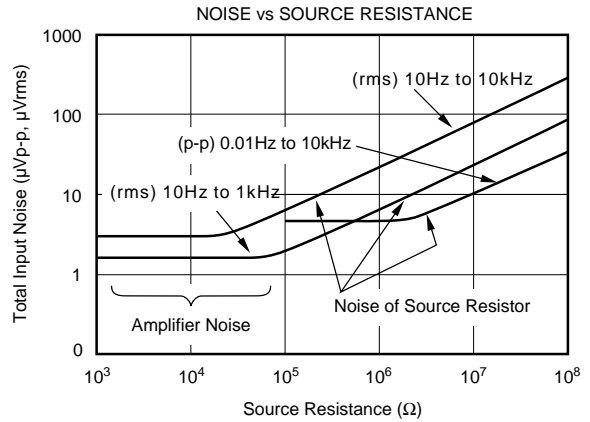
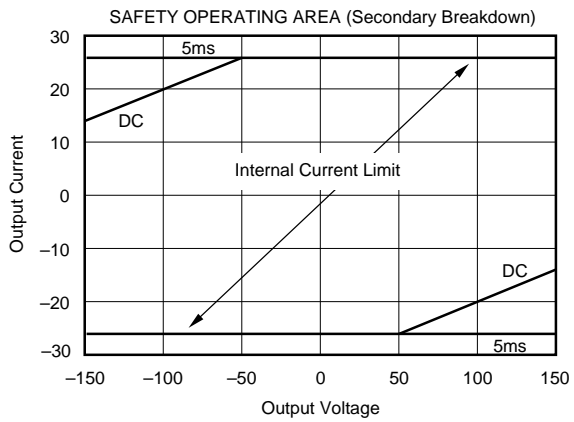
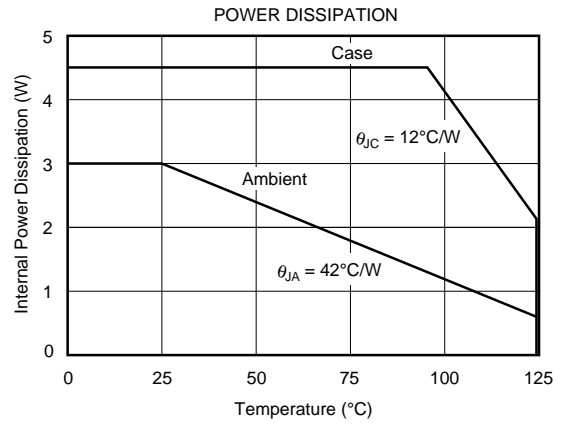
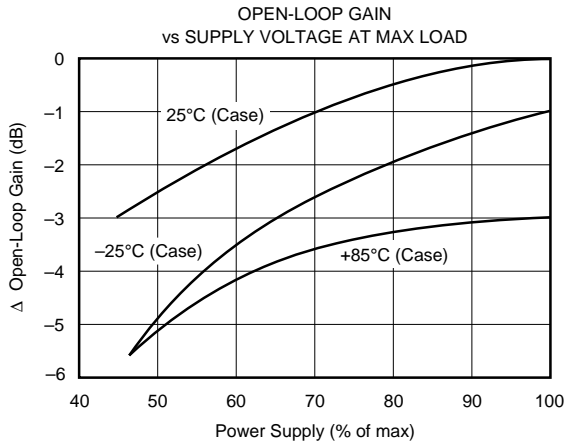
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, V_S = \pm 150V, unless otherwise noted.



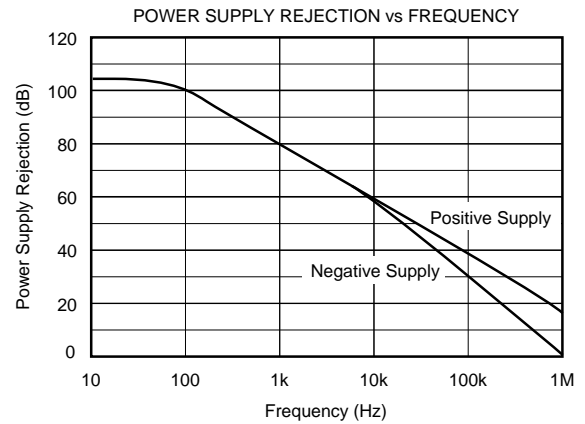
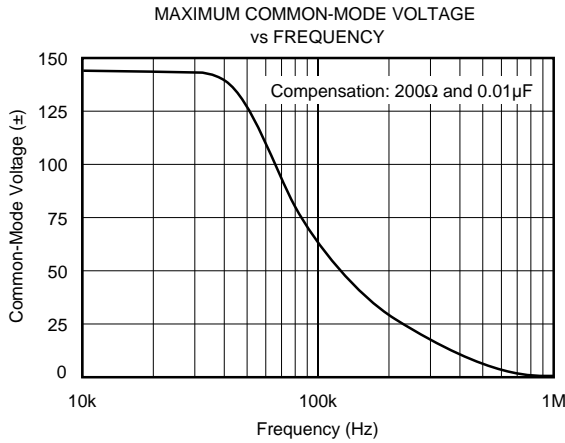
TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 150V$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required to operate the 3584. Bypass capacitors should be connected close to the device pins. Be sure that these capacitors have an adequate voltage rating.

Frequency compensation components must be connected to pin 8 for closed-loop gains of 100 or less. Recommended values are shown in Figure 1. Some adjustment in these values may be required depending on exact circuit configuration and load conditions. Be sure the compensation capacitor has a voltage rating equal to or greater than the positive power supply voltage, V₊. Standard 0.25W resistors can be used for R_C.

Input offset voltage and drift of the 3584 are laser-trimmed. Many applications require no external offset trimming. Figure 1 shows connection of an optional offset trim potentiometer which connects to pins 3 and 4.

FET input circuitry reduces the input bias current of the 3584 to less than 20pA at room temperature. Input bias current remains nearly constant throughout the full common-mode range. Input bias current approximately doubles for each 10°C increase in case temperature above 25°C. Heat sinking can help minimize this effect by reducing the case temperature.

Input circuitry of the 3584 is protected with series limiting resistors and input clamp diodes. The inputs can withstand the full rated supply voltage of ±150V (common-mode or differential).

THERMAL PROTECTION

The 3584 has internal thermal shut-down circuitry that activates at a case temperature of approximately 150°C or higher. As this circuitry is activated, the output current drive is reduced. As the case temperature returns to less than the activation temperature, operation will return to normal.

The thermal shut-down circuit will normally protect the amplifier during a short-circuit to ground. It will not protect against short-circuit to one of the power supplies. The typical performance curve “Safe Operating Area” shows that the large stress occurring during this high voltage condition may cause damage if it exceeds 5ms duration. The thermal protection circuitry will not activate fast enough to protect the device from short-circuits to one of the power supplies.

The package case of the 3584 is electrically isolated from all circuitry. No special insulating hardware is required. Although not absolutely required, it is recommended that the case be connected to ground.

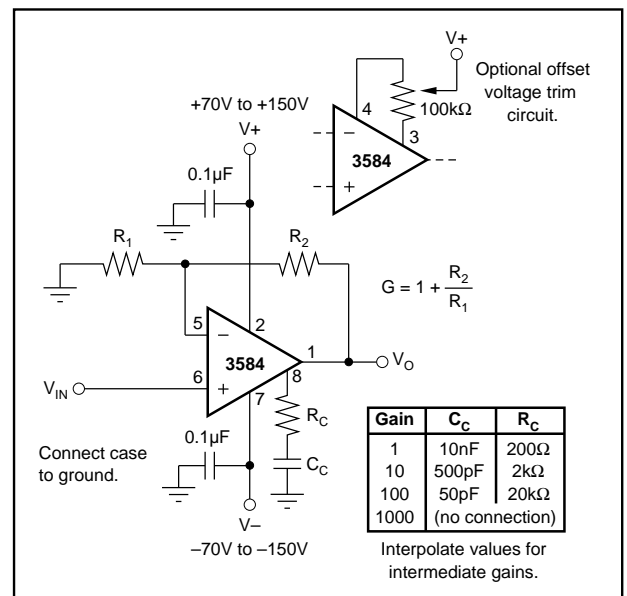


FIGURE 1. Basic Circuit Connections.

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