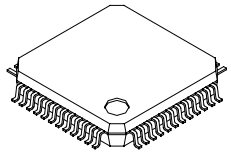
SONY

CXA1202Q-Z/CXA1202R

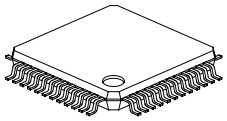
REC/PB Amplifier for VCR

For the availability of this product, please contact the sales office.

CXA1202Q-Z
48 pin QFP (Plastic)



CXA1202R
48 pin LQFP (Plastic)



Description

CXA1202Q-Z/CXA1202R are bipolar ICs developed as REC/PB amplifiers for VCR's.

Features

- Built-in head amplifier feedback dumping contributes to the reduction of external components and simplification of the print circuit board design.
- Built-in BPF for PB signals medium range frequency compensation totally eliminates external resonance circuits (L. C. R.)
- Low range recording signal variable-level mix amplifier allows for both metal powder and metal evaporated tapes application.
- Consumption saving through power save function of the REC AMP.
- 4-head system switch incorporated.

Functions

- Recording: 2-channel REC AMP, 5-input (Y, Chroma, AFM, ATF, PCM) Mix AMP.
- Playback: 2-channel low-noise head amplifier, medium range frequency compensation circuit, RF AGC, dropout detecting circuit.

Structure

Bipolar silicon monolithic IC

Applications

- 8-mm system VCR
- β-system VCR
- VHS-system VCR

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	8	V
• Operating temperature	Topr	–10 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D (CXA1202Q-Z)	920	mW
	P_D (CXA1202R)	1100	mW

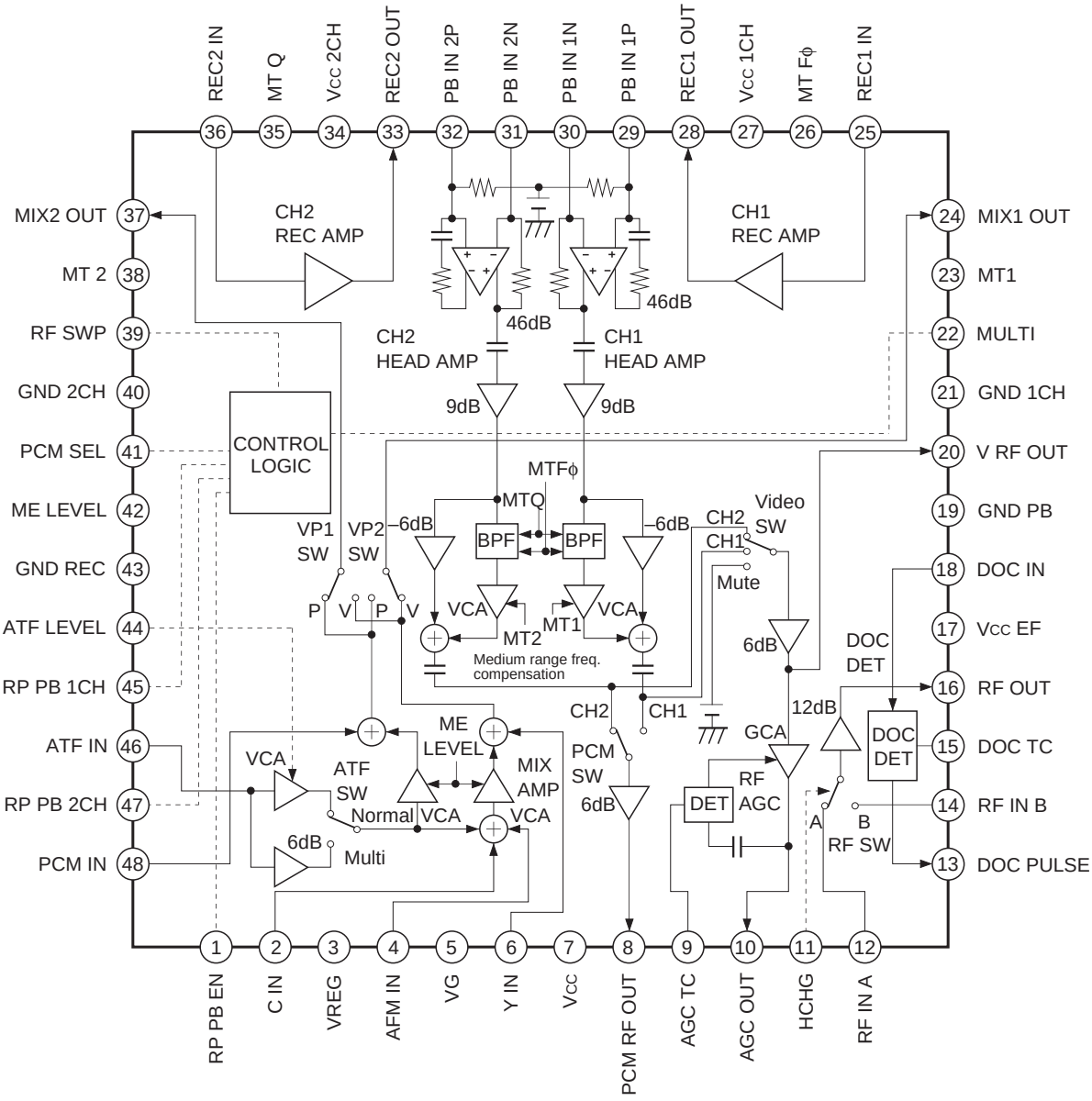
(CXA1202R: Substrate area 40 × 25mm^2, t = 0.635mm when ceramic print circuit board mounted)

Recommended Operating Condition

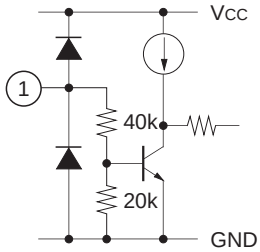
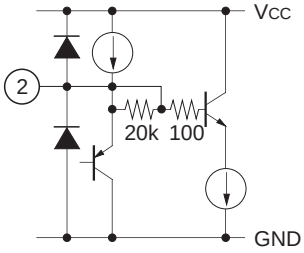
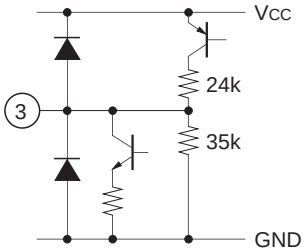
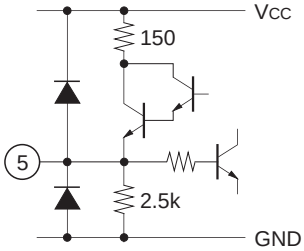
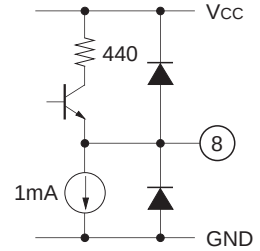
Supply voltage	Vcc	5 ± 0.25	V

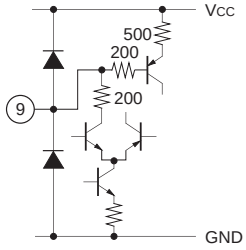
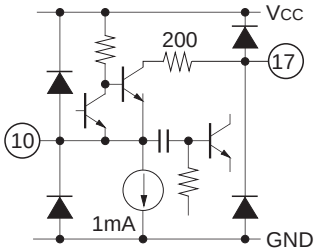
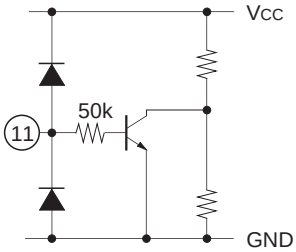
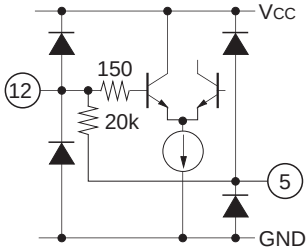
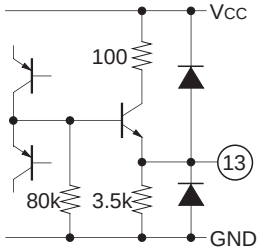
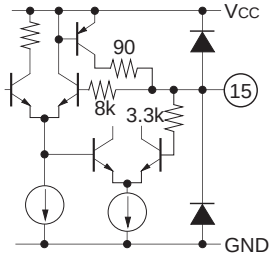
E88012-PS

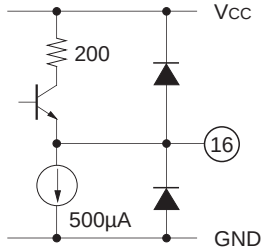
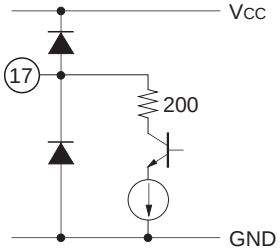
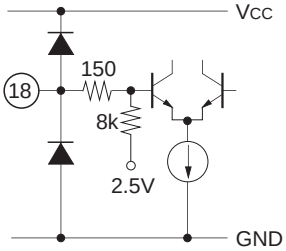
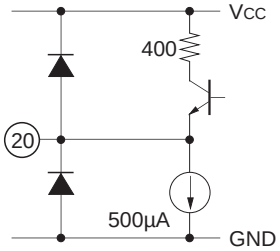
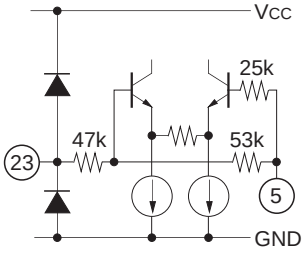
Block Diagram and Pin Configuration

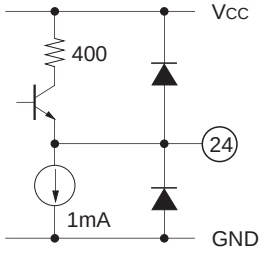
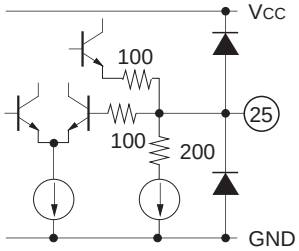
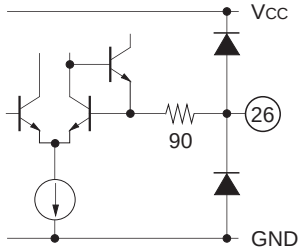
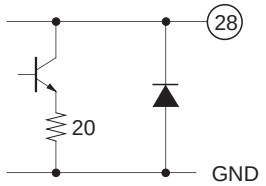
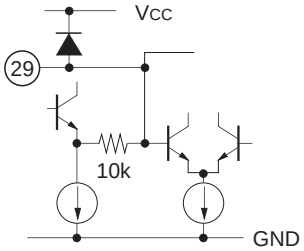
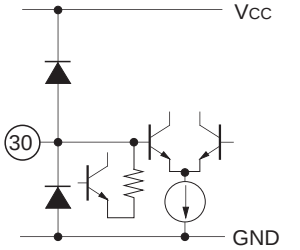


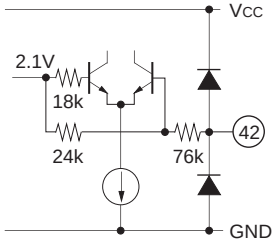
Pin Description

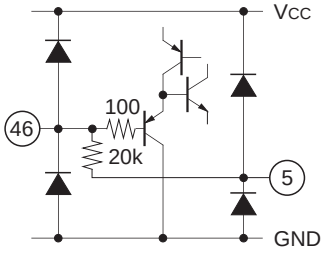
No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
1	RP PB EN	(Open: "L")	—	40kΩ		Power-save recording at Low. High: over 3V Low: under 1V
2	C IN	3.2V	134 mVp-p	20kΩ		Input pin for Chroma signal.
3	VREG	4.2V	—	—		Output pin for VREG 4.2V. Decoupling with capacitance.
4	AFM IN	3.2V	80 mVp-p	20kΩ	Same as for Pin No. 2	Input pin for AFM signal.
5	VG	2.5V	—	—		Output pin for virtual GND. Decoupling with capacitance.
6	Y IN	3.2V	250 mVp-p	20kΩ	Same as for Pin No. 2	Input pin for Y signal.
7	Vcc	5.0V	—	—	—	Supply pin for circuits other than REC AMP and Head AMP.
8	PCM RF OUT	1.8V	50 to 500 mVp-p	Emitter follower (I_E = 1mA)		Output pin for PB PCM signal.

No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
9	AGC TC	4.25V (Load: 150kΩ	—	—		Pin to apply time constant of envelope detection for RF AGC. Optimum load resistance across Vcc is 150kΩ.
10	AGC OUT	2.5V	100 mVp-p	Emitter follower (I_E = 1mA)		AGC output pin for PB VIDEO signal (Max. gain of AGC AMP is about 7dB).
11	HCHG	— (Open: "L")	—	50kΩ		Control signal input pin for RF SW switching: High (over 3V): selects RF IN A Low (under 0.3V): selects RF IN B
12	RF IN A	2.5V	100 mVp-p	—		Input pin for RF switch and 12dB AMP.
13	DOC PULSE	H: 3.2V L: 0V	—	Emitter follower (H: I_E = 1mA)		Dropout detection signal output pin; High upon dropout.
14	RF IN B	2.5V	100 mVp-p	20kΩ	Same as for Pin No. 12	Input pin for RF switch and 12dB AMP.
15	DOC TC	2.5V	—	—		Pin to connect time constant of dropout detection.

No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
16	RF OUT	2.5V	400 mVp-p	Emitter follower (I_E = 500µA)		Output pin of signal selected by HCHG from RF IN A and RF IN B.
17	Vcc EF	5.0V	—	—		Supply pin for emitter followers of AGC OUT, DOC TC and RF OUT.
18	DOC IN	2.5V	400 mVp-p	8kΩ		Input pin for dropout detection.
19	GND PB	0V	—	—	—	GND pin for medium range frequency compensation circuit, RF AGC and DOC DET.
20	V RF OUT	1.8V	50 to 500 mVp-p	Emitter follower (I_E = 500µA)		Output pin for PB VIDEO signal.
21	GND 1CH	0V	—	—	—	GND pin for CH1 REC AMP and CH1 Head AMP.
22	MULTI	— (OPEN: "L")	—	40kΩ	Same as for Pin No. 1	Multi-channel PCM REC mode at High.
23	MT1	— (2.5V at OPEN of pin)	—	100kΩ		Boost level adjusting pin for CH1 medium range frequency compensation circuit. Variable between 0 and +12dB at 4.2 to 0.8V.

No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
24	MIX1 OUT	2.5V	203 mVp-p	Emitter follower (I_E = 1mA)		Mix circuit output pin for CH1.
25	REC1 IN	1.8V	92µA (Y signal)	≃ 0		CH1 REC AMP input pin.
26	MT Fϕ	2.5V	—	—		Fϕ adjusting pin for medium range frequency compensation circuit; Fϕ is controlled through current value by connecting resistance between GNDs. Mutually affected by MT Q. Do not connect capacitance.
27	Vcc 1CH	5.0V	—	—	—	Power supply pin for CH1 REC AMP and CH1 Head AMP.
28	REC1 OUT	15mA	13 mAp-p	Open collector		CH1 REC AMP output pin.
29	PB IN 1P	2.4V	90 to 900 µVp-p	1.3kΩ		CH1 head AMP positive phase input pin (PB signal input pin).
30	PB IN 1N	2.4V	—	1.3kΩ		CH1 Head AMP inverter phase input pin (decoupling with capacitance).

No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
31	PB IN 2N	2.4V	—	1.3kΩ	Same as for Pin No. 30	CH2 Head AMP Inverter phase input pin (decoupling with capacitance).
32	PB IN 2P	2.4V	90 to 900 µVp-p	1.3kΩ	Same as for Pin No. 29	CH2 Head AMP positive phase input pin (PB signal input pin).
33	REC2 OUT	15mA	13 mAp-p		Same as for Pin No. 28	CH2 REC AMP output pin.
34	Vcc 2CH	5.0V	—	—	—	Power supply pin for CH2 REC AMP and CH2 Head AMP.
35	MT Q	2.5V	—	—	Same as for Pin No. 26	Q adjusting pin for medium range frequency compensation circuit. Controls Q through current value by connecting resistance between GNDs; Mutually effected by MT Fϕ. Do not connect capacitance.
36	REC2 IN	1.8V	92µA (Y signal)	≃ 0	Same as for Pin No. 25	CH2 REC AMP input pin.
37	MIX2 OUT	2.5V	203 mVp-p	Emitter follower (I_E = 1mA)	Same as for Pin No. 24	Mix circuit output pin for CH2.
38	MT 2	— (2.5V at OPEN of pin)	—	100kΩ	Same as for Pin No. 23	Boost level adjusting pin for CH2 medium range frequency compensation circuit; variable between 0 and +12dB at 4.2 to 0.8V.
39	RF SWP	— (Open: "L")	—	40kΩ	Same as for Pin No. 1	RF switching pulse input pin for CH switchover.
40	GND 2CH	0V	—	—	—	GND pin for CH2 REC AMP and CH2 head AMP.
41	PCM SEL	— (Open: "L")	—	40kΩ	Same as for Pin No. 1	PCM AREA input pin; High: PCM REC period During High period after recording, MUTE is applied to PB VIDEO output.
42	ME LEVEL	— (2.1V at OPEN of pin)	—	100kΩ		Level of low range REC signals (Chroma, AFM, ATF rec. with VIDEO) can be boosted by 0 to 3dB by voltage (0 to 5V) applied to this pin.

No.	Symbol	Voltage		I/O resistance	Equivalent circuit	Description
		DC	AC			
43	GND REC	0V	—	—	—	GND pin for VG, VREG, LOGIC and mix circuit.
44	ATF LEVEL	— (2.1V at OPEN of pin)	—	100kΩ	Same as for Pin No. 42	REC level of ATF signal can be boosted by 0 to 3dB by the voltage (0 to 5V) applied to this pin. In multi PCM mode, priority given to 6dB AMP.
45	RP PB 1CH	— (Open: "L")	—	40kΩ	Same as for Pin No. 1	REC/PB switchover signal for CH1: High: PB Low: REC However, when RP PB EN pin is at Low: High: power save REC Low: REC
46	ATF IN	2.5V	250 mVp-p	20kΩ		Input pin for ATF pilot signal.
47	RP PB 2CH	— (Open: "L")	—	40kΩ	Same as for Pin No. 1	REC/PB switchover signal for CH2: High: PB Low: REC However, when RP PB EN pin is at Low: High: power save REC Low: REC
48	PCM IN	3.2V	250 mVp-p	20kΩ	Same as for Pin No. 2	Input pin for PCM signal.

Electrical Characteristics

(Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit.)

No.	Item		Symbol	Test conditions					Test point, Ammeter name	Test method	Min.	Typ.	Max.	Unit
				Input condition			Control logic*1	Other SW ON						
				Input pin	Level	Frequency								
<Recording>														
1	REC mode circuit current		I_{REC}				A	42, 44	I_{VCC}	In both CH REC, internal consumption current (excluding REC output current)	20.5	27.5	35.0	mA
2	Mix AMP Y gain	CH1	G_{Y1}	6	250 mVp-p	1MHz	A		24		–2.6	–1.8	–1.0	dB
		CH2	G_{Y2}						37					
3	Mix AMP Y frequency response	CH1	V_{FY1}	6	250 mVp-p	10MHz 1MHz	B		24	$\frac{\text{10MHz level}}{\text{1MHz level}}$	–1.0	–0.2		dB
		CH2	V_{FY2}						37					
4	Mix AMP Y secondary distortion factor	CH1	D_{Y1}	6	500 mVp-p	5MHz	C		24			–50	–40	dB
		CH2	D_{Y2}						37					
5	Mix AMP PCM gain	CH1	G_{P1}	48	250 mVp-p	1MHz	F		24		–2.8	–1.8	–0.8	dB
		CH2	G_{P2}				E		37					
6	Mix AMP PCM frequency response	CH1	V_{FP1}	48	250 mVp-p	10MHz 1MHz	J		24	$\frac{\text{10MHz level}}{\text{1MHz level}}$	–1.0	–0.2		dB
		CH2	V_{FP2}				K		37					
7	Mix AMP PCM secondary distortion factor	CH1	D_{P1}	48	500 mVp-p	5MHz	K		24			–50	–40	dB
		CH2	D_{P2}						37					
8	Mix AMP Chroma gain		G_{C1}	2	150 mVp-p	750kHz	D		24	At min. gain of 0V at ME LEVEL pin	–12.7	–11.7	–10.7	dB

*1 See the Control Logic Truth Table for control logic conditions.

(Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit.)

No.	Item	Symbol	Test conditions					Test point, Ammeter name	Test method	Min.	Typ.	Max.	Unit
			Input condition			Control logic*1	Other SW ON						
			Input pin	Level	Frequency								
9	Mix AMP Low range freq. (Chroma, AFM, ATF rec. with VIDEO) variable gain by ME LEVEL pin	ΔG_{ME}	2	150 mVp-p	750kHz	D		24	Change in gain when ME LEVEL pin is brought from 0 to 5V	2.4	3.4	4.4	dB
						E	42						
10	Mix AMP Chroma secondary distortion factor	D_{CI}	2	250 mVp-p	750kHz	K	42	24	At max. gain of 5V at ME LEVEL pin		–50	–40	dB
11	Mix AMP AFM gain	G_{AF1}	4	100 mVp-p	1.5MHz	D		37	At min. gain of 0V at ME LEVEL pin	–11.2	–10.1	–9.0	dB
12	Mix AMP AFM secondary distortion factor	D_{AF1}	4	250 mVp-p	1.5MHz	F	42	37	At max. gain of 5V at ME LEVEL pin		–50	–40	dB
13	Mix AMP ATF gain (rec. with VIDEO)	G_{ATV}	46	250 mVp-p	100kHz	J		37	At min. gain of 0V at both ME LEVEL pin and ATF LEVEL pin	–28.9	–27.6	–26.3	dB
14	Mix AMP ATF gain (rec, with PCM)	G_{ATP}	46	250 mVp-p	100kHz	J		24	At min. gain of 0V at both ME LEVEL pin and ATF LEVEL pin	–28.9	–27.6	–26.3	dB
15	Mix AMP ATF variable gain by ATF LEVEL pin	ΔG_{ATA}	46	250 mVp-p	100kHz	J		37	Change in gain when ATF LEVEL pin is brought from 0 to 5V	2.4	3.4	4.4	dB
							44						
16	Mix AMP ATF rec. with PCM variable gain by ME LEVEL pin	ΔG_{ATM}	46	250 mVp-p	100kHz	J		24	Change in gain when ME LEVEL pin is brought from 0 to 5V	2.3	3.3	4.3	dB
							42						

*1 See the Control Logic Truth Table for control logic conditions.

(Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit.)

No.	Item		Symbol	Test conditions					Test point, Ammeter name	Test method	Min.	Typ.	Max.	Unit
				Input condition			Control logic*1	Other SW ON						
				Input pin	Level	Frequency								
17	Mix AMP ATF gain increment at multi PCM		ΔG_{ATMU}	46	250 mVp-p	100kHz	J		24	Change in gain when control logic is set to multi PCM	4.9	5.9	6.9	dB
							G							
18	REC AMP output bias current	CH1	I_{DR1}				A		I_{REC1}	DC current testing	13.4	15.7	18.0	mA
		CH2	I_{DR2}						I_{REC2}					
19	REC AMP output bias current	CH1	I_{R1}	25	200 mVp-p	1MHz	F		28	$\frac{\text{Output level [V]}}{100\ [\Omega]}$	12.0	13.2	14.4	mA p-p
		CH2	I_{R2}	36					33					
20	REC AMP channel balance		ΔV_{R21}	25	200 mVp-p	1MHz	F		28	Difference in output level between CH1 and CH2	–0.8	0.0	0.8	dB
				36					33					
21	REC AMP frequency response	CH1	ΔV_{FR1}	25	200 mVp-p	10MHz 1MHz	B		28	$\frac{\text{10MHz level}}{\text{1MHz level}}$	–3.2	–2.1		dB
		CH2	ΔV_{FR2}	36					33					
22	REC AMP secondary distortion factor	CH1	D_{R1}	25	300 mVp-p	5MHz	E		28			–49	–40	dB
		CH2	D_{R2}	36					33					
<Playback>														
23	Head AMP VRF OUT gain	CH1	G_{V1}	29	200 µVp-p	1MHz	H	23	20		52.2	54.5	57.2	dB
		CH2	G_{V2}	32			I	38						
24	Head AMP PCM RF OUT gain	CH1	G_{P1}	29	200 µVp-p	1MHz	I	23	8		52.2	54.5	57.2	dB
		CH2	G_{P2}	32			H	38						
25	AGC OUT level		V_{AGC}	29	200 µVp-p	5MHz	H	23	10		70	95	120	mV p-p

*1 See the Control Logic Truth Table for control logic conditions.

(Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit.)

No.	Item		Symbol	Test conditions					Test point, Ammeter name	Test method	Min.	Typ.	Max.	Unit
				Input condition			Control logic*1	Other SW ON						
				Input pin	Level	Frequency								
26	AGC control characteristics "H"		ΔV_{AGCH}	29	900 µVp-p / 200 µVp-p	5MHz	H	23	10	Output level at input 900µV / Output level at input 200µV	–0.3	0.5	1.3	dB
27	AGC control characteristics "L"		ΔV_{AGCL}	29	100 µVp-p / 200 µVp-p	5MHz	H	23	10	Output level at input 100µV / Output level at input 200µV	–0.8	–0.1	0.6	dB
28	DC offset between channels CH1 – CH2		ΔV_{DC12}	29	100 µVp-p	1MHz	H	23	10	DC voltage testing At CH1 Low input – at CH2 High input At CH2 High input – at CH1 Low input	–60	0	60	mV
				32	900 µVp-p		I	38						
29	DC offset at MUTE, CH1, CH2 – MUTE		ΔV_{DCM}	29	100 µVp-p	1MHz	H → J	23	10	Difference of DC voltage at logic switchover	–60	0	60	mV
				32			I → J	38						
30	RF SW gain	A input	G_{RFA}	12	100 mVp-p	300kHz	H	11	16		11.1	12.1	13.1	dB
		B input	G_{RFB}	14			I							
31	RF SW frequency response	A input	ΔV_{FRFA}	12	100 mVp-p	10MHz 300kHz	J	11	16	10MHz level / 300kHz level	–2.0	–0.4		dB
		B input	ΔV_{FRFB}	14			K							
32	Dropout detection, ON level		$V_{D\ ON}$	12	See the following figure *2		H	11	18	Pin 18 level when DOC PULSE pin becomes High (0dB = 400mVp-p)	–16.5	–13.0	–10.5	dB

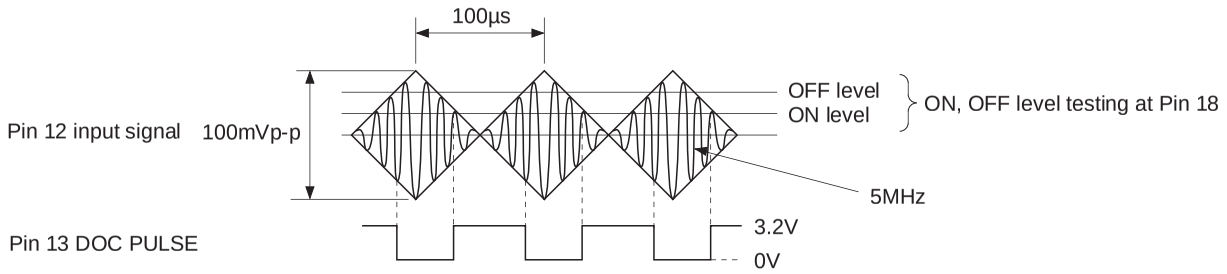
*1 See the Control Logic Truth Table for control logic conditions.

(Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit.)

No.	Item	Symbol	Test conditions					Test point, Ammeter name	Test method	Min.	Typ.	Max.	Unit
			Input condition			Control logic*1	Other SW ON						
			Input pin	Level	Frequency								
33	Dropout detection, OFF level	$V_{D\ OFF}$	12	see the figure below *2		I	11	18	Pin 18 level when DOC PULSE pin becomes Low (0dB = 400mVp-p)	–9.5	–7.0	–5.0	dB
34	Dropout pulse, Low level	V_{PDL}	12	100 mVp-p	5MHz	H	11	13	DC voltage testing		0.0	0.1	V
35	Dropout pulse, High level	V_{PDH}				H	11	13	DC voltage testing	3.1	3.2	3.4	V
36	PB mode circuit current	I_{PB}				H		I_{VCC}	Current consumption with both CHs in PB	30.0	40.0	50.5	mA
<Standard voltage supply in IC>													
37	VG pin DC voltage	V_G				H		5		2.41	2.51	2.61	V
38	VREG pin DC voltage	V_{REG}				A	42.44	3		4.08	4.23	4.38	V

*1 See the Control Logic Truth Table for control logic conditions.

*2 Signal description of dropout detection.



Control Logic Truth Table

Input condition and operation	Control logic input condition								Operation of each section under respective input condition									Mode
									Recording				Playback					
Control logic condition	(Pin 1) RP PB EN	(Pin 45) RP PB 1CH	(Pin 47) RP PB 2CH	(Pin 39) RF SWP	(Pin 22) MULTI	(Pin 41) PCM SEL	(Pin 24) MIX1 OUT	(Pin 37) MIX2 OUT	(Pin 28) REC1 OUT	(Pin 33) REC2 OUT	CH1 HEAD AMP	CH2 HEAD AMP	medium range freq. compensation circuit, DOC DET, RF SW	(Pin 8) PCM RF OUT	(Pin 10) AGC OUT	(Pin 20) V RF OUT	Operation	
A	H	L	L	L	L	L	V	V	V	V	X	X	X	X	X	X	VIDEO REC	REC
B	L	L	L	L	L	L	V	V	V	V	X	X	X	X	X	X	Power save VIDEO REC	
C	L	H	L	L	L	L	V	V	X	V	X	X	X	X	X	X		
D	L	L	H	L	L	L	V	V	V	X	X	X	X	X	X	X		
E	H	L	L	H	L	H	V	P	V	P	X	X	X	X	X	X	VIDEO • PCM REC	
F	H	L	L	L	L	H	P	V	P	V	X	X	X	X	X	X		
G	H	L	L	—	H	—	MP	MP	MP	MP	X	X	X	X	X	X	MULTI PCM REC	
H	H	H	H	H	—	L	X	X	X	X	O	O	O	CH2	CH1	CH1	PB	PB
I	H	H	H	L	—	L	X	X	X	X	O	O	O	CH1	CH2	CH2		
J	H	L	H	L	L	H	P	V	P	X	X	O	O	O (No signal)	MUTE	MUTE	VIDEO • PCM PCM after recording	PCM after recording
K	H	H	L	H	L	H	V	P	X	P	O	X	O	O (No signal)	MUTE	MUTE		
L	H	L	H	L	H	H	MP	MP	MP	X	X	O	O	O (No signal)	MUTE	MUTE	MULTI • PCM PCM after recording	
M	H	H	L	H	H	H	MP	MP	X	MP	O	X	O	O (No signal)	MUTE	MUTE		

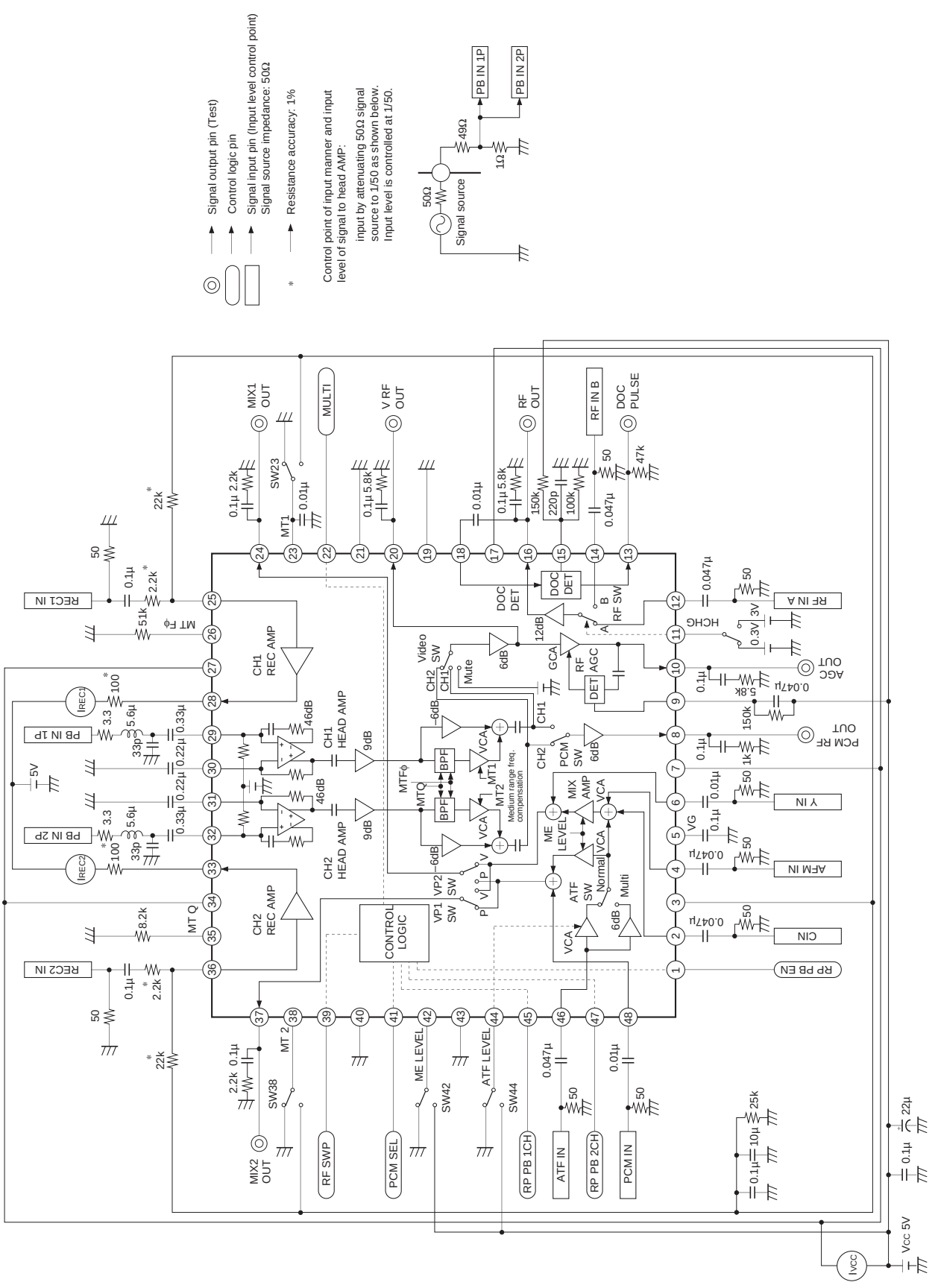
1. Description of input condition
   "High" … Control logic input, over 3V.
   "Low" …. Control logic input, under 1V.
   "—" …… Independent of High, Low.

2. Description of operation mode
   O ……. Operating
   X ……. Not operating

   • In recording mode
   V ..... VIDEO signal is output.
   P ..... PCM signal is output.
   MP..... ATF signal that passed through fixed 6-dB AMP in mix circuit is output, mixed with PCM signal.

   • In playback mode
   CH1 ..... CH1 signal is output.
   CH2 ..... CH2 signal is output.
   MUTE ... MUTE is applied to PB VIDEO signal in PCM after recording; at the same time, RF AGC gain is held.

Electrical Characteristics Test Circuit



Description of Operations

The functional blocks, voltage supply and GND pins of CXA1202Q-Z and CXA1202R are configured as follows:

Block name		Voltage supply pin	GND pin
Mix AMP + SW section		7	43
REC AMP section	CH1	27	21
	CH2	34	40
Head AMP section	CH1	27	21
	CH2	34	40
Medium range frq. compensation circuit + SW section		7	19
RF AGC section		7, 17 (Output emitter follower section)	19
RF SW section		7, 17 (Output emitter follower section)	19
Dropout detecting section		7, 17 (Peak hold section)	19
Control logic section		7	43
Standard voltage supply section in IC (VREG, VG)		7	43

Individual blocks are described in the following paragraphs.

[Mix AMP + SW]

Here, each of Y, Chroma, AFM, ATF and PCM signals is input at a prescribed input level so that they are mixed together internally to achieve an appropriate current value at the head, and output to MIX1 OUT pin (CH1 signal) and MIX2 OUT (CH2 signal) at a correct timing.

Control is possible at ATF LEVEL pin (0 to 3dB at 0 to 5V, OPEN not allowed) when only the ATF recording level is to be increased as required, and at ME LEVEL pin (0 to 3dB at 0 to 5V, OPEN not allowed) when only the low range signal (Chroma + AFM + ATF) recording level is to be increased.

In MULTI PCM mode, the ATF recording level is boosted by 6dB.

In SW, the signal is output to MIX1 OUT and MIX2 OUT pins under control of the control logic section.

[REC AMP]

Mix AMP + SW output is input after it is converted into a suitable current by an external resistor, to drive the head. Adjustment of the external resistor makes it possible to set a gain and DC bias current to match that of the head.

Feedback dumping is applied to inhibit head resonance (refer to the Application Circuit), and take care that capacitance coupling will not occur across the input and output.

Control signals of RP PB EN, RP PB 1CH and RP PB 2CH permit power saving in the channels while recording (refer to the Control Logic Truth Table). Power saving of about 85mW is possible through a single channel.

[Head AMP]

The playback signal from the head is amplified with low noise and high gain. For example, the equivalent input noise level at 1MHz is 662pVrms/ $\sqrt{Hz}$.*1

In PB, the total input capacitance*2 will be about 75pF. To inhibit resonance between this capacitance and the head inductance, a feedback dumping is incorporated.

Connect a bypass capacitor for PB IN 1N and PB IN 2N pins between these pins and the rotary transformer Vcc. So far as this capacitor is over 0.2µF, the low-level frequency response does not deteriorate. Beside the 0.1µF good frequency response capacitor connected to pin VREG, by adding a capacitor of over 10µF, degradation of noise level at low range can be prevented.

Take care not to allow capacitance coupling between PB output and Head AMP input.

*1 and *2 See the next page.

[Medium range frequency compensation circuit + SW]

This corrects the frequency response of the PB signal. It is possible to set to and Q magnitude by means of the external resistance value of MT Fϕ and MTQ pins (refer to the Fϕ graph). The amount of boost may be adjusted through the external volumes of MT1 and MT2 pins (refer to the graph showing the effect of standard response MT2 pin voltage on the amount of boost).

By controlling the control logic section, SW is changed over with the timing of RF SW (switching pulse), to output PCM RF signals and VIDEO RF signals. Mute is applicable to VIDEO RF signals during PCM after recording within the PCM recording area period.

[RF AGC]

The played back VIDEO RF signal are output here to achieve a constant level of 100mVp-p. The time constant for AGC is set by means of the resistance and capacitance external to AGC TC pin.

At the input section of the detector a HPF with a cutoff frequency of about 1MHz is incorporated. This is to permit detection within the Y signal band.

In PCM after recording, MUTE applies during the PCM recording area period to keep the gain on an unchanged level.

[RF SW]

Signals input to RF IN A and RF IN B pins are selected by means of HCHG control signals and output via the 12-dB amplifier to RF OUT pin. This switch is utilized for SP/LP head changeover when a 4-head system is employed.

[Dropout detection]

Dropout is detected here from RF signals of played-back VIDEO and dropout pulse is output. The time constant is set by means of the external resistance and capacitance external to DOC TC pin.

The detection level is set in the interior with 400mVp-p input as standard to obtain optimum level.

Use an external coupling capacitance value of input of 47pF to achieve HPF function.

[Control Logic]

The IC is controlled from this section as it will save power when circuit blocks are not in use. Therefore, power saving is automatically executed while all the power supplies are switched on. Many SWs are also available to switch inputs or outputs with complicated timing. Internal logic circuits to control them are provided.

It is possible to achieve all possible combinations of inputs/outputs necessary for the basic operations by means of the 13 modes shown in the Control Logic Truth Table.

L is set when the control logic pin is open.

[Standard voltage supplies in the IC]

VREG 4.2V and VG 2.5V are provided as the standard voltage supplies in the IC.

*1 (Reference) Test Method of Head AMP C/N

(1) input signal

Level –42.0dBm [signal source: 50Ω]

(generates a voltage of 100μVp-p at both ends of 1Ω).

(2) Signal injection circuit

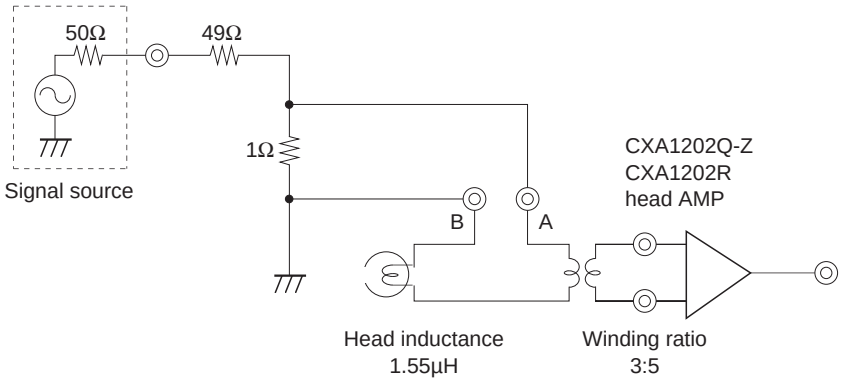
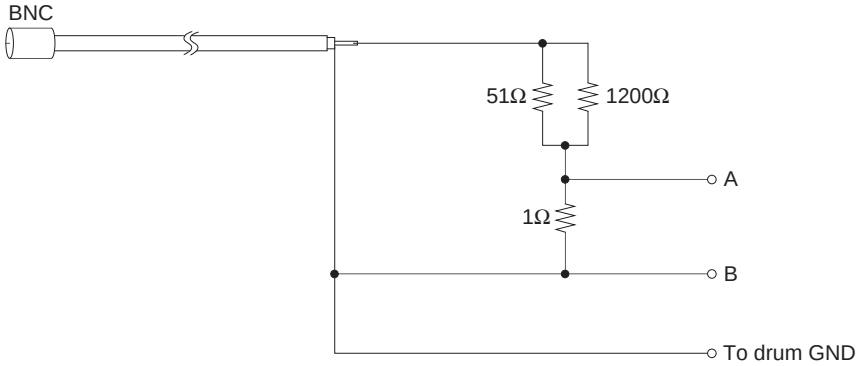


Fig. 1

The signal is input from A and B in Fig. 1. The equipment used for the input is shown in Fig. 2.

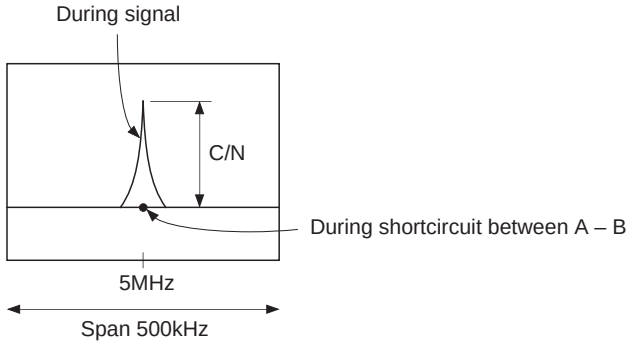


Notes) 1. A chip resistance is used for 1Ω (ordinary carbon resistance produces inductance.)
2. 49Ω is composed of 51Ω/1200Ω.

Fig. 2

(3) SPECTRUM ANALYZER setting conditions:

RBW: 10kHz
VBW: 1Hz
Sweep time: 500s
Span: 500kHz



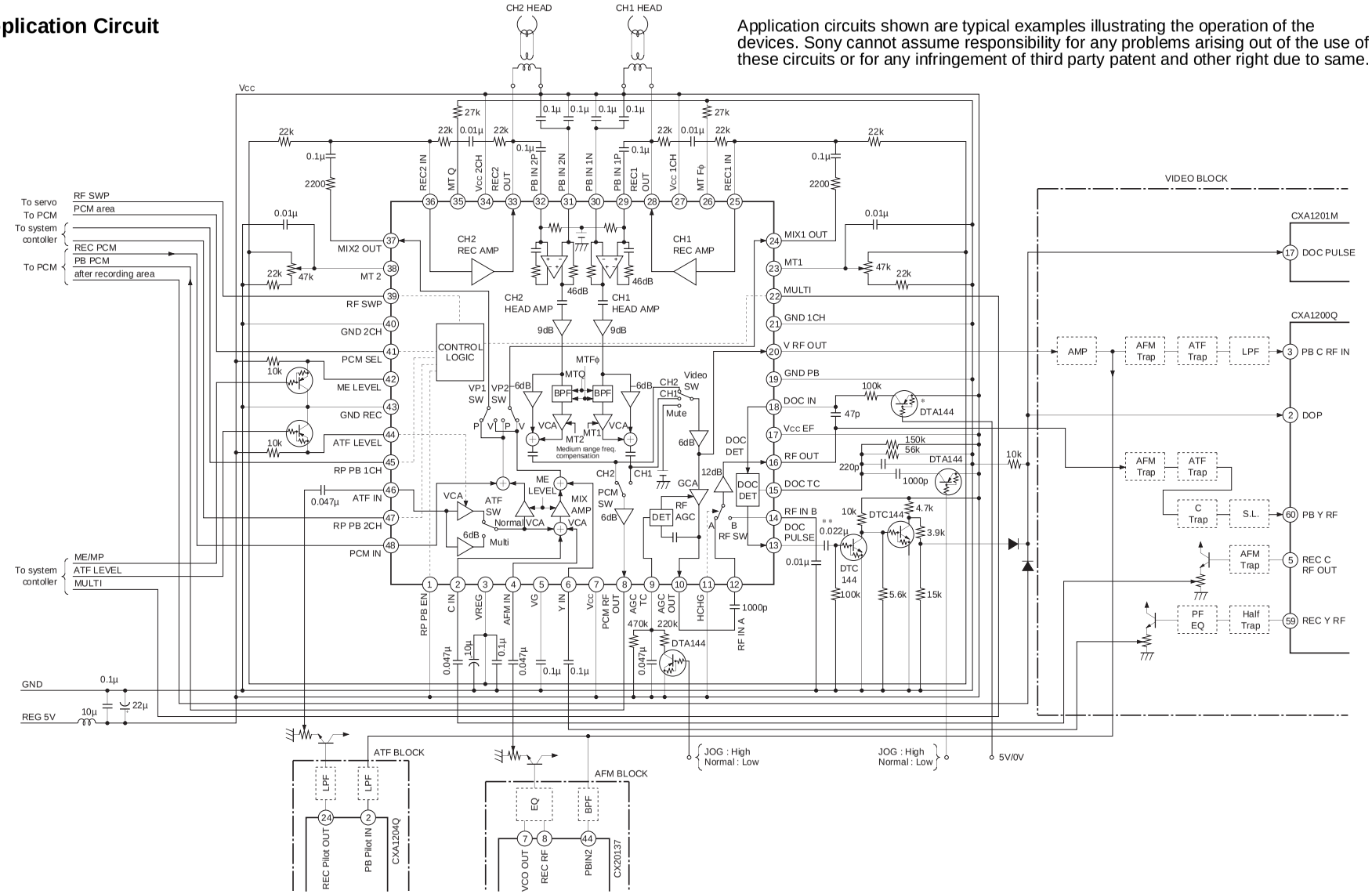
(4) Keep the medium range frequency compensation circuit flat. (Voltage of Pins MT1 and MT2 is made equal to that of Pin VREG)

(5) Observe the output at Pin 20 V RF OUT.

*2 The total input capacitance includes all capacitances of REC AMP, rotary transformer, shielding wire, etc., in addition to the input capacitance of the Head AMP alone (47pF).

Application Circuit

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

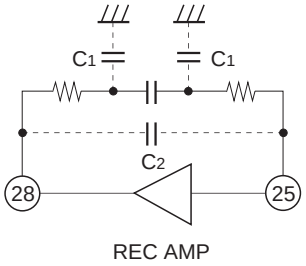


* Countermeasure for drop out pulse in EE or editing mode.
On a Virgin tape, drop out pulse shows with EE or editing mode in the absence of playback output. In such case CXA1201M holds AGC gain. This may cause image disturbance at the beginning of either recording or editing from EE mode.
To prevent this inconvenience, a 0V signal in recording and 5V in playback, synchronized with the REC/PB signal of CXA1201M is entered. At 0V, the voltage of Pin 18 rises as if the input level for drop out detection had increased.
This prevents the drop out pulse even if there is no signal.

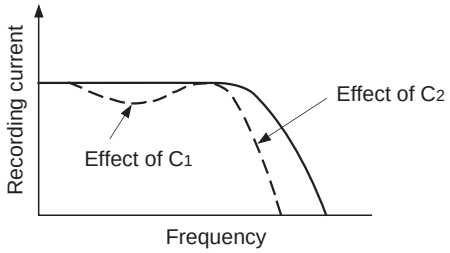
** Drop out countermeasures for virgin tape in playback.
During playback of virgin tape, as drop out pulse is generated, drop out compensation is activated for long periods to deal with noise. V sync is disturbed and the picture loses its clarity.
To prevent that, drop out pulse is passed through HPF and after continuation for a certain period the pulse disappears.

Precautions

1. Do not connect parasite capacitance to REC AMP dumping.



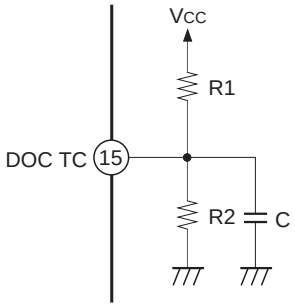
REC AMP



2. Do not bring Head AMP input near PB output.
   Normally, there is a gain of 67dB between Head Amp input (Pins 29, 30) and RFOUT (Pin 16). During no signal, the gain is 74dB (as AGC reaches maximum gain). Bringing those closer on the pattern may cause oscillations in the vicinity of 6 to 7MHz.

3. Use 150kΩ for RF AGC time constant, Resistance
   Because a change in this R causes a change in the AGC output level, change the time constant using the value of capacitance.

4. Watch the time constant of dropout detection.



Time constant: $t = C \times (R1//R2)$

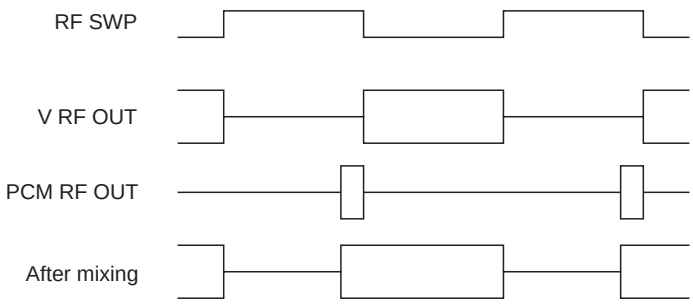
C: over 150pF

R1, R2: $5 \times \frac{R2}{R1 + R2} = 1.2$ to 2.0V

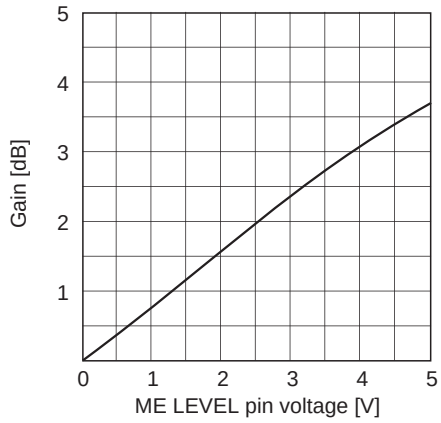
Oscillations may occur unless this condition is satisfied.

5. Take AFM PB output from V RF OUT (Pin 20)
   Passing AFM signal through RF AGC causes AGC to reach maximum gain when playing back a virgin tape. As a result MUTE may not apply to AFM IC (CX20137, CX20037).

6. Adjust tape path by mixing V RE OUT signal and PCM RF OUT signal. In the absence of a signal before switching, observe the envelope comprising the combination of the VIDEO area and the PCM area by mixing outputs from V RF OUT (Pin 20) and PCM RF OUT (Pin 8).

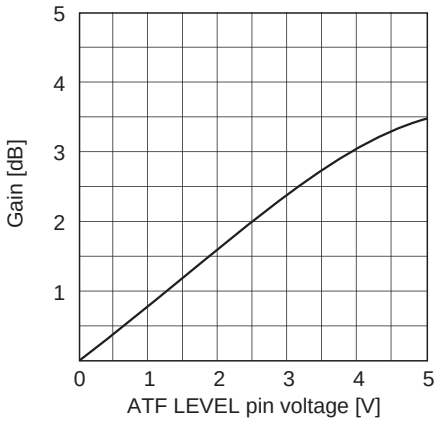


Mix AMP Chroma gain vs. ME LEVEL pin voltage



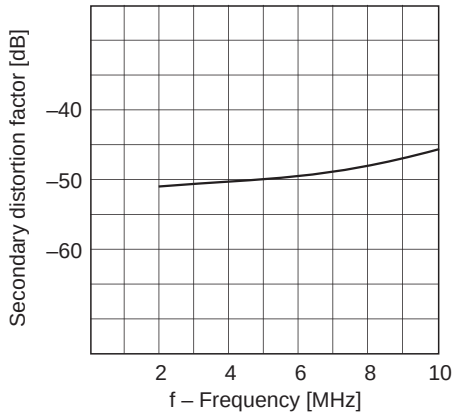
Conditions: Input: Pin 2, 126mVp-p, 750kHz
Output: Pin 24
Logic A

Mix AMP ATF gain vs. ATF LEVEL pin voltage



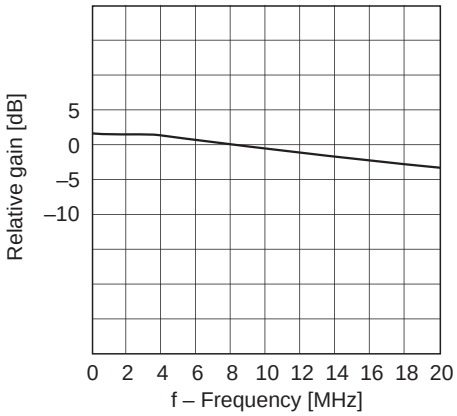
Conditions: Input: Pin 46, 250mVp-p, 100kHz
Output: Pin 24
Logic A

Mix AMP Y output secondary distortion factor vs. Frequency



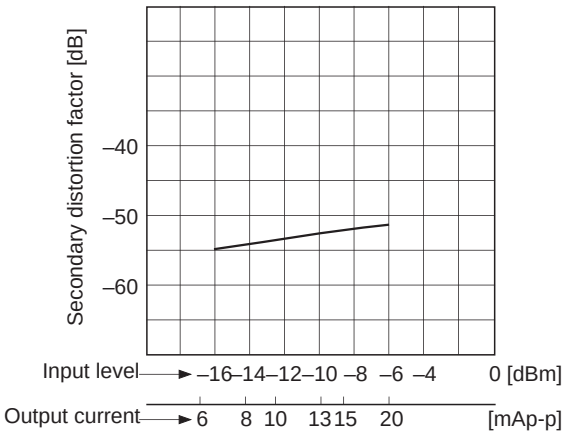
Conditions: Input: Pin 6, 250mVp-p
Output: Pin 37
Logic A

REC AMP frequency response



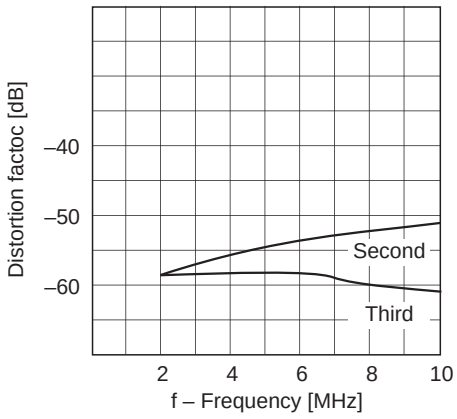
Conditions: Input: At resistance (2.2kΩ) with Pin 25, 200mVp-p
Output: Pin 28, load resistance: 100Ω
Logic A

REC AMP secondary distortion factor vs. input level, output current



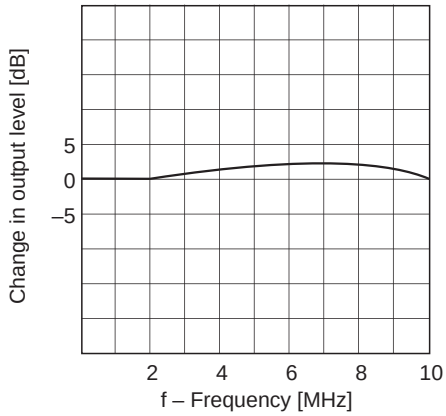
Conditions: Input: At resistance (2.2kΩ) with Pin 25, 5MHz
Output: Pin 28, load resistance: 100Ω
Logic A

REC AMP distortion factor vs. Frequency



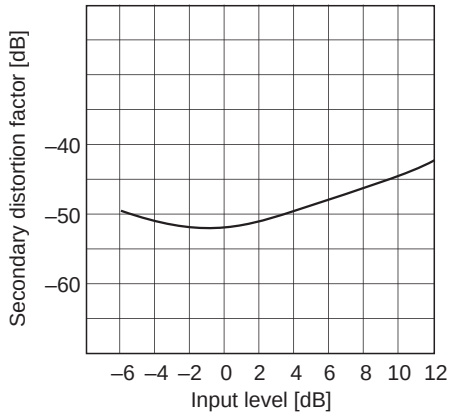
Conditions: Input: At resistance (2.2kΩ) with Pin 25, 200mVp-p
Output: Pin 28, load resistance: 100Ω
Logic A

Head AMP output level vs. Frequency



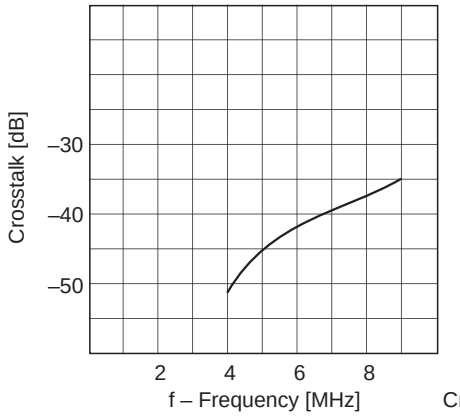
Conditions: Input: 25µm-wide head for NTSC, 100mVp-p at head tip
Output: Pin 20
Logic H, medium range freq. conpensation circuit boost: 0

V RF OUT secondary distortion factor vs. Input level

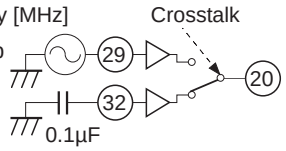


Conditions: Input: Pin 29, 0dB = 200mVp-p, 5MHz
Output: Pin 20
Logic H

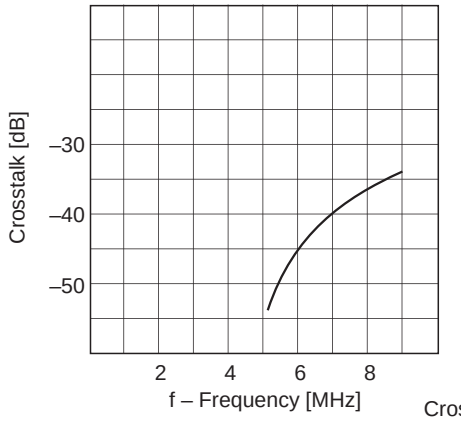
CH1 → CH2 crosstalk at RF OUT vs. Frequency



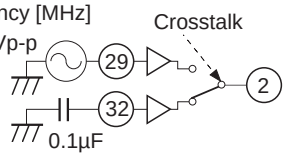
Conditions: Input: Pin 29, 200µVp-p
Output: Pin 20
Logic I



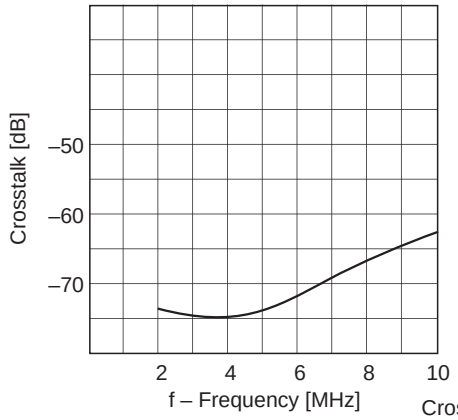
CH1 → CH2 crosstalk at PCM RF OUT vs. Frequency



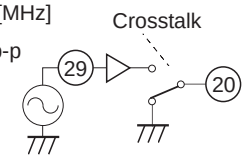
Conditions: Input: Pin 29, 200µVp-p
Output: Pin 8
Logic H



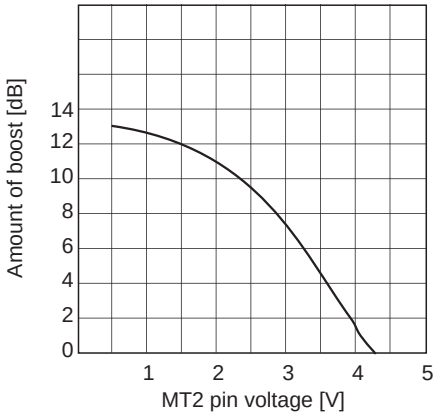
Crosstalk in MUTE at V RF OUT vs. Frequency



Conditions: Input: Pin 29, 200µVp-p
Output: Pin 20
Pin 41 voltage: 5V
Logic H

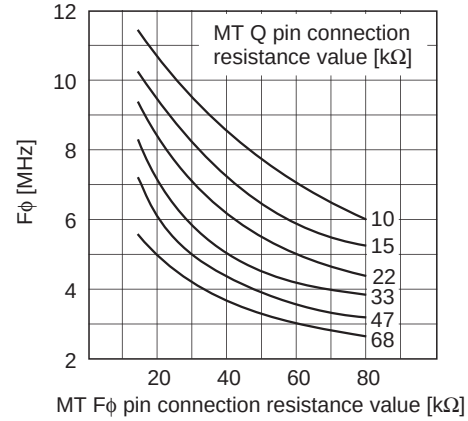


Medium range freq. compensation circuit MT2 pin voltage vs. Amount of boost

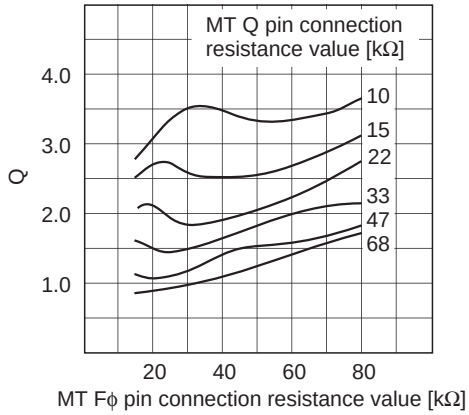


Conditions: MT Fϕ pin: 18kΩ
MT Q pin: 33kΩ

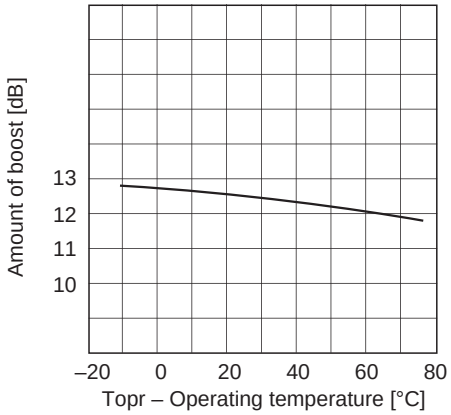
Medium range freq. compensation circuit MT Fϕ, MT Q pin connection resistance value vs. Fϕ



Medium range freq. compensation circuit MT Fϕ, MT Q pin connection resistance value vs. Q

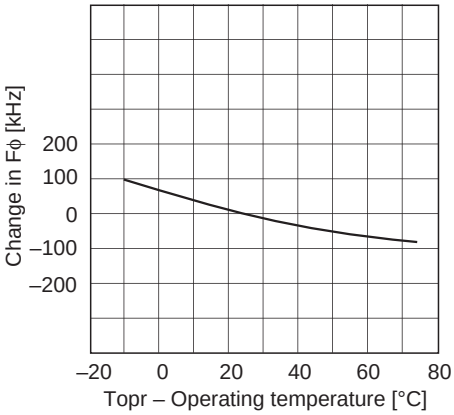


Medium range freq. compensation circuit boost amount vs. Operating temperature



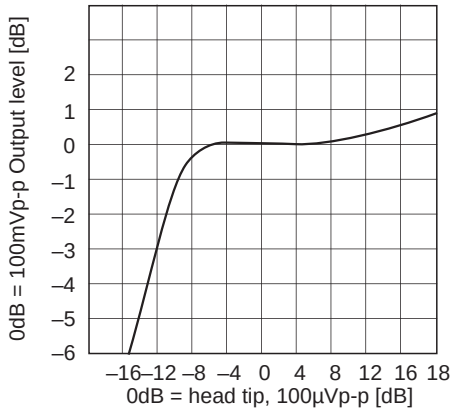
Conditions: Input: Pin 29
Output: Pin 20
Pin 23 voltage: 4.2V
Logic H

Medium range freq. compensation circuit Fϕ, vs. Operating temperature



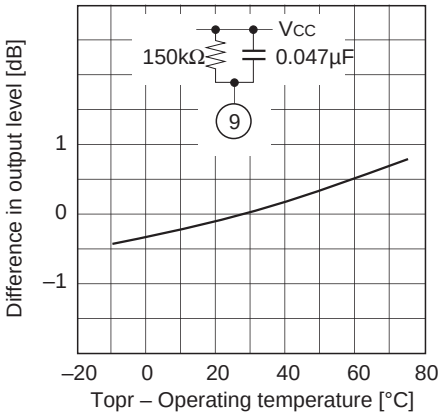
Conditions: Input: Pin 29
Output: Pin 20
Pin 23 voltage: 4.2V
Q pin connection resistance value: 33kΩ
Fϕ pin connection resistance value: 18kΩ

RF AGC Control characteristics



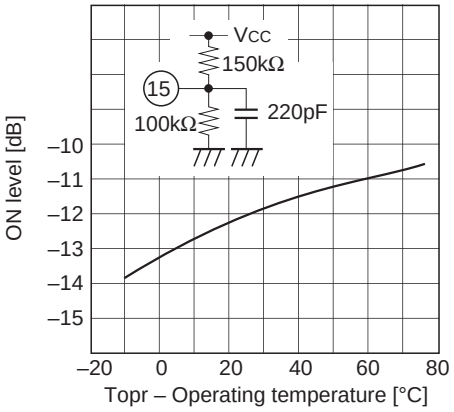
Conditions: Input: 25µm-wide head for NTSC, 5MHz
Output: Pin 10
Logic I
Pin 9 time constant: R: 150kΩ, C = 0.047µF

AGC output level vs. Operating temperature



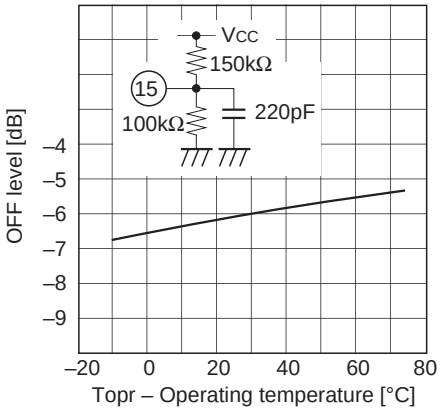
Conditions: Input: Pin 29, 5MHz, 170µVp-p
Output: Pin 10
Logic H

Dropout detection ON level vs. Operating temperature



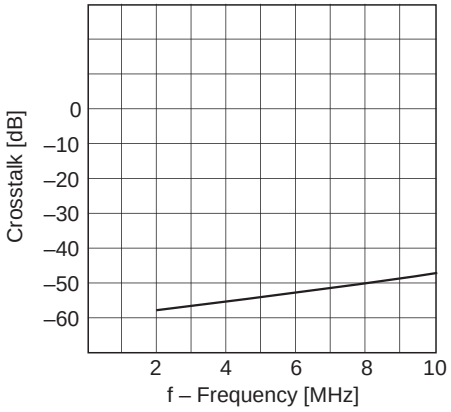
Conditions: Input: Pin 14
400mVp-p to 0dB at Pin 16
Logic H

Dropout detection OFF level vs. Operating temperature

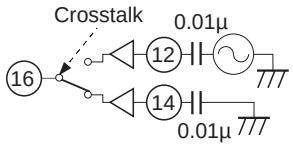


Conditions: Input: Pin 14
400mVp-p to 0dB at Pin 16
Logic H

RF SW Crosstalk (A → B) vs. Frequency

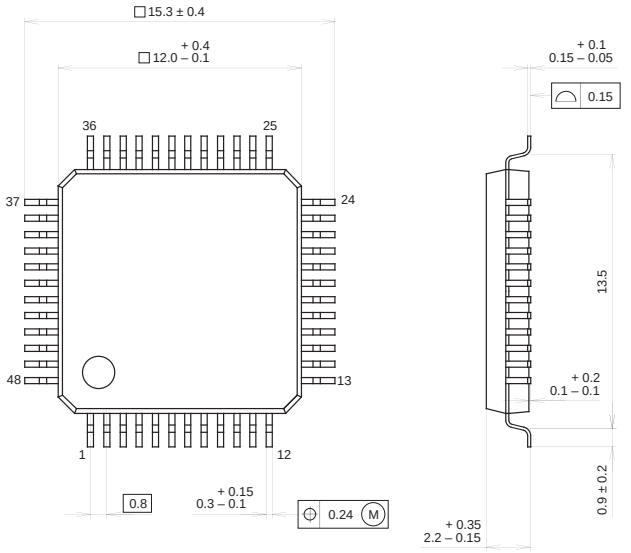


Conditions: Input: Pin 12, 100mVp-p
Output: Pin 16
Logic H
Pin 11 = 3V



Package Outline Unit: mm

CXA1202Q-Z 48PIN QFP (PLASTIC)



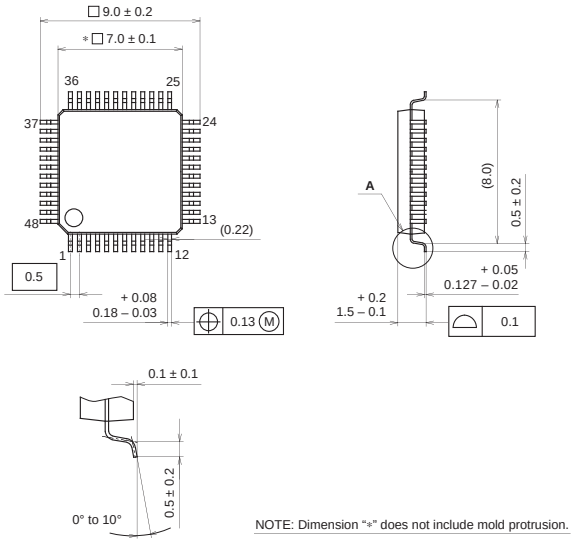
SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1202R 48PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g