VITESSE

VSC3138
Datasheet

4.25 Gbps 40 x 40 Asynchronous Crosspoint Switch

FEATURES

- 40 input by 40 output crosspoint switch
- 4.25 Gbps non-return to zero (NRZ) data bandwidth
- Input signal equalization (ISE) and output drive levels globally programmable, or on a per channel basis.
- On-board pseudorandom bit sequence (PRBS) generator and detector
- 2.5 V and 3.3 V complementary metal oxide semiconductor and TT L CMOS I/O
- Parallel and serial programming modes
- Differential current mode logic (CML) data output driver
- Software power-down for unused channels
- Secondary access port (SAP) for configuration and monitoring
- Boundary scan support for data I/O
- 125 MHz multi-mode program port
- Multicast and striping programming modes
- On-chip input and output terminations
- Single 2.5 V supply; 3.3 V option for control port
- 4.4 W typical power in nominal drive mode
- Integrated temperature sensor and alarm
- Ball grid array (BGA) packaging

APPLICATIONS

- Dense wavelength, division multiplexing (DWDM) switches
- Wavelength routers
- Storage area network (SAN) switch fabrics
- Packet-switching fabrics

GENERAL DESCRIPTION

The VSC3138 is a 40 × 40, asynchronous, crosspoint switch designed to carry broadband data streams in a variety of applications. Its fully non-blocking switch core is programmed using a multi-mode port interface that allows random access programming of each I/O port; each VSC3138 data output can be programmed to connect to any of its inputs. The signal path through the device is unregistered and fully asynchronous. This means that there are no restrictions on the phase, frequency, or signal pattern of any input.

A high degree of signal integrity is maintained throughout the device because each high-speed output is a fully differential, switched current driver with on-die terminations. Data inputs are terminated on-die using 100 Ω resistors between true and complement inputs with a common connection to an internal bias source that facilitates AC coupling to the switch inputs.

The VSC3138 provides a multi-mode programming interface that allows commands to be implemented as either serial data or multiplexed parallel data. Unused channels can be powered down to allow efficient use of the switch in applications that require only a subset of the available I/O channels. A Secondary Access Port (SAP) provides for asynchronous readback and configuration control even while the primary programming port is in use.

Block Diagrams

High-Level Functional Block Diagram

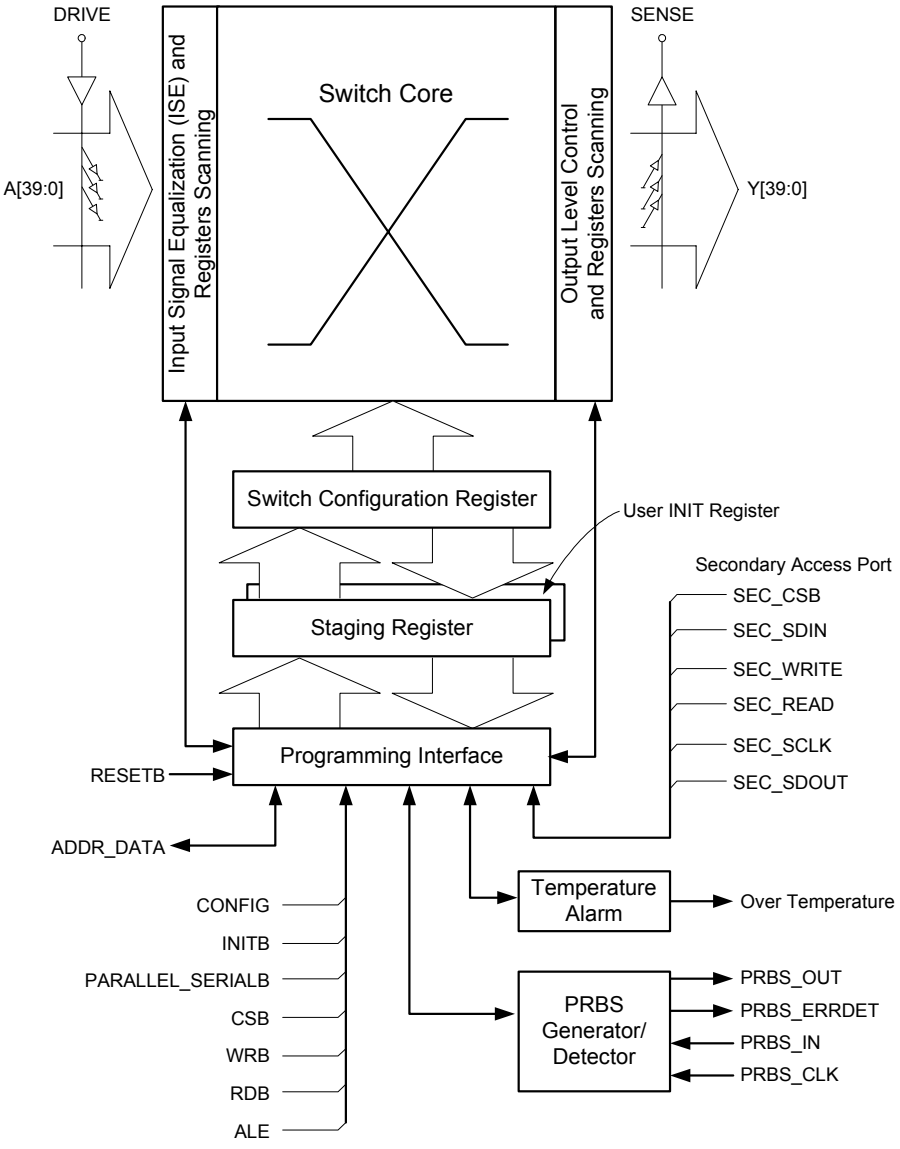


Figure 1. High-Level Functional Block Diagram

PRBS Generator and Detector Block Diagrams

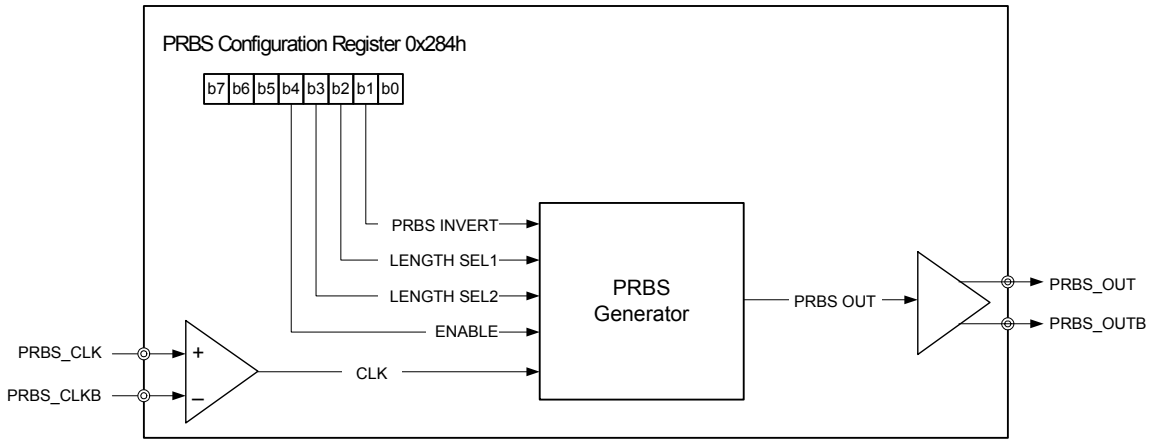


Figure 2. PRBS Generator

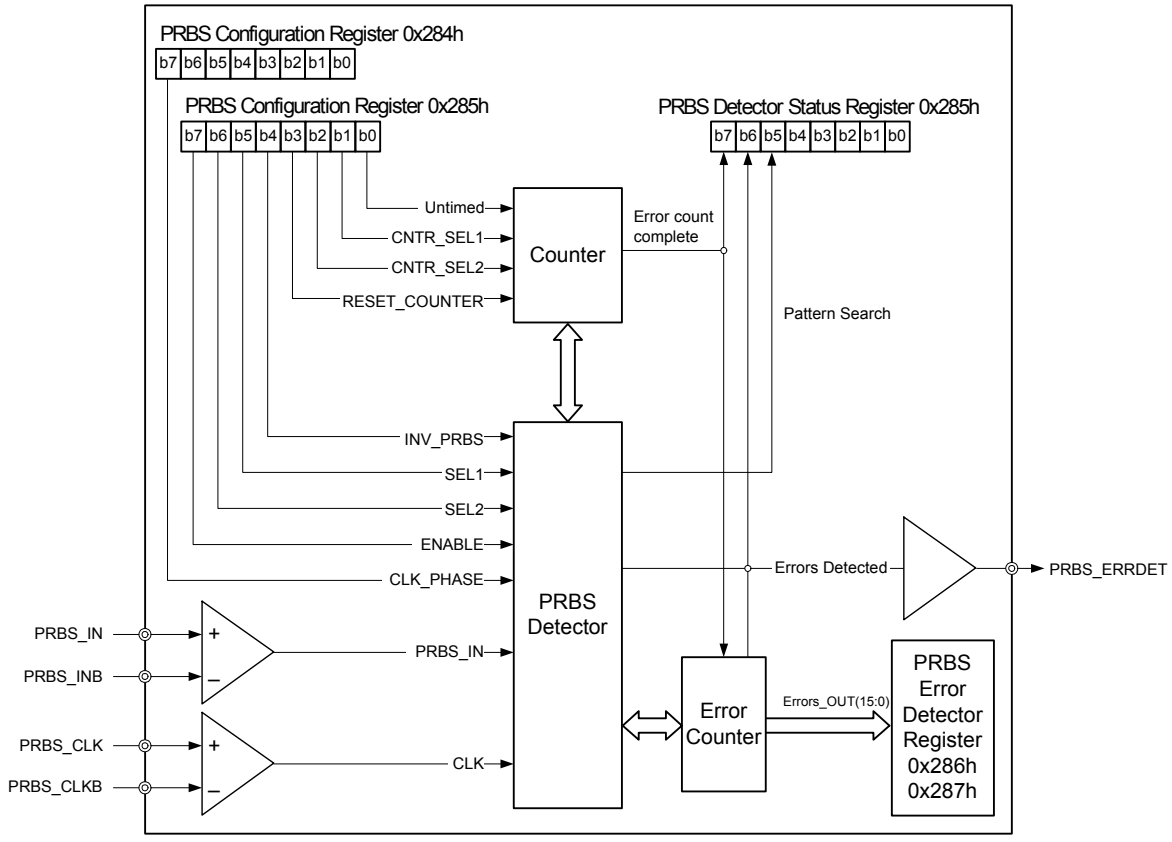


Figure 3. PRBS Error Detector

FUNCTIONAL DESCRIPTIONS

Power-On RESET

The VSC3138 device provides a power-on RESET function, which ensures that the matrix is fully disconnected and powered off. When the device is powered up, the switch draws additional power as each output is programmed. To avoid an accidental power down, care must be taken to keep power supply excursions above 2.2 VDC by providing adequate supply decoupling.

Software Power-Down

Unused outputs may be disabled using the software power-down feature. This is accomplished by programming each unused output with the power-down code (7FF'h). Programming a valid input address will reactivate the channel. Any changes in power programming should be executed only as part of an initialization sequence. This will guard against the effects of switching transients that might result from suddenly changing the power supply current.

CONFIG

The functionality of the CONFIG pin is duplicated in bit 1 of the Switch Control register (address 281'h). Writing to this bit has the same effect as driving the external pin to the same value. This bit is multiplexed with the external pin through logic and initializes to the state that uses the external pin. The states are therefore mutually exclusive. To pulse CONFIG using the register pin, write an active signal and then an inactive signal to register bit 1 of the Switch Control register. Holding the CONFIG pin "HIGH," or setting the CONFIG bit to a 1 causes the programming to be active upon asserting LOAD.

To prevent accidental reprogramming of the switch interconnects, the VSC3138 programming interface provides the option of disabling this feature through software. Setting the CONFIG Lockout bit [2] in the Switch Setup register (address 280'h) to a 1 will inhibit the use of both the external CONFIG pin and the CONFIG bit [1] in the Switch Control register from reprogramming the interconnects.

On power-up, the CONFIG Lockout bit [2] of the Switch Setup register is 0, and consequently, CONFIG is enabled.

Staging Register Readback

When the CONFIG control is used to accumulate a number of program steps and execute them simultaneously, it is possible to verify the pending switch programming prior to asserting the CONFIG control. Setting the Staging Register Readback bit [4] of the Switch Configuration register (address 281'h) to 1 and reading the programming information from the switch will return configuration information about the pending switch programming, rather than the current connections.

If CONFIG is set to a value of 1, all programming propagates directly to the switch matrix, and the information returned during a readback will be the same. In this case, the result is the same, regardless of the setting of the Staging Register Readback bit [4] of the Switch Configuration register.

DRIVE Input

The VSC3138 provides a DRIVE input that can be connected internally to any of the device's 40 data input connections. By connecting an external signal to the DRIVE input and then switching it to one of the 40 data inputs, a test signal can be placed on that input.

The signal from the DRIVE input is superimposed onto the data input path, rather than multiplexed between the DRIVE and data input signals. This is done so that the DRIVE input can be used to verify signal path integrity. For correct operation, the signal present on the selected input must be either in a neutral state or in a high-impedance state to allow the DRIVE input to have an effect on the data input under test.

The DRIVE input can also be used with the SENSE output and an external test generator/receiver to verify programmed signal path integrity.

The DRIVE input can be programmed to drive any or all of the 40 data inputs. Writing to the appropriate address either connects or disconnects a data input from the specified DRIVE input.

SENSE Output

The VSC3138 provides a SENSE output that can be used to monitor any one of the 40 data outputs. The SENSE output monitors the data output signal at the package pin, thereby facilitating true verification of the complete signal path through the switch.

The SENSE output can be used with the external monitoring circuit and DRIVE input to determine the presence of a signal on any output or to determine signal path integrity.

PRBS Control

The Pseudo-Random Bit Sequence (PRBS) Generator and Detector can generate and detect four NRZ patterns: 2^7-1, 2^9-1, 2^{10}-1, and 2^{11}-1. The main purpose of the PRBS Generator and Detector is to provide for switch diagnostics and signal tracing functions. The block diagram of the PRBS Generator is shown in Figure 2, page 3. The data rate of the Generator and Detector is determined by the external clock signal to a maximum of 400 Mbps. The PRBS output data is clocked on the rising edge of the clock. The PRBS function controls are located in the PRBS Generator Configuration register 0x284'h. The PRBS Generator is enabled by writing 1 to the PRBS Generator Enable bit [4] of the PRBS Generator Configuration register. Pattern length is selected using the PRBS Generator Pattern Length Selection bits [3] and [2] of the PRBS Generator Configuration register. Selecting 00 will generate pattern 2^7-1, 01=2^9-1, 10=2^{10}-1, 11=2^{11}-1. It is possible to invert the pattern by writing 1 into the PRBS Output Invert bit [1] of the PRBS Generator Configuration register.

The PRBS Detector uses the same clock as the PRBS Generator. The block diagram of the PRBS Detector is shown in Figure 3, page 3. The clock used by the Detector can be inverted by setting the PRBS Detector Clock Phase bit [0] of the PRBS Generator Configuration register to 1. It may be necessary to invert the Detector's clock in order to compensate for the phase difference between the PRBS data input and the clock. The PRBS Detector is enabled by writing a 1 to the PRBS Input Pattern bit [4] of the PRBS Detector Configuration register. The Detector pattern length is selected by the Detector Pattern Length Select bits [6] and [5] of the PRBS Detector Configuration register. Respectively; 00 represents pattern 2^7-1, 01=2^9-1, 10=2^{10}-1, 11=2^{11}-1. The error counter is not enabled until the pattern detector recognizes the pattern coming into the detector. It can take up to 30 clock cycles for the detector to recognize the pattern. Once the pattern has been detected, the PRBS Lock Detect bit [2] of the PRBS Error Status register (address 288'h) goes HIGH.

This enables the error counters in the Detector. The user has the option to choose the period over which errors are counted by setting the Error Counter Length bits [2:1] of the PRBS Detector Configuration register. Respectively, the Error Counter Length bits [2:1] represent the following count lengths: 00=2^7, 01=2^9, 10=2^{11}, 11=2^{15}.

When any one of the above periods is selected, the error count will continue until that period has elapsed. At that time the error counter will hold its count and the Period Indicator bit [1] of the PRBS Error Status register will be set to 1 to indicate the count period is complete. If the Error Flag bit [0] in the PRBS Error Status register is set to 1, it means that during the set time period, errors occurred and the error count is stored in the PRBS Error Count Read registers 0x267'h and 0x287'h. The error counter can be reset by strobing the Error Detect Reset bit [3] of the PRBS Detector Configuration register LOW. The Error Detect Reset bit [3] of the PRBS Detector Configuration register should be set HIGH while the detector is enabled.

Upon reset, the Fixed Error Count Period Indicator bit [1] and the Error Flag bit [0] of the PRBS Error Status register, and PRBS Error Count bits [7:0] of the PRBS Error Count Read register will be set to 0. The user can read errors without setting the error count period by setting the Error Detection Run Length bit [0] of the PRBS Detector Configuration register 0x285'h to 0. If the error count period is not set, and if the number of errors exceeds 65535 (counter overflow), the error counter will restart the count from 0. It is possible to invert the PRBS pattern that is entering into the pattern detector by setting the PRBS Input Pattern bit [4] of the PRBS Detector Configuration register 0x285'h to 1. This can be used to detect an inverted pattern from the PRBS Generator.

Figure 4 illustrates how the PRBS function can be connected to the switch core for signal path tracing to and from the switch. Refer to Figure 3 and use the following set of steps to effect a trace.

1. Connect PRBS_OUT and PRBS_OUTB to DRIVE0 and DRIVE0B, respectively.
2. Connect SENSE0 and SENSE0B to PRBS_IN and PRBS_INB, respectively.
3. Select channel to send the pattern through.
4. Generate the pattern with the PRBS generator.
5. Check the PRBS Detector for errors.

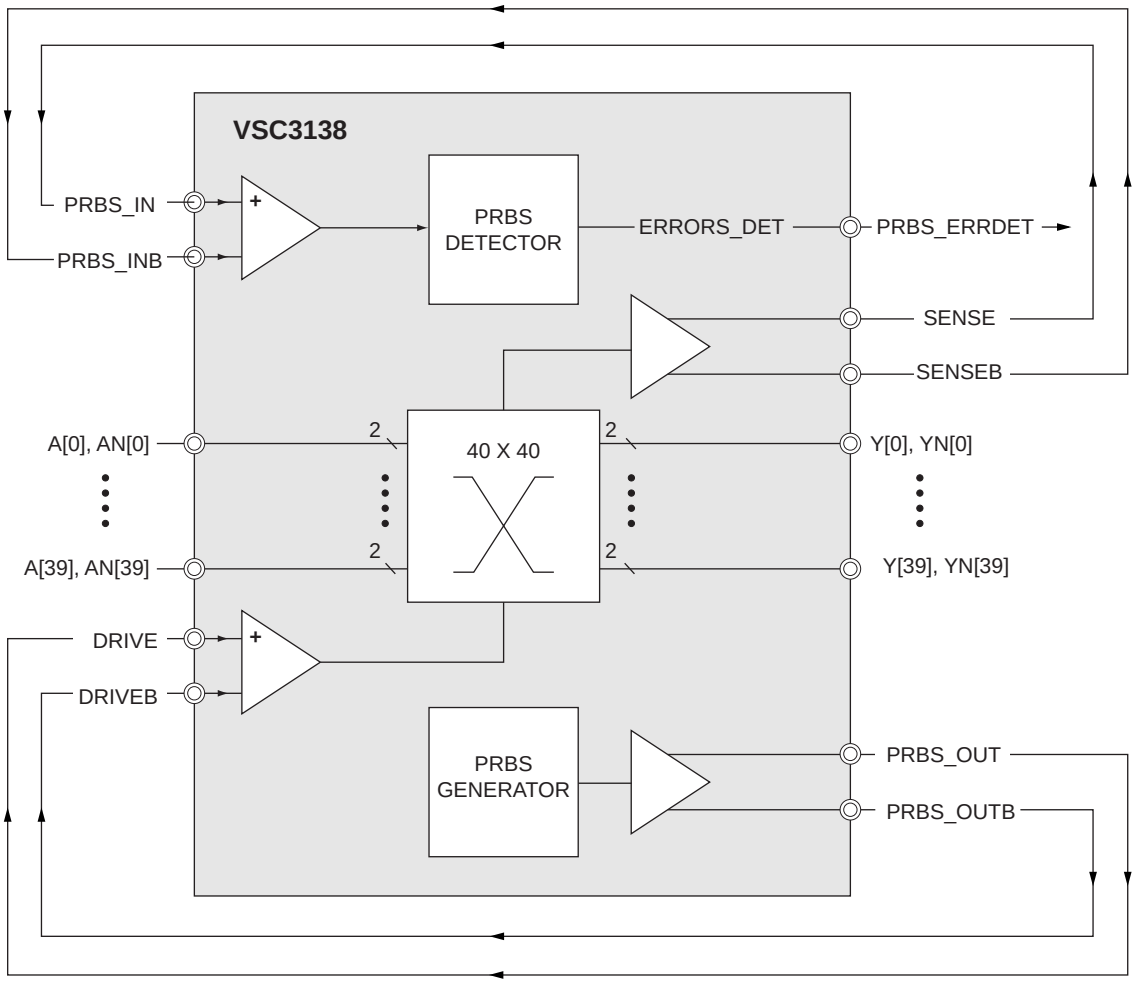


Figure 4. PRBS Connection Example

Input Configuration

The Global Input Channel Configuration register (address 283'h) and the Individual Input Configuration registers (addresses 600'h through 647'h) are used to configure the properties of the high-speed data inputs. (See Register 6 on page 19.) The two primary properties of these inputs are the Input Signal Equalization (ISE) and the Drive assignment. These properties can be set either globally or individually on a per input basis. When a property is set globally, it affects the setting for all inputs without exception. When a bit is set in the global registers, that state overrides any attempts to change the setting on an individual basis; it forces the global setting until the bit in the global register is cleared.

The Individual Input Configuration registers also provide a function that is not available in the global registers: the Scan register table. The Scan Input Value bit [8] of each Individual Input Configuration register (addressed 600'h through 647'h) reflects the latched state of the associated high-speed input at the time that the Input State Latch bit [0] of the Boundary Scan Control register (address 289'h) is set to 1.

Programmable Output Drive Levels

Two output drive levels can be set using the Output Level Control register. Output drive level can be controlled both globally and on a per-channel basis, through either the primary programming port or the secondary access port.

If both HIGH and LOW output bits are enabled simultaneously, LOW output level mode takes precedence.

Temperature Sensor/Alarm

The VSC3138 has circuitry that detects and flags temperatures exceeding a user-set range. The temperature range is set using Register 5, (address 28B'h). The device temperature alarm is asserted when the circuitry detects that the approximate die temperature meets or exceeds the maximum temperature in the user-selected range. There are 15 temperature range presets between 30ºC and 160ºC.

Boundary Scan Support

The VSC3138 includes registers that can be used to drive and sense the state of every pin of the high-speed data paths. These registers can be accessed through the programming port in serial mode, allowing the device to be fully tested with only five active pins.

The VSC3138 can sample the current state of the high-speed data inputs and can drive the high-speed data outputs with a static value.

To reduce power consumption, the input buffers for the boundary scan are powered off after reset. Before using the Scanning feature, these buffers must be activated by setting bit 1 of the Boundary Scan Control register to 1. Once the boundary scan input feature is no longer in use, this bit can reset to 0 to reduce power consumption. Sampling of the high-speed data inputs is triggered by writing a 1 to bit 0 of the Boundary Scan Control register. This bit is self-clearing, it does not need to be cleared prior to the next operation, and will always return a 0 when read. This operation will latch the current value of the high-speed inputs into bit 8 of each respective Input Channel Configuration register (600'h-647'h). These registers can be read one by one to determine the state of each input.

Access to the high-speed output scan support is through bits 2 and 3 of the Individual Output Level Control register (0x400-0x447). Setting bit 2 HIGH enables the Scan drive for the output associated with the selected Output Level Control register. Once enabled, bit 3 of the Individual Output Level Control register determines the value of the high-speed data output.

Multicast Mode

Multicast mode provides programming efficiency when a single input is to be connected to multiple outputs. By modifying the use of the ALE bit, it is possible to latch the DATA[10:0] value, and use it to represent the input value in subsequent programming steps.

To use multicast mode, ALE is held LOW while the input to be multicasted is written to the data word space of the Switch Array Connection register (or the multicast input storage register). ALE is then raised and held HIGH for the programming steps to follow. Connections to the saved input value are programmed solely with the rising edge of the WRB control signal. Figure 9, page 29 shows the programming sequence in parallel mode.

Normal programming is resumed by following the standard programming sequence. The input value is retained while ALE remains HIGH, but will change once ALE is brought LOW. The input value will also be cleared when information is read from the control interface, regardless of the value of ALE.

Multicast is also available in serial programming mode. ALE is held LOW during normal operation of the serial port. To initiate Multicast during serial programming, the first connection is made in the regular manner by first shifting in the 11 –bit address and then the 11–bit DATA. The WRB signal is raised HIGH to clock in the last bit and then negated at the next falling edge of SCLK. As the WRB signal is negated, the ALE control is raised, prior to the next rising edge of SCLK. As long as ALE is held HIGH, the input port that was designated in the data portion of the first programming sequence will be retained. To configure the outputs after the first connection, only the ADDR value is shifted in and written. The value will also be cleared during a read instruction regardless of the sense of ALE. Figure 9, page 29 shows the programming sequence in serial mode.

Address Striping Mode

Setting bit 5 of the Switch Configuration register enables striping mode, which allows groups of four inputs to be connected to four outputs with a single programming instruction.

The groups are predetermined, and have been selected according to the physical locations of their pins on the package and their numerical ordering. Because even and odd inputs and outputs are on opposite sides of the device, the groups consist of consecutively numbered even and odd inputs or outputs. The result is that the inputs and outputs are arranged in 10 stripes. Any of the 10 input stripes can be connected to any of the 10 output stripes.

Programming of the connections is accomplished by using only the nine MSBs of the ADDR_DATA bus. The two LSBs of each address or data word should be ignored. For example, the ADDR_DATA word 00000010000 specifies stripe 4, which includes inputs or outputs 16, 18, 20, and 22.

A complete list of the ADDR_DATA words is shown in the following table. In Striping mode, the only functionality that is striped is the switch core programming. All other functions such as readback, SENSE control, DRIVE control, Input Signal Equalization, and output drive level select are accessed and programmed individually.

Table 1. Address Striping Mode I/O Grouping

Group Number	Input/Output Designations	Group Address	Group Number	Input/Output Designations	Group Address
0	0, 2, 4, 6	00000000000	1	1, 3, 5, 7	00000000100
2	8, 10, 12, 14	00000010000	3	9, 11, 13, 15	00000010100
4	16, 18, 20, 22	00000100000	5	17, 19, 21, 23	00000100100
6	24, 26, 28, 30	00000110000	7	25, 27, 29, 31	00000110100
8	32, 34, 36, 38	00001000000	9	33, 35, 37, 39	00001000100

Secondary Access Port

The Secondary Access Port is an interface to the VSC3138 registers that operates concurrently with the primary programming interface. The main purpose of the Secondary Access Port is to facilitate monitoring and to maintain the operational state of the switch (verify and monitor port connections, die temperature, set drive and equalization levels) without interrupting the primary port programming operations. Having a secondary port means that the primary port can focus strictly on establishing connections while the Secondary Access Port performs all other operations “off-line.”

Before it can be used, the Secondary Access Port must be enabled by setting the Secondary Access Port Enable bit (7) in the Switch Configuration register (281’h). This bit allows the primary port controller to grant or deny access to the Secondary Access Port as required. For the Secondary Access Port to be enabled continuously, set the bit during initialization.

To protect the integrity of the primary port programming operations, there are two areas of the VSC3138 that cannot be written to by the Secondary Access Port. The Switch Connection registers at addresses 000'h to 08F'h, and the first two Configuration registers at addresses 280'h and 281'h (register 1 and register 2). These registers can be read by the Secondary Access Port, but can only be written to using the primary port.

The two interfaces share some logic, therefore care should be exercised when executing certain concurrent operations. In the event that coincident operations are in conflict, an arbitration circuit will grant control as appropriate. A conflict is defined as an overlap of an RDB or WRB assertion on the primary port with an assertion of the SEC_READ or SEC_WRITE signals on the Secondary Access Port. There is one exception to this rule, and that is when the primary port writes a switch connection. The Secondary Access Port cannot write switch connections, so there is never a conflict when the primary port writes a connection, regardless of the activity on the Secondary Access Port.

The Secondary Access Port provides an indication of one of its own read or write operations being overridden by a primary port operation. Upon completion of a successful write operation, the Secondary Access Port echoes back the address and data bits following the SEC_WRITE pulse. In the event of a failed write operation on the Secondary Access Port, the echoed data stream is fully or partially inverted. For a Secondary Access Port read, the 12^{th} bit (the bit after the last bit of valid data) indicates the status of the read. If the bit is a 1, then the previous 11 bits are correct. If the 12^{th} bit is a 0, the last read operation was interrupted by an operation on the primary port and the data is corrupt.

The primary port is only overridden when a read operation conflicts with a write operation on the Secondary Access Port. In this case, there is no indication of the failed read. In the event the primary port needs to perform uninterrupted read operations, the Secondary Access Port can be disabled.

Table 2 shows the decision matrix for conflicts between the primary port and the Secondary Access Port.

Table 2. Programming Port Conflict Resolution Decision Matrix

Conflict Combinations	Primary Port Write	Primary Port Read
Secondary Access Port Write	**Result:** Priority given to primary port. **Indication:** SEC_WRITE echoed on SEC_SDOUT will be fully or partially inverted. **Exception:** Primary port writes to connection metric do not conflict with Secondary Access Port writes.	**Result:** Priority given to Secondary Access Port. **Indication:** None
Secondary Port Read	**Result:** Priority given to primary port. **Indication:** 13^{th} bit of the SEC_SDOUT will be 0.	**Result:** Priority given to primary port. **Indication:** 13^{th} bit of the SEC_SDOUT will be 0.

Programming Interface

Power-down is enabled in software by programming individual unused outputs with a power-down code.

Core programming can be effected sequentially, port-by-port, or multiple program assignments can be queued and issued simultaneously using the CONFIG bit.

The VSC3138 is programmed using an 11–bit, multiplexed address/data (ADDR_DATA) bus in conjunction with the ALE, RDB, WRB, and CONFIG pins. Additionally, the CONFIG signal can be set via an internal control register to reduce the number of signals required to interface with the switch.

To lock in programming of switch connections, CONFIG can be disabled in software. Negating the appropriate bits in the Setup register blocks input on this control, preventing it from affecting the switch configuration.

The VSC3138 programming interface uses a multiplexed address and data bus. The ALE signal differentiates whether the binary word on the multiplexed bus is address or data information. The conventions listed in Table 3 are used in this document to describe the various terms used in the programming interface.

Table 3. VSC3138 Datasheet Programming Interface Conventions

Convention	Description
SIGNAL NAME	Active HIGH signal
SIGNAL_NAMEB	Active LOW signal
ADDR	Identifies OUTPUT channel to be programmed
DATA	Identifies INPUT channel to be programmed
1	A logic level high signal. Also denoted by 'HIGH'
0	A logic level low signal. Also denoted by 'LOW'

Register Use

All registers are accessed as described in the programming interface description for parallel and serial read and write functions. Each register has a corresponding address which, when written to with a data word, alters the functions defined for that register . For more information about registers, see "Registers," page 13. Table 2, page 10 provides an overview of all of the device registers, including detailed descriptions of the functions controlled in each register.

Note that all bits in all registers initialize to 0.

Parallel Mode—Write Operation

Parallel mode is enabled when PARALLEL_SERIALB=1. When ALE=1, the information on the ADDR_DATA bus is used as the address, and specifies the OUTPUT port that is being programmed in this write cycle. The falling edge of the ALE pin latches the address value. When ALE=0, the information on the ADDR_DATA bus is the INPUT port that is to be connected to the previously selected output port. The connection between the specified input and output is programmed into memory when WRB=1.

When CONFIG=1, all new programming data is transferred directly to the switch core and any new connections are configured as they are entered. When CONFIG=0, newly programmed connections are held in staging registers. Asserting CONFIG=1 transfers the data from the staging registers to the switch core independently of other control signals, so that any changes occur concurrently. CONFIG may be tied HIGH so that all programming takes effect sequentially as written, or it may be toggled HIGH and LOW to store multiple programming steps and activate them simultaneously.

Figure 6, page 27 shows the programming sequence for parallel mode write operations.

Parallel Mode—Read Operation

The VSC3138 supports parallel readback using the multiplexed bus to read programming information from the switch fabric. The falling edge of ALE will latch the address (OUTPUT) value of the connection to be read. The device will then drive the requested data onto the bus after the falling edge of RDB and will remain valid until RDB=1. Figure 6, page 27 shows the programming sequence for parallel mode read operations.

Serial Mode—Write Operation

Serial mode operation is enabled when PARALLEL_SERIALB=0. The ADDR_DATA0 pin becomes the serial data input (SDIN) pin and the ADDR_DATA1 pin becomes the serial clock (SCLK) pin, that is rising edge triggered. In addition, in serial mode, the sense of the WRB pin is inverted from parallel operation. That is, the pin should normally be set LOW and set HIGH to write the address and data information to the programming port. A serial word of the form [Output][Input] is shifted into the internal shift register (MSB-first), and the WRB pin is set HIGH, coincident with the last bit of the data word to indicate the last bit of a connection. This transfers the input identifier to the staging register of the addressed output. CONFIG is then asserted (1, asynchronously) to transfer one or more program commands to the switch core.

The programming information that is shifted in during the write cycle is repeated back to the SDOUT (ADDR_DATA2) pin, but delayed by 22 clock cycles. This allows for easy confirmation of the previous programming step. The output field is 11 bits long, representing the binary numerical identifier of the output to be programmed. The input field is also 11 bits long, representing the numerical identifier of the input that will be connected to the specified output. Figure 7, page 28 shows the programming sequence for serial mode write operations. During normal Serial port operations, the ALE pin must be held LOW. Setting ALE HIGH is used in Serial Multicast programming mode.

Serial Mode—Read Operation

During serial mode readback, the sense of the RDB pin is inverted from its operation during parallel mode. To read back information about a specific output connection, the address corresponding to the output of interest is shifted in while RDB is held LOW. RDB is set HIGH with the last bit of the output address, and is held HIGH for three clock cycles thereafter. The data begins to be shifted out on the SDOUT pin beginning four SCLK cycles after RDB was initially set HIGH, and for the following 11 clock cycles. Figure 7, page 28 shows the programming sequence for serial mode read operations.

REGISTERS

Table 4. VSC3138 Register Map

Register Name	ADDR [10:0]	DATA[10:0]										
		Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Switch Array Connection	0'h thru 47'h	Input Connections										
Switch Setup	280'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	CONFIG Register	Set to 0	CONFIG Disable	Set to 1
Switch Configuration	281'h	Not Used	Not Used	Not Used	Second-ary Access	Not Used	Address Striping	Staging Read-back	Set to 0	User INITB	Software CONFIG	Set to 1
DRIVE/SENSE Control	282'h	Not Used	Not Used	Not Used	Not Used	Global SENSE	Global DRIVE		Reserved. Do not write.			
SENSE Connection	300'h	Not Used	Drive Level	Power-On State	Address of Output Port Connection to SENSE							
Temperature Sensor	28B'h	Not Used	Not Used	Not Used	Current Chip Temperature				Alarm Threshold Temperature			
Global Input Channel Configuration	283'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Global Clear for Equalization		Global Set for Equalization	
Individual Input Channel Configuration	600'h thru 647'h	Not Used	Not Used	Scan State	Equalization State		Drive Input Connection State		Reserved. Do not write.			
PRBS Generator Configuration	284'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	PRBS Control	PRBS Pattern Length Control		Invert Pattern	Invert Clock
PRBS Receiver/Error Detector Configuration	285'h	Not Used	Not Used	Not Used	Receiver Control	Receiver Pattern Length Control		Input Pattern	Detector Reset	Detection Pattern Length Control		Error Run Length
PRBS Receiver/Error Count Read	286'h=LS Byte 287'h=MS Byte	Not Used	Not Used	Not Used	Error Count							
PRBS Error Status	288'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Pattern Search	Count Period	Error Flag
Global Output Level Control	28A'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Output Level HIGH	Output Level Nominal
Individual Output Level Control	400'h thru 447'h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Override Value	Output Override	Output Control	Output Status
Boundary Scan Control	289'h	Not Used	Not Used	Not Used	Reserved. Do not write.				Not Used	Not Used	Not Used	Latch Input
User Status	28C'h thru 28F'h	Storage Registers for transfer between Primary and Secondary Access Ports										

Switch Setup and Configuration

Register 1: Switch Setup

Reg Name:	Switch Setup	Reg. Address:	280'h
Reg Type:	R/W		
Description:	Configuration for various modes of operation.		

Bit	Bit Description	Reset Value	R/W
10-4	Not used	0000000	R
3	Input pin or software control for CONFIG 0 = Use input pin for CONFIG control 1 = Use register for CONFIG control	0	R/W
2	Always set to 0	0	R/W
1	CONFIG lockout 0 = CONFIG function enable 1 = CONFIG function disable (overrides bit 3)	0	R/W
0	Always set to '1'	0	R/W

Register 2: Switch Configuration

Reg Name:	Switch Configuration	Reg. Address:	281'h
Reg Type:	R/W		
Description:	Provides access to features and external pin functions via the programming interface. Writing updates the value and reading returns the current settings.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7	Secondary Access Port enable 0 = Disable Secondary Access Port 1 = Enable Secondary Access Port	0	R/W
6	Not Used	0	R
5	Address stripping mode select 0 = Standard address mode 1 = Address stripping mode	0	R/W
4	Staging readback select 0 = Read present switch configuration 1 = Read pending switch configuration	0	R/W
3	Always set to 0	0	R/W
2	User INITB programming 0 = Straight-through configuration upon INITB asserted LOW 1 = User programmed switch configuration upon INITB asserted LOW, stored using bit 3 of this register	0	R/W
1	Software programmable CONFIG 0 = CONFIG LOW when bit 3 of Switch Setup register, address 280'h, is 1 1 = CONFIG HIGH when bit 3 of Switch Setup register, address 280'h, is 1	0	R/W
0	Always set to 1	0	R/W

Switch Connection Register

Note that the address bit ADDR[3] is always zero in the following two tables.

Table 5. Address Map for Input Addresses

Input Channel	Input Address ADDR[10:0]	Input Channel	Input Address ADDR[10:0]	Input Channel	Input Address ADDR[10:0]
A0	0	A13	10101	A26	110010
A1	1	A14	10110	A27	110011
A2	10	A15	10111	A28	110100
A3	11	A16	100000	A29	110101
A4	100	A17	100001	A30	110110
A5	101	A18	100010	A31	110111
A6	110	A19	100011	A32	1000000
A7	111	A20	100100	A33	1000001
A8	10000	A21	100101	A34	1000010
A9	10001	A22	100010	A35	1000011
A10	10010	A23	100111	A36	1000100
A11	10011	A24	110000	A37	1000101
A12	10100	A25	110001	A38	1000110
				A39	1000111

Table 6. Address Map for Output Addresses

Output Channel	Output Address ADDR[10:0]	Output Channel	Output Address ADDR[10:0]	Output Channel	Output Address ADDR[10:0]
Y0	0	Y13	10101	Y26	110010
Y1	1	Y14	10110	Y27	110011
Y2	10	Y15	10111	Y28	110100
Y3	11	Y16	100000	Y29	110101
Y4	100	Y17	100001	Y30	110110
Y5	101	Y18	100010	Y31	110111
Y6	110	Y19	100011	Y32	1000000
Y7	111	Y20	100100	Y33	1000001
Y8	10000	Y21	100101	Y34	1000010
Y9	10001	Y22	100010	Y35	1000011
Y10	10010	Y23	100111	Y36	1000100
Y11	10011	Y24	110000	Y37	1000101
Y12	10100	Y25	110001	Y38	1000110
				Y39	1000111

Table 7. Switch Array Connection Examples

Output ADDR[10:0]	Input ADDR[10:0]	Description
0'b	0'b	Program output Y0 to connect to A0
. . .	. . .	. . .
0'b	111'b	Program output Y0 to connect to A7
0'b	10000'b	Program output Y0 to connect to A8
. . .	. . .	. . .
0'b	10111'b	Program output Y0 to connect to A15
0'b	100000'b	Program output Y0 to connect to A16
. . .	. . .	. . .
0'b	100111'b	Program output Y0 to connect to A23
0'b	110000'b	Program output Y0 to connect to A24
. . .	. . .	. . .
0'b	110111'b	Program output Y0 to connect to A31
0'b	1000000'b	Program output Y0 to connect to A32
. . .	. . .	. . .
0'b	1000111'b	Program output Y0 to connect to A39
1'b	0'b	Program output Y1 to connect to A0
. . .	. . .	. . .
1'b	111'b	Program output Y1 to connect to A7
1'b	10000'b	Program output Y1 to connect to A8
. . .	. . .	. . .
1'b	10111'b	Program output Y1 to connect to A15
1'b	100000'b	Program output Y1 to connect to A16
. . .	. . .	. . .
1'b	100111'b	Program output Y1 to connect to A23
1'b	110000'b	Program output Y1 to connect to A24
. . .	. . .	. . .
1'b	110111'b	Program output Y1 to connect to A31
1'b	1000000'b	Program output Y1 to connect to A32
1000111'b	0'b	Program output Y39 to connect to A0
. . .	. . .	. . .
1000111'b	111'b	Program output Y39 to connect to A7
1000111'b	10000'b	Program output Y39 to connect to A8
. . .	. . .	. . .
1000111'b	10111'b	Program output Y39 to connect to A15
1000111'b	0'b	Program output Y39 to connect to A0
. . .	. . .	. . .
1000111'b	100111'b	Program output Y39 to connect to A23
1000111'b	110000'b	Program output Y39 to connect to A24
. . .	. . .	. . .
1000111'b	110111'b	Program output Y39 to connect to A31

Table 7. Switch Array Connection Examples *(continued)*

Output ADDR[10:0]	Input ADDR[10:0]	Description
1000111'b	1000000'b	Program output Y39 to connect to A32
. . .	. . .	. . .
1000111'b	10000111'b	Program output Y39 to connect to A39

Drive/Sense Control

Register 3: DRIVE/SENSE Control

Reg Name:	DRIVE/SENSE Control	**Reg. Address:**	282'h
Reg Type:	R/W		
Description:	Controls the DRIVE input and SENSE output functions.		

Bit	Bit Description	Reset Value	R/W
10-7	Not used	0000	R
6	Global SENSE control 0 = No effect on existing state of SENSE control signals 1 = Clears SENSE connection and turns off output buffer	0	R/W
4-5	Global DRIVE control 00 = Maintains current connection state 01 = Do not use 10 = Clears DRIVE connection state 11 = Maintains current connection state	00	R/W
3-0	Reserved. Do not write.	0'h	Read Only

Register 4: SENSE Connection

Reg Name:	SENSE	**Reg. Address:**	300'h
Reg Type:	R/W		
Description:	Controls the operating mode of SENSE output bit.		

Bit	Bit Description	Reset Value	R/W
10	Not used	0	R
9	Drive level for SENSE output. Always returns '1' when bit 8 = '1'. 0 = nominal drive mode 1 = high output level	0	R/W
8	Power-on state of SENSE output 0 = on 1 = off	0	R
7-0	Address of output port connection to SENSE (for Y0 to Y39). Returns FF'h when SENSE is powered off.	FF'h	R/W

Register 5: Temperature Sensor

Reg Name:	Temperature Sensor	**Reg. Address:**	28B'h
Reg Type:	R/W		
Description:	User-controllable on-board temperature sensing function.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7-4	Approximate die temperature (not a calibrated value) 0000 = 23ºC to 41ºC 0001 = 33ºC to 50ºC 0010 = 42ºC to 60ºC 0011 = 52ºC to 69ºC 0100 = 61ºC to 78ºC 0101 = 70ºC to 88ºC 0110 = 80ºC to 97ºC 0111 = 89ºC to 106ºC 1000 = 98ºC to 116ºC 1001 = 108ºC to 125ºC 1010 = 117ºC to 135ºC 1011 = 127ºC to 144ºC 1100 = 136ºC to 153ºC 1101 = 145ºC to 163ºC 1110 = 155ºC to 172ºC 1111 = 164ºC to 181ºC	00000	R
3-0	Temperature alarm threshold 0000 = 23ºC to 41ºC 0001 = 33ºC to 50ºC 0010 = 42ºC to 60ºC 0011 = 52ºC to 69ºC 0100 = 61ºC to 78ºC 0101 = 70ºC to 88ºC 0110 = 80ºC to 97ºC 0111 = 89ºC to 106ºC 1000 = 98ºC to 116ºC 1001 = 108ºC to 125ºC 1010 = 117ºC to 135ºC 1011 = 127ºC to 144ºC 1100 = 136ºC to 153ºC 1101 = 145ºC to 163ºC 1110 = 155ºC to 172ºC 1111 = 164ºC to 181ºC	00	R/W

Register 6: Global Input Channel Configuration

Reg Name:	Global Input Channel Configuration	**Reg. Address:**	283'h
Reg Type:	R/W		
Description:	Global input channel configuration control.		

Bit	Bit Description	Reset Value	R/W
10-4	Not Used	0000000	R
3-2	Global Clear for ISE Setting 00 = bits 6 and 7 of all Individual Input Configuration registers are writeable 01 = bit 6 of all Individual Input Configuration registers forced to 0 10 = bit 7 of all Individual Input Configuration registers forced to 0 11 = bits 6 and 7 of all Individual Input Configuration registers forced to 0	00	R/W
1-0	Global Clear for ISE Setting 00 = bits 6 and 7 of all Individual Input Configuration registers are writeable 01 = bit 6 of all Individual Input Configuration registers forced to 1 10 = bit 7 of all Individual Input Configuration registers forced to 1 11 = bits 6 and 7 of all Individual Input Configuration registers forced to 1	00	R/W

Register 7: Individual Input Channel Configuration

Reg Name:	Individual Input Channel Configuration	**Reg. Address:**	600'h – 607'h = A0 – A7
Reg Type:	R/W		610'h – 617'h = A8 – A15
Description:	Individual input channel configuration control.		620'h – 627'h = A16 – A23
			630'h – 637'h = A24 – A31
			640'h – 647'h = A32 – A39

Bit	Bit Description	Reset Value	R/W
10-9	Not used	00	R
8	A[0:71] scan register table (values latched using register 14, bit 0)	0	R
7-6	ISE Setting 00 = ISE disabled 01 = low ISE 10 = medium ISE 11 = high ISE	00	R/W
5-4	DRIVE Input Connection State 00 = Maintains current connection state 01 = Do not use 10 = Removes DRIVE connection to input 11 = Maintains current connection state	00	R/W
3-0	Reserved. Do not write.	0'h	R

Register 8: PRBS Generator Configuration

Reg Name:	PRBS Generator and Detector Configuration	**Reg. Address:**	284'h
Reg Type:	R/W		
Description:	Configures the operating mode of the on-board PRBS Generator and Detector.		

Bit	Bit Description	Reset Value	R/W
10-5	Not used	000000	R
4	PRBS Generator enable 0 = Disable PRBS Generator 1 = Enable PRBS Generator	0	R/W
3-2	PRBS Generator pattern length selection 11 = 2^{11}-1 10 = 2^{10}-1 01 = 2^{9}-1 00 = 2^{7}-1	00	R/W
1	PRBS output pattern 0 = Non-inverted pattern 1 = Inverted pattern	0	R/W
0	PRBS Error Detector clock phase selection (to correct for timing skews) 0 = Non-inverted clock phase 1 = Inverted clock phase	0	R/W

Register 9: PRBS Error Status

Reg Name:	PRBS Error Status	**Reg. Address:**	288'h
Reg Type:	R/W		
Description:	Report error status from the on-board PRBS Detector.		

Bit	Bit Description	Reset Value	R/W
10-3	Not used	00000000	R
2	Error Detector Search Status 0 = Error Detector has not locked onto a valid PRBS pattern 1 = PRBS pattern detected. Detector is counting errors	0	R
1	Error Count Period Indicator (not valid if register 10, bit 0 = 0) 0 = Fixed error count period has not yet completed 1 = Fixed error count period has completed	0	R
0	Error flag bit (resets when read) 0 = No errors detected since last reset 1 = Errors detected since last reset	0	R

Register 10: PRBS Receiver/Error Detector Configuration

Reg Name:	PRBS Receiver and Error Detector Configuration	**Reg. Address:**	285'h
Reg Type:	R/W		
Description:	Configures the operating mode of the on-board PRBS receiver and error detector.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7	PRBS Receiver enable 0 = Disable PRBS 1 = Enable PRBS Detector	0	R/W
6-5	Select Receiver and Error Detector Pattern Length (to match PRBS Generator) 11 = 2^{11}-1 10 = 2^{10}-1 01 = 2^{9}-1 00 = 2^{7}-1	00	R/W
4	PRBS input pattern 0 = Non-inverted PRBS input 1 = Inverted PRBS input	0	R/W
3	Error detector reset 0 = Reset error count 1 = Enable error count	0	R/W
2-1	Error counter length control (dependent on bit 0) 11 = 2^{15}-1 10 = 2^{11}-1 01 = 2^{9}-1 00 = 2^{7}-1	00	R/W
0	Error detection run length 0 = No stop length, free running error detection 1 = Run and stop at count length	0	R/W

Register 11: PRBS Error Count Read

Reg Name:	PRBS Error Count Read	**Reg. Address:**	286'h = LSB Reg
Reg Type:	R/W		287'h = MSB Reg
Description:	Provides Error Count report.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7-0	Number of errors since start of count or last reset	00'h	R

Register 12: Global Output Level Control

Reg Name:	Global Output Level Control	**Reg. Address:**	28A'h
Reg Type:	R/W		
Description:	Enables global output high drive and nominal drive mode.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7-4	Internal use only	0000	R
3-2	Not used	00	R
1-0	00 = No change 10 = Force all outputs to high drive mode 01 = Force all outputs to nominal drive mode 11 = Not allowed	00	R/W

Register 13: Individual Output Level Control

Reg Name:	Individual Output Level Control	**Reg. Address:**	400'h – 407'h = Y0 – Y7
Reg Type:	R/W		410'h – 417'h = Y8 – Y15
Description:	Enables individual output high drive and nominal drive mode.		420'h – 427'h = Y16 – Y23
			430'h – 437'h = Y24 – Y31
			440'h – 447'h = Y32 – Y39

Bit	Bit Description	Reset Value	R/W
10-9	Internal use only	00	R
8-4	Not used	00000	R
3	Override output value 0 = Force the addressed Y output value to 0 when bit 2 is HIGH 1 = Force the addressed Y output value to 1 when bit 2 is HIGH	0	R/W
2	Output override mode (boundary scan support) control 0 = Disable output override mode 1 = Enable output override mode. Y output forced to value stored in bit 3 of this register	0	R/W
1	Individual output level control 0 = Set output level nominal 1 = Set output level HIGH	0	R/W
0	Individual output status 0 = Y output OFF 1 = Y output ON	0	R

Register 14: Boundary Scan Control

Reg Name:	Boundary Scan Control	**Reg. Address:**	289'h
Reg Type:	R/W		
Description:	Controls the operating mode of the Boundary Scan function.		

Bit	Bit Description	Reset Value	R/W
10-8	Not used	000	R
7-4	Always set to 0	0	R/W
3-2	Not used	00	R
1	Boundary scan input enable 0 = Boundary scan inputs disabled 1 = Boundary scan inputs enabled	0	R/W
0	Input state latch 0 = No change 1 = Triggers latch of input state (A0 through A39). Self-clearing.	0	W

Register 15: User Status

Reg Name:	User Status	**Reg. Address:**	28C'h through 28F'h
Reg Type:	R/W		
Description:	Enables information exchange between primary and secondary ports and display user status.		

Bit	Bit Description	Reset Value	R/W
7-0	Registers for user status or information transfer between primary and secondary ports.	00000000	R/W

ELECTRICAL SPECIFICATIONS

AC Characteristics

Unless stated otherwise, all data is assumed to be over recommended operating conditions.

Table 8. High-Speed Data Inputs (A, AN)

Symbol	Parameter	Typical	Maximum	Unit	Condition
DR_A	Serial NRZ input data rate		4.25	Gbps	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled)
t_{PD_AY}	Propagation delay from any A input to any Y output	700	900	ps	
t_{SKEW}	Output channel-to-channel delay skew		40	ps	Within striping group
t_{R_A} , t_{F_A}	Serial data input rise and fall times	100	150	ps	20% to 80%. See Figure 5, page 25.

Table 9. High-Speed Data Outputs (Y, YN)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
DR_Y	Serial NRZ output data rate			4.25	Gbps	Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled)
t_{J_rms}	Serial output data added delay Jitter: rms(1)			10	ps	With 50 Ω to V_{CC}.
t_{Jp-p}	Serial output data added delay Jitter: peak-peak(1)			40	ps	With 50 Ω to V_{CC}.
t_{R_Y} , t_{F_Y}	Serial output data rise and fall times		80	120	ps	20% to 80%. See Figure 5, page 25. With 50 Ω to V_{CC}.
DC_Y	Serial data output duty cycle	40	50	60	%	Only relevant with 101010 input data patterns. With 50 Ω to V_{CC}.

1. Broadband (unfiltered) deterministic jitter added to a jitter free input: 2^{23} -1 PRBS data pattern.

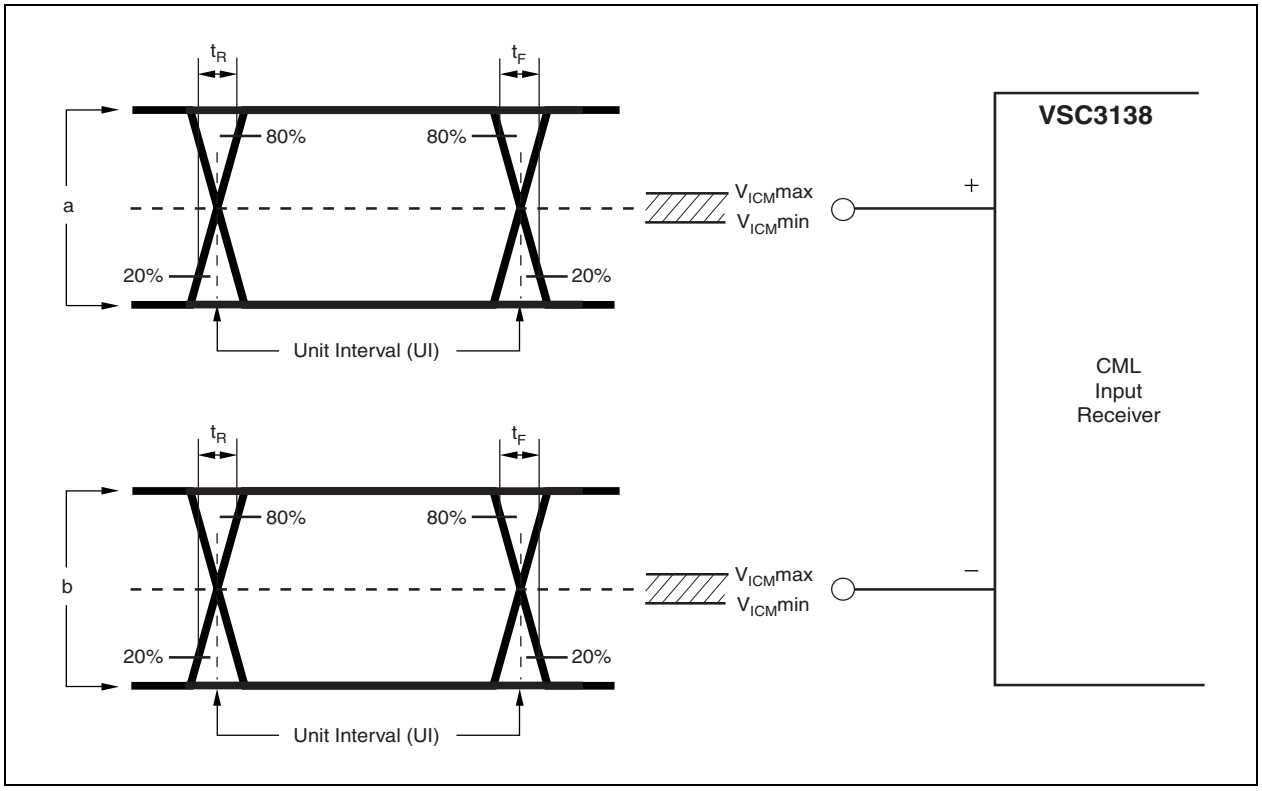


Figure 5. Parametric Measurement Setup

If used differentially (true and complement), each signal should meet the requirements for $a = b = V_{A\_DE} / 2$. For more information, see Table 11. If used single-ended (true only), the value required is $a = V_{A\_DE}$.

Table 10. Program Interface

Symbol	Parameter	Minimum	Maximum	Unit
t_{sPS}	Setup time from PARALLEL_SERIALB selection to CSB falling edge	2		ns
t_{sCS}	Setup time from falling edge of CSB to falling edge of ALE	3		ns
t_{sALE}	Setup time from ADDR[10:0] stable to falling edge of ALE	3		ns
t_{hALE}	Hold time for ADDR[10:0] after falling edge ALE	3		ns
t_{pwALE}	High and low pulse width for ALE	4		ns
t_{pwlRD}	Pulse width for RDB low	22		ns
t_{pwhRD}	Pulse width for RDB high	8		ns
t_{hRD}	Hold time for DATA[10:0] after rising edge of RDB	3		ns
t_{pwlWR}	Pulse width low of WRB	4		ns
t_{sWR}	Setup time from DATA[10:0] stable to rising edge of WRB	2.3		ns
t_{hWR}	Hold time for DATA[10:0] after rising edge of WRB	4.7		ns
t_{pwhWR}	Pulse width high of WRB	8		ns
t_{pwCFG}	High and low pulse width for CONFIG	8		ns

Table 10. Program Interface *(continued)*

Symbol	Parameter	Minimum	Maximum	Unit
t_{sCFG}	Setup time between rising edge of WRB and rising edge of CONFIG (if not permanently tied HIGH)	4.5		ns
t_{hCFG}	Hold time for CONFIG before rising edge of CSB	8		ns
t_{hCSB}	Hold time for CSB after rising edge of RDB	8		ns
t_{sLOAD}	Time for LOAD stable before rising edge of SCLK	5		ns
t_{hLOAD}	Time to hold LOAD stable after rising edge of SCLK	5		ns
$t_{pwhLOAD}$	Time to hold LOAD stable after rising edge of SCLK	14	18	ns
t_{sSDIN}	Time for SDIN stable before rising edge of SCLK	5		ns
t_{hSDIN}	Time to hold SDIN stable after rising edge of SCLK	5		ns
$t_{sSERIALB}$	Time for PARALLEL_SERIALB stable before falling edge of CSB	5		ns
t_{sRDB}	Time for RDB stable before rising edge of SCLK	5		ns
t_{hRDB}	Time to hold RDB stable after rising edge of SCLK	26		ns
t_{dSDOUT}	Delay for SDOUT valid after rising edge of SCLK		10	ns
t_{hSDOUT}	Time for SDOUT valid after rising edge of SCLK	2		ns
$t_{perSCLK}$	Period of SCLK	14		ns
t_{DRVN}	Time required for ADDR_DATA bus to change direction	3		ns
t_{VALID}	Time until data valid after falling RDB	20		ns
$t_{sSecSDIN}$	Setup time for SEC_SDIN to rising edge of SEC_SCLK	20		ns
$t_{hSecSDIN}$	Hold time for SEC_SDIN from rising edge of SEC_SCLK	25		ns
$t_{sSecWrite}$	Setup time for SEC_WRITE rising edge to rising edge of SEC_SCLK	20		ns
$t_{hSecWrite}$	Hold time for SEC_WRITE from rising edge of SEC_SCLK	34		ns
$t_{wSecWrite}$	Pulse width of SEC_WRITE	54	73	ns
$t_{sSecRead}$	Setup time for SEC_READ rising edge to rising edge of SEC_SCLK	20		ns
$t_{hSecRead}$	Hold time for SEC_READ from rising edge of SEC_SCLK	34	40	ns
$t_{wSecRead}$	Pulse width of SEC_READ	54	73	ns
$t_{pSecSDOUT}$	Delay to data valid on SEC_SDOUT from rising edge of SEC_SCLK	12	62[1]	ns
$t_{perSecSCLK}$	Minimum period for SEC_SCLK	67		ns
t_{pHI-Z}	Delay time from SEC_CSB to SEC_SDOUT active/inactive		20	ns
$t_{sSecCSB}$	Setup time from rising edge of SEC_CSB to SEC_SCLK in A10	20		ns
$t_{hSecCSB}$	Hold time for SEC_CSB from rising edge of SEC_SCLK in SEC_READ	67		ns

1. Except for $t_{dSecSDOUT}$, the maximum timing values are dependent on the period of SEC_SCLK. For every 2 ns added to the period of SEC_SCLK beyond 67 ns, add 1 ns to the maximum values provided.

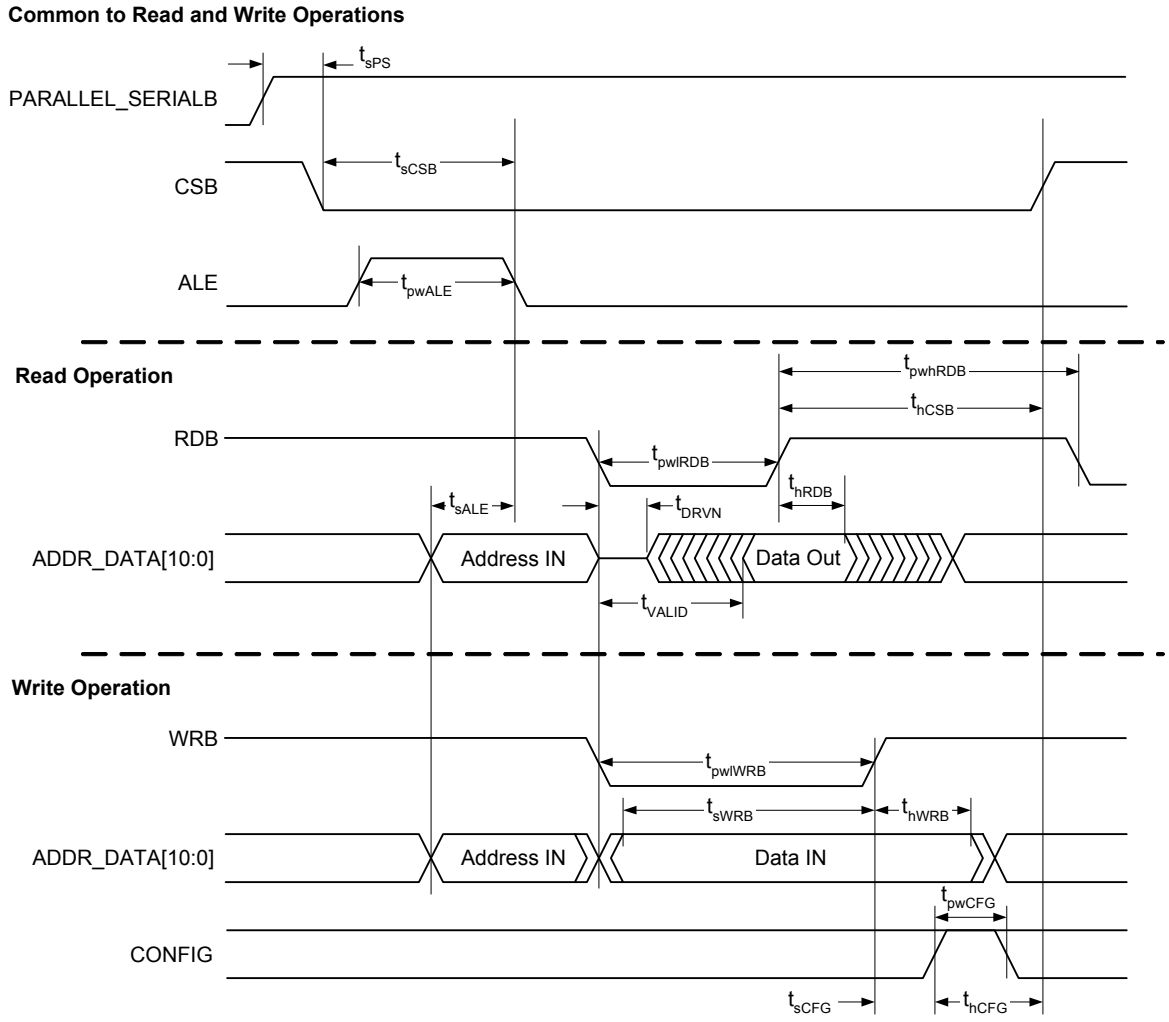


Figure 6. Parallel Mode Timing

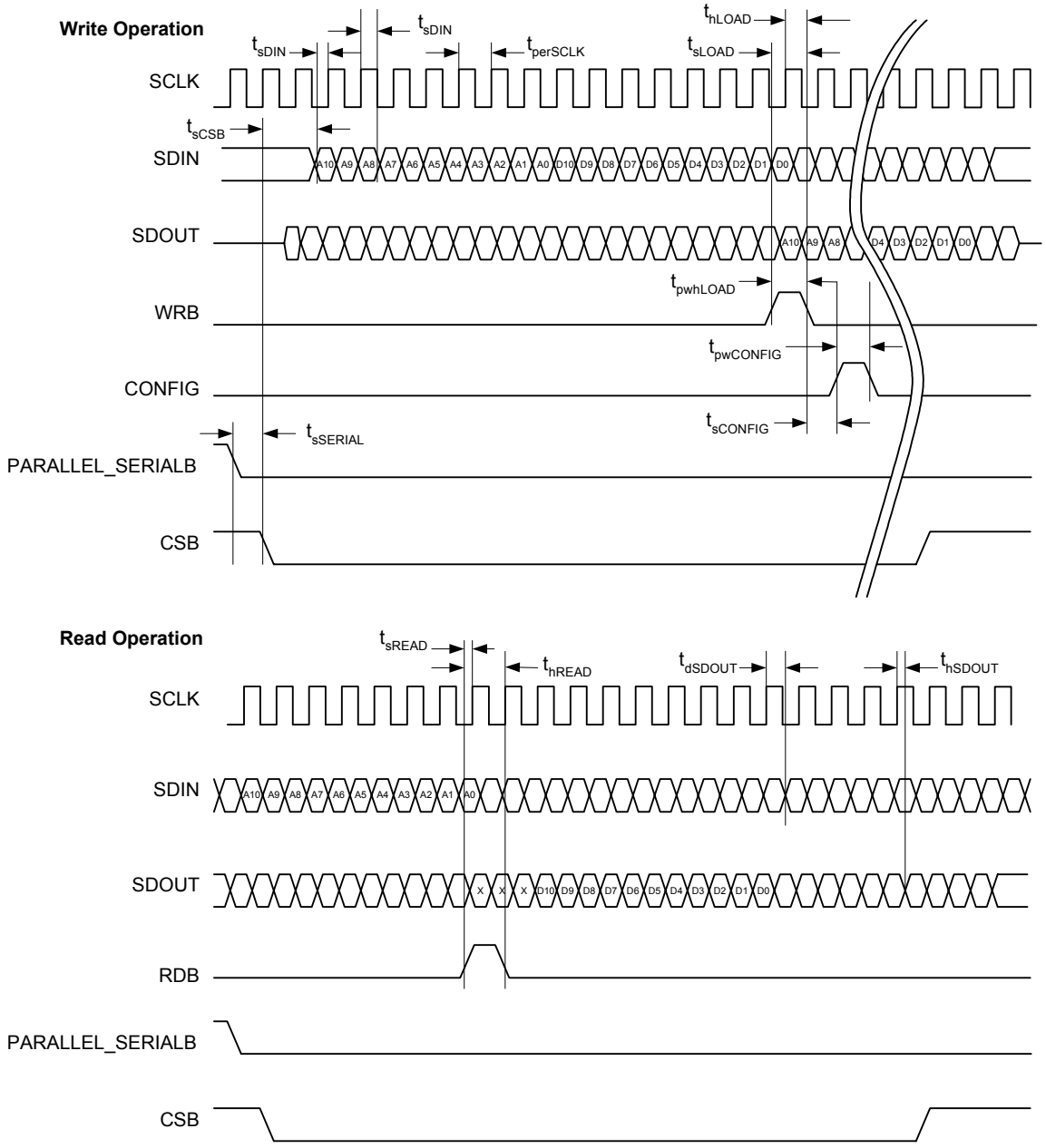


Figure 7. Serial Mode Timing

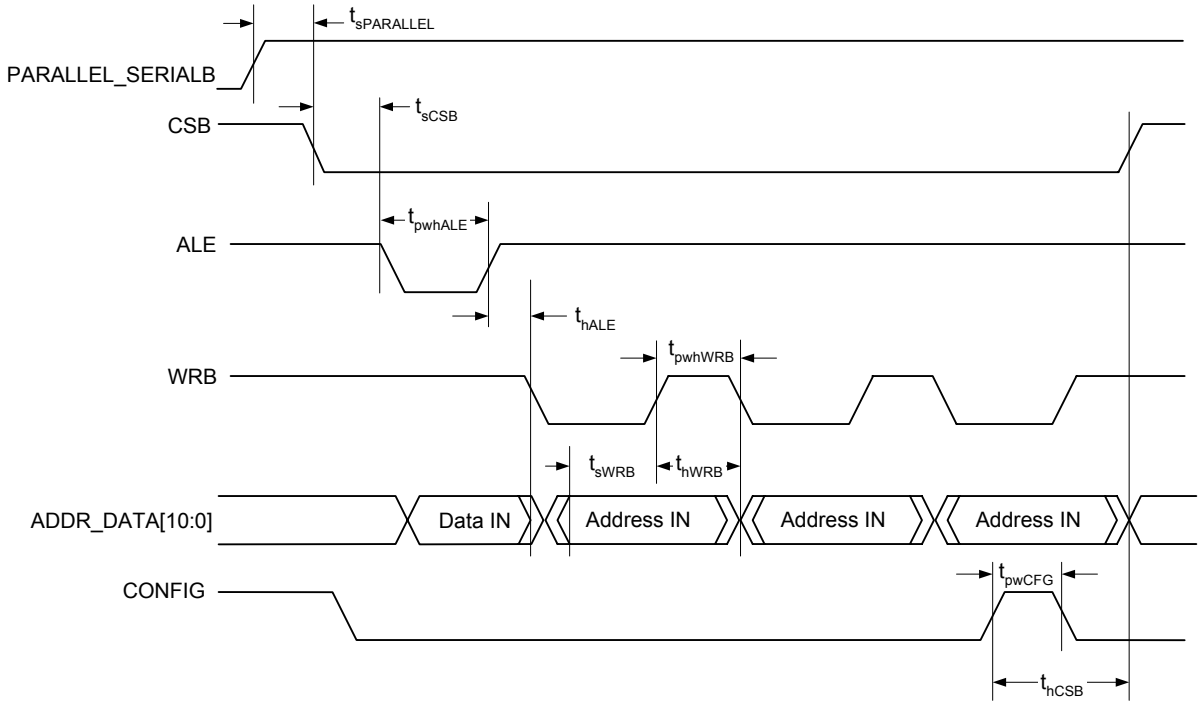


Figure 8. Parallel Multicast Mode

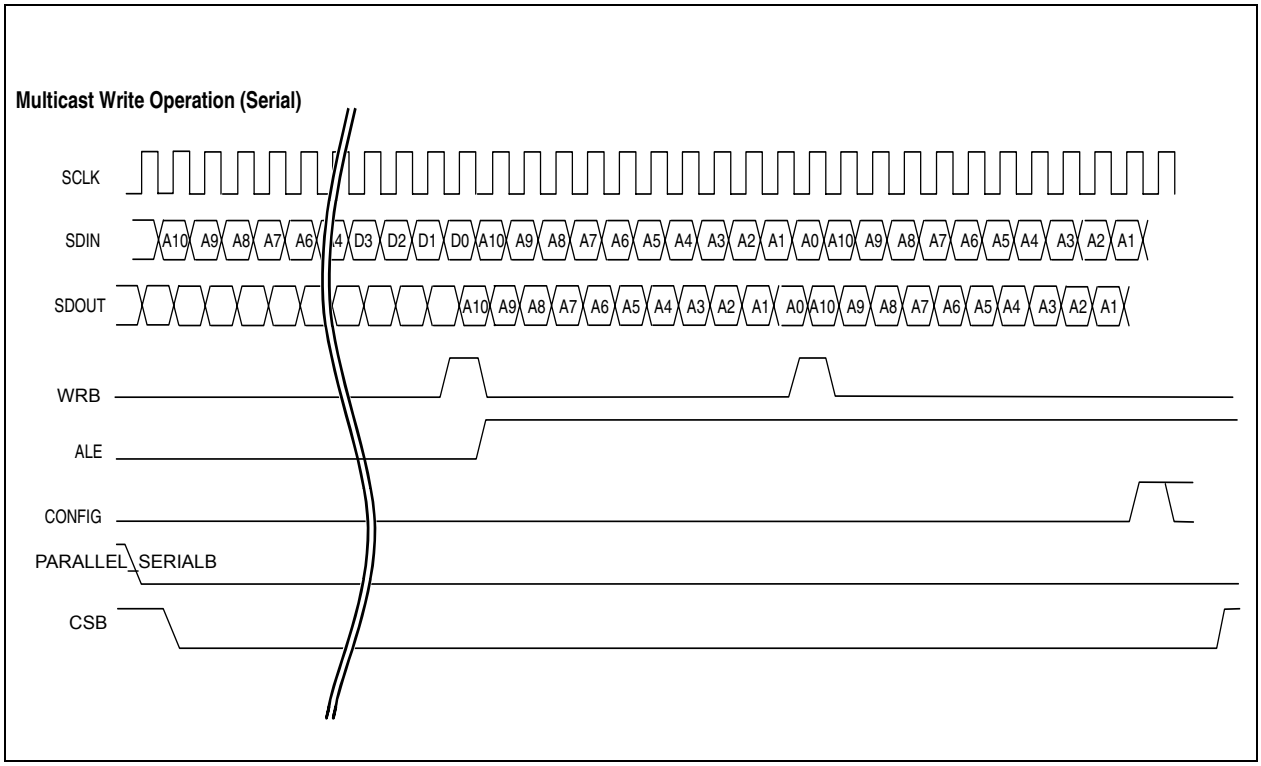


Figure 9. Serial Multicast Mode

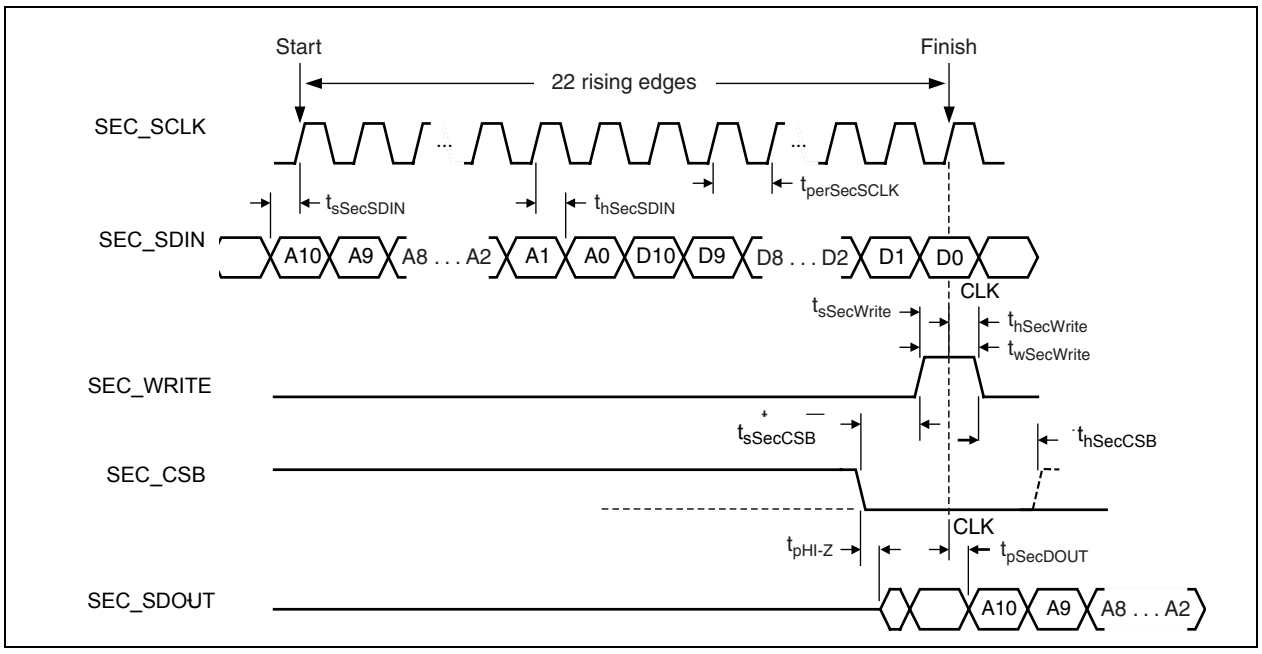


Figure 10. Secondary Access Port Write Timing Diagram

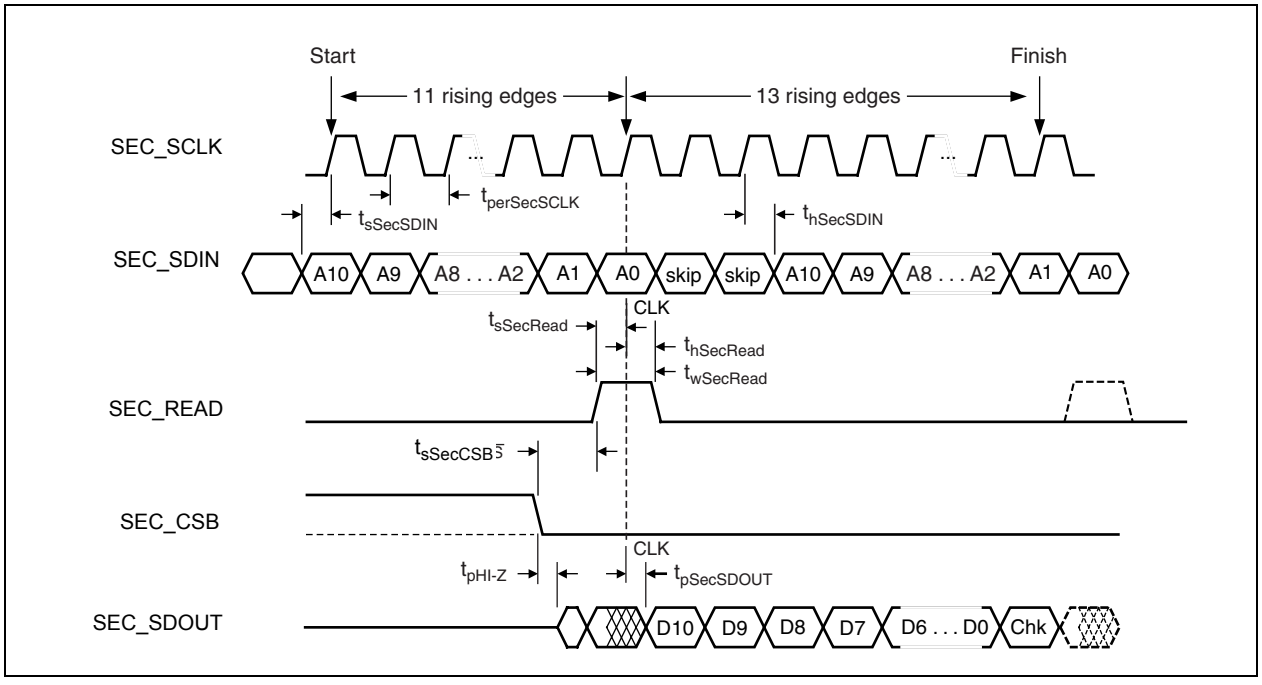


Figure 11. Secondary Access Port Read Timing Diagram

DC Characteristics

Unless stated otherwise, all data is assumed to be over recommended operating conditions.

Table 11. High-Speed Data Inputs (A, AN), Differential CML

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{A_DE}	Voltage input swing (differential drive)	200		2000	mVp-p	Mean p-p differential amplitude between true and complement inputs. See Figure 5, page 25.
V_{ICM}	Input common-mode voltage	V_{CC} – 0.7	2	V_{CC} – 0.3	V	
R_{IN_A}	Input resistance	80	100	120	Ω	Between true and complement Inputs. See Figure 15.

Table 12. High-Speed Data Outputs (Y, YN), Differential CML

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OUT_ND}	Serial data output voltage swing: Nominal drive mode	500	650	800	mVp-p	Mean p-p differential amplitude between true and complement outputs. With 50 Ω to V_{CC}.
V_{OUT_HD}	Serial data output voltage swing: High drive mode	1000	1300	1600	mVp-p	Mean p-p differential amplitude between true and complement outputs. With 50 Ω to V_{CC}.
R_{OUT_Y}	Back-terminated output resistance	40	50	60	Ω	See Figure 15.

Table 13. LVTTL/CMOS Input Signals

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	1.7	V_{CCD} + 1.0	V	V_{CCD} = 2.5 V / 3.3 V
V_{IL}	Input LOW voltage	0	0.8	V	V_{CCD} = 2.5 V / 3.3 V
I_{IH}	Input HIGH current		100	µA	
I_{IL}	Input LOW current	–100		µA	

Table 14. LVTTL/CMOS Output Signals

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{OH}	Output HIGH voltage	V_{CCD} – 0.2	V_{CCD}	V	DC load < 500 µA
V_{OL}	Output LOW voltage	0	0.2	V	DC load < 2 mA

Table 15. Power Dissipation

Symbol	Parameter	Typical	Maximum	Unit	Condition
P_{D_ND}	Total power dissipation: Nominal drive mode	4.5	5.0	W	V_{CC} = 2.5 V ± 5%
P_{D_HD}	Total power dissipation: High drive mode	6.5	7.2	W	V_{CC} = 2.5 V ± 5%

Operating Conditions

Table 16. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Power supply voltage	+2.375	+2.5	+2.625	V
V_{CCD}	Power supply voltage, programming port(1)		+2.5 or +3.3		V
T	Operating temperature(2)	0		+85	°C

1. *All timing specifications and diagrams reflect +3.3 V.*
2. *Lower limit of specification is ambient temperature, and upper limit is case temperature.*

Maximum Ratings

Table 17. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{CC}	Power Supply Voltage, Potential to GND	–0.5	+3.5	V
	DC Input Voltage Applied (TTL)	–0.5	V_{CCD} + 1.0	V
	DC Input Voltage Applied (CML)	–0.5	V_{CC} + 0.5	V
I_{OUT}	Output Current	–50	+50	mA
T_S	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–500	+500	V

Stresses listed under Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliabiility of the device.

I/O Equivalent Circuits

Input Termination

Termination resistor pairs are isolated between each input to minimize crosstalk. The termination will self-bias to +2.0 V (nominal) for AC-coupled applications.

All input data must be differential and nominally biased to +2.0 V relative to V_{EE} or AC-coupled. Internal terminations are provided with nominally 50 Ω from the true and complement inputs to a common bias point.

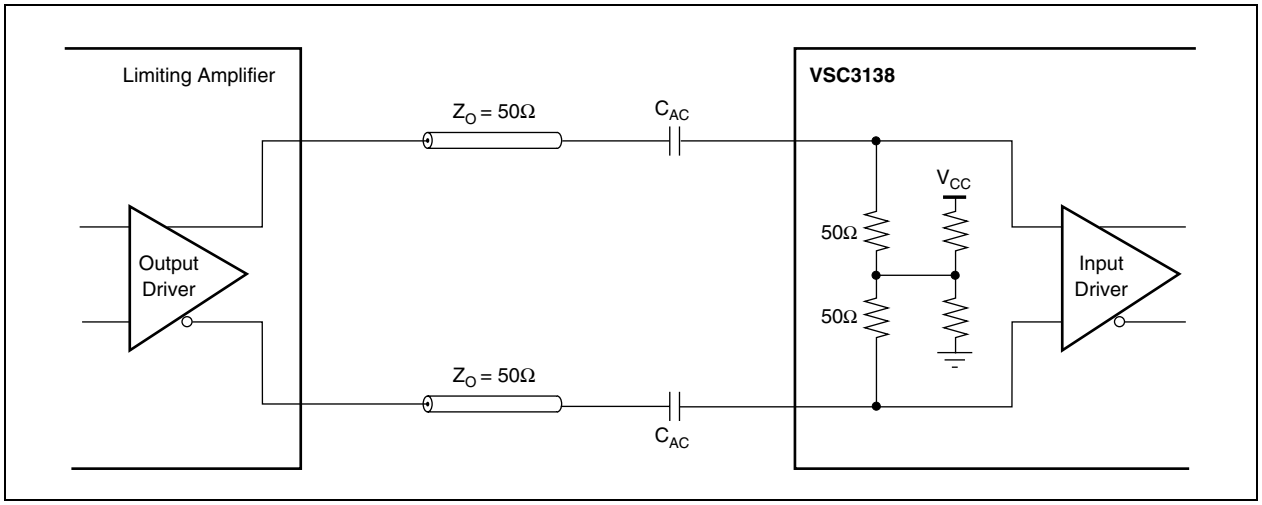


Figure 12. Differential AC-Coupled Input Termination

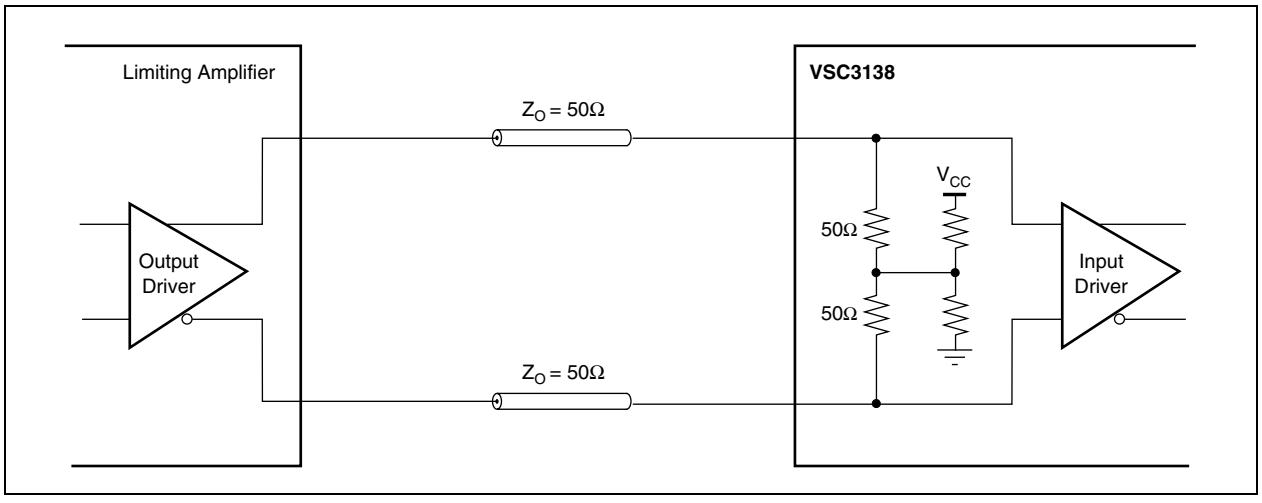
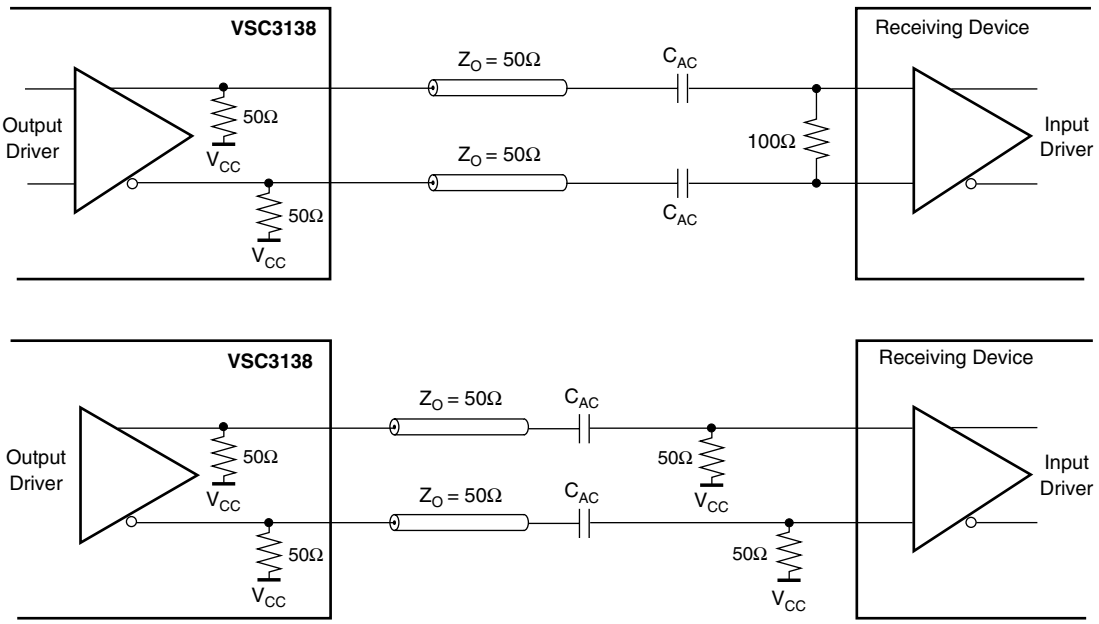


Figure 13. Differential DC-Coupled Input Termination

Output Termination

The high-speed outputs of the VSC3138 are current sinks, internally back-terminated by 50 Ω pull-up resistors to the positive supply rail. Typical DC terminations are 50 Ω pull-ups to the positive supply rail, 50 Ω terminations to +2.0 V, and 100 Ω from true to complement.

Data outputs are provided through differential current switches with on-chip 50 Ω back-termination. Two drive levels are provided to facilitate power and noise margin optimization on a per-output basis.



NOTE: The 50Ω and 100Ω termination resistors can be internal or external to the receiving device.

Figure 14. High-Speed Output—AC Coupled Terminations

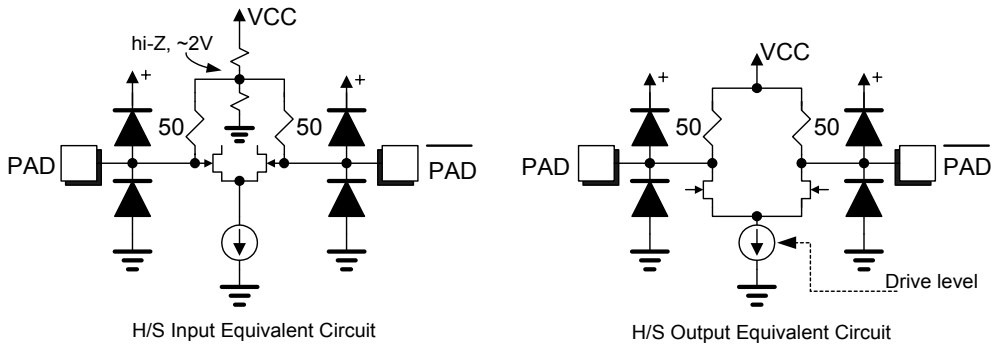


Figure 15. Input and Output Equivalent Circuits

PIN DESCRIPTIONS

Pin Diagram

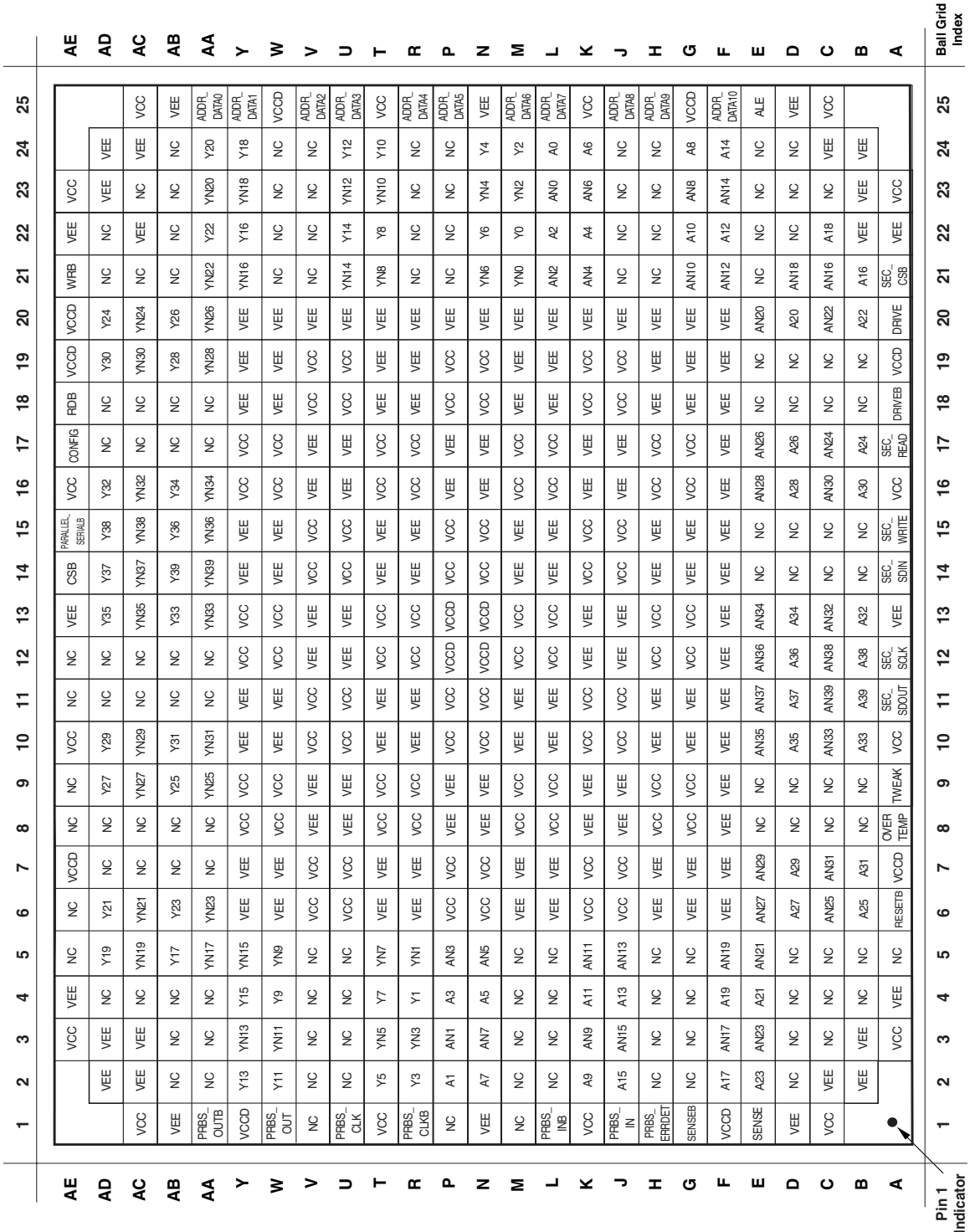


Figure 16. Pin Diagram, Bottom View

Pin Identifications

Table 18. Pin Identifications

Pin	Pin Site	I/O	Level	Description
High-Speed Data Inputs				
A0, AN0	L24, L23	I	CML	Data input channel 0; true, complement.
A1, AN1	P2, P3	I	CML	Data input channel 1; true, complement.
A2, AN2	L22, L21	I	CML	Data input channel 2; true, complement.
A3, AN3	P4, P5	I	CML	Data input channel 3; true, complement.
A4, AN4	K22, K21	I	CML	Data input channel 4; true, complement.
A5, AN5	N4, N5	I	CML	Data input channel 5; true, complement.
A6, AN6	K24, K23	I	CML	Data input channel 6; true, complement.
A7, AN7	N2, N3	I	CML	Data input channel 7; true, complement.
A8, AN8	G24, G23	I	CML	Data input channel 8; true, complement.
A9, AN9	K2, K3	I	CML	Data input channel 9; true, complement.
A10, AN10	G22, G21	I	CML	Data input channel 10; true, complement.
A11, AN11	K4, K5	I	CML	Data input channel 11; true, complement.
A12, AN12	F22, F21	I	CML	Data input channel 12; true, complement.
A13, AN13	J4, J5	I	CML	Data input channel 13; true, complement.
A14, AN14	F24, F23	I	CML	Data input channel 14; true, complement.
A15, AN15	J2, J3	I	CML	Data input channel 15; true, complement.
A16, AN16	B21, C21	I	CML	Data input channel 16; true, complement.
A17, AN17	F2, F3	I	CML	Data input channel 17; true, complement.
A18, AN18	C22, D21	I	CML	Data input channel 18; true, complement.
A19, AN19	F4, F5	I	CML	Data input channel 19; true, complement.
A20, AN20	D20, E20	I	CML	Data input channel 20; true, complement.
A21, AN21	E4, E5	I	CML	Data input channel 21; true, complement.
A22, AN22	B20, C20	I	CML	Data input channel 22; true, complement.
A23, AN23	E2, E3	I	CML	Data input channel 23; true, complement.
A24, AN24	B17, C17	I	CML	Data input channel 24; true, complement.
A25, AN25	B6, C6	I	CML	Data input channel 25; true, complement.
A26, AN26	D17, E17	I	CML	Data input channel 26; true, complement.
A27, AN27	D6, E6	I	CML	Data input channel 27; true, complement.
A28, AN28	D16, E16	I	CML	Data input channel 28; true, complement.
A29, AN29	D7, E7	I	CML	Data input channel 29; true, complement.
A30, AN30	B16, C16	I	CML	Data input channel 30; true, complement.
A31, AN31	B7,C7	I	CML	Data input channel 31; true, complement.
A32, AN32	B13, C13	I	CML	Data input channel 32; true, complement.
A33, AN33	B10, C10	I	CML	Data input channel 33; true, complement.
A34, AN34	D13, E13	I	CML	Data input channel 34; true, complement.
A35, AN35	D10, E10	I	CML	Data input channel 35; true, complement.

Table 18. Pin Identifications *(continued)*

Pin	Pin Site	I/O	Level	Description
A36, AN36	D12, E12	I	CML	Data input channel 36; true, complement.
A37, AN37	D11, E11	I	CML	Data input channel 37; true, complement.
A38, AN38	B12, C12	I	CML	Data input channel 38; true, complement.
A39, AN39	B11, C11	I	CML	Data input channel 39; true, complement.
High-Speed Data Outputs				
Y0, YN0	M22, M21	O	CML	Data output channel 0; true, complement.
Y1, YN1	R4, R5	O	CML	Data output channel 1; true, complement.
Y2, YN2	M24, M23	O	CML	Data output channel 2; true, complement.
Y3, YN3	R2, R3	O	CML	Data output channel 3; true, complement.
Y4, YN4	N24, N23	O	CML	Data output channel 4; true, complement.
Y5, YN5	T2, T3	O	CML	Data output channel 5; true, complement.
Y6, YN6	N22, N21	O	CML	Data output channel 6; true, complement.
Y7, YN7	T4, T5	O	CML	Data output channel 7; true, complement.
Y8, YN8	T22, T21	O	CML	Data output channel 8; true, complement.
Y9, YN9	W4, W5	O	CML	Data output channel 9; true, complement.
Y10, YN10	T24, T23	O	CML	Data output channel 10; true, complement.
Y11, YN11	W2, W3	O	CML	Data output channel 11; true, complement.
Y12, YN12	U24, U23	O	CML	Data output channel 12; true, complement.
Y13, YN13	Y2, Y3	O	CML	Data output channel 13; true, complement.
Y14, YN14	U22, U21	O	CML	Data output channel 14; true, complement.
Y15, YN15	Y4, Y5	O	CML	Data output channel 15; true, complement.
Y16, YN16	Y22, Y21	O	CML	Data output channel 16; true, complement.
Y17, YN17	AB5, AA5	O	CML	Data output channel 17; true, complement.
Y18, YN18	Y24, Y23	O	CML	Data output channel 18; true, complement.
Y19, YN19	AD5, AC5	O	CML	Data output channel 19; true, complement.
Y20, YN20	AA24, AA23	O	CML	Data output channel 20; true, complement.
Y21, YN21	AD6, AC6	O	CML	Data output channel 21; true, complement.
Y22, YN22	AA22, AA21	O	CML	Data output channel 22; true, complement.
Y23, YN23	AB6, AA6	O	CML	Data output channel 23; true, complement.
Y24, YN24	AD20, AC20	O	CML	Data output channel 24; true, complement.
Y25, YN25	AB9, AA9	O	CML	Data output channel 25; true, complement.
Y26, YN26	AB20, AA20	O	CML	Data output channel 26; true, complement.
Y27, YN27	AD9, AC9	O	CML	Data output channel 27; true, complement.
Y28, YN28	AB19, AA19	O	CML	Data output channel 28; true, complement.
Y29, YN29	AD10, AC10	O	CML	Data output channel 29; true, complement.
Y30, YN30	AD19, AC19	O	CML	Data output channel 30; true, complement.
Y31, YN31	AB10, AA10	O	CML	Data output channel 31; true, complement.
Y32, YN32	AD16, AC16	O	CML	Data output channel 32; true, complement.
Y33, YN33	AB13, AA13	O	CML	Data output channel 33; true, complement.

Table 18. Pin Identifications *(continued)*

Pin	Pin Site	I/O	Level	Description
Y34, YN34	AB16, AA16	O	CML	Data output channel 34; true, complement.
Y35, YN35	AD13, AC13	O	CML	Data output channel 35; true, complement.
Y36, YN36	AB15, AA15	O	CML	Data output channel 36; true, complement.
Y37, YN37	AD14, AC14	O	CML	Data output channel 37; true, complement.
Y38, YN38	AD15, AC15	O	CML	Data output channel 38; true, complement.
Y39, YN39	AB14, AA14	O	CML	Data output channel 39; true, complement.
Control Pins				
ADDR_DATA0	AA25	I/O	LVTTL	Address and data bus bit 0.
ADDR_DATA1	Y25	I/O	LVTTL	Address and data bus bit 1.
ADDR_DATA2	V25	I/O	LVTTL	Address and data bus bit 2.
ADDR_DATA3	U25	I/O	LVTTL	Address and data bus bit 3.
ADDR_DATA4	R25	I/O	LVTTL	Address and data bus bit 4.
ADDR_DATA5	P25	I/O	LVTTL	Address and data bus bit 5.
ADDR_DATA6	M25	I/O	LVTTL	Address and data bus bit 6.
ADDR_DATA7	L25	I/O	LVTTL	Address and data bus bit 7.
ADDR_DATA8	J25	I/O	LVTTL	Address and data bus bit 8.
ADDR_DATA9	H25	I/O	LVTTL	Address and data bus bit 9.
ADDR_DATA10	F25	I/O	LVTTL	Address and data bus bit 10.
ALE	E25	I	LVTTL	Control signal. Multiplexed ADDR_DATA bus select; ALE = 1 selects the address (output); ALE = 0 selects the data (input) information on the ADDR_DATA bus.
CONFIG	AE17	I	LVTTL	Control signal. Logic HIGH transfers programming to main program memory.
CSB	AE14	I	LVTTL	Control signal. Selects the device to be programmed when CSB = 0. When CS = 1, it is not possible to write or read from the device.
DRIVE	A20	I	CML	High-speed Input. External test signal input for signal path integrity verification; true.
DRIVEB	A18	I	CML	High-speed Input. External test signal input for signal path integrity verification; complement.
OVERTEMP	A8	O	LVTTL	Status signal. Overtemp flag exceeding user-defined temperature range.
PARALLEL_ SERIALB	AE15	I	LVTTL	Control signal. Selects between parallel or serial mode operation of the main programming port. PARALLEL_SERIALB programming mode; 1 = Parallel, 0 = Serial.
PRBS_CLK	U1	I	CML	High-speed input. PRBS external clock input; true. When AC-coupled, external bias resistors will be required.
PRBS_CLKB	R1	I	CML	High-speed Input. PRBS external clock input; complement. When AC-coupled, external bias resistors will be required.
PRBS_ERRDET	H1	O	LVTTL	Status signal. PRBS error detect
PRBS_IN	J1	I	CML	High-speed input. PRBS detector input; true. When AC-coupled, external bias resistors will be required.

Table 18. Pin Identifications *(continued)*

Pin	Pin Site	I/O	Level	Description
PRBS_INB	L1	I	CML	High-speed input. PRBS detector input; complement. When AC-coupled, external bias resistors will be required.
PRBS_OUT	W1	O	CML	High-speed output. PRBS generator output; true.
PRBS_OUTB	AA1	O	CML	High-speed output. PRBS generator output; complement.
RDB	AE18	I	LVTTL	Control signal. Address and data multiplexed bus read, active LOW. See "Programming Interface," page 10 and "Address Map for Output Addresses," page 15.
RESETB	A6	I	LVTTL	Control signal. Address and data multiplexed bus reset.
SEC_CSB	A21	I	LVTTL	Control signal. Secondary access port CSB.
SEC_READ	A17	I	LVTTL	Control signal. Secondary access port read.
SEC_SCLK	A12	I	LVTTL	Control signal. Secondary access port external serial clock input.
SEC_SDIN	A14	I	LVTTL	Control signal. Secondary access port serial data input.
SEC_SDOUT	A11	O	LVTTL	Control signal. Secondary access port serial data output.
SEC_WRITE	A15	I	LVTTL	Control signal. Secondary access port write.
SENSE	E1	O	CML	Control signal. Signal path integrity verification output; true.
SENSEB	G1	O	CML	Control signal. Signal path integrity verification output; complement.
TWEAK	A9	I	LVTTL	Test signal. Internal test pin for factory use only. Do not connect to any supply, ground, or device.
WRB	AE21	I	LVTTL	Control signal. Address and data multiplexed bus write.

Table 19. Power Supply Pins

Pin	Pin Site	Description
NC	A5, B4, B5, B8, B9, B14, B15, B18, B19, C3, C4, C5, C8, C9, C14, C15, C18, C19, C23, D2, D3, D4, D5, D8, D9, D14, D15, D18, D19, D22, D23, D24, E8, E9, E14, E15, E18, E19, E21, E22, E23, E24, G2, G3, G4, G5, H2, H3, H4, H5, H21, H22, H23, H24, J21, J22, J23, J24, L2, L3, L4, L5, M1, M2, M3, M4, M5, P1, P21, P22, P23, P24, R21, R22, R23, R24, U2, U3, U4, U5, V1, V2, V3, V4, V5, V21, V22, V23, V24, W21, W22, W23, W24, AA2, AA3, AA4, AA7, AA8, AA11, AA12, AA17, AA18, AB2, AB3, AB4, AB7, AB8, AB11, AB12, AB17, AB18, AB21, AB22, AB23, AB24, AC4, AC7, AC8, AC11, AC12, AC17, AC18, AC21, AC23, AD4, AD7, AD8, AD11, AD12, AD17, AD18, AD21, AD22, AE5, AE6, AE8, AE9, AE11, AE12	Do not connect to any supply, ground or device.
VCC	A3, A10, A16, A23, C1, C25, G8, G9, G12, G13, G16, G17, H8, H9, H12, H13, H16, H17, J6, J7, J10, J11, J14, J15, J18, J19, K1, K6, K7, K10, K11, K14, K15, K18, K19, K25, L8, L9, L12, L13, L16, L17, M8, M9, M12, M13, M16, M17, N6, N7, N10, N11, N14, N15, N18, N19, P6, P7, P10, P11, P14, P15, P18, P19, R8, R9, R12, R13, R16, R17, T1, T8, T9, T12, T13, T16, T17, T25, U6, U7, U10, U11, U14, U15, U18, U19, V6, V7, V10, V11, V14, V15, V18, V19, W8, W9, W12, W13, W16, W17, Y8, Y9, Y12, Y13, Y16, Y17, AC1, AC25, AE3, AE10, AE16, AE23	Positive power supply, +2.5 V
VCCD(1)	A7, A19, F1, G25, N12, N13, P12, P13, W25, Y1, AE7, AE19, AE20	Positive power supply, 2.5 V or 3.3 V

Table 19. Power Supply Pins *(continued)*

Pin	Pin Site	Description
VEE	A4, A13, A22, B2, B3, B22, B23, B24, C2, C24, D1, D25, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, G6, G7, G10, G11, G14, G15, G18, G19, G20, H6, H7, H10, H11, H14, H15, H18, H19, H20, J8, J9, J12, J13, J16, J17, J20, K8, K9, K12, K13, K16, K17, K20, L6, L7, L10, L11, L14, L15, L18, L19, L20, M6, M7, M10, M11, M14, M15, M18, M19, M20, N1, N8, N9, N16, N17, N20, N25, P8, P9, P16, P17, P20, R6, R7, R10, R11, R14, R15, R18, R19, R20, T6, T7, T10, T11, T14, T15, T18, T19, T20, U8, U9, U12, U13, U16, U17, U20, V8, V9, V12, V13, V16, V17, V20, W6, W7, W10, W11, W14, W15, W18, W19, W20, Y6, Y7, Y10, Y11, Y14, Y15, Y18, Y19, Y20, AB1, AB25, AC2, AC3, AC22, AC24, AD2, AD3, AD23, AD24, AE4, AE13, AE22	Ground

1. *3.3 V is recommended. All timing diagrams are with V_{CCD} = 3.3 V.*

PACKAGE INFORMATION

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

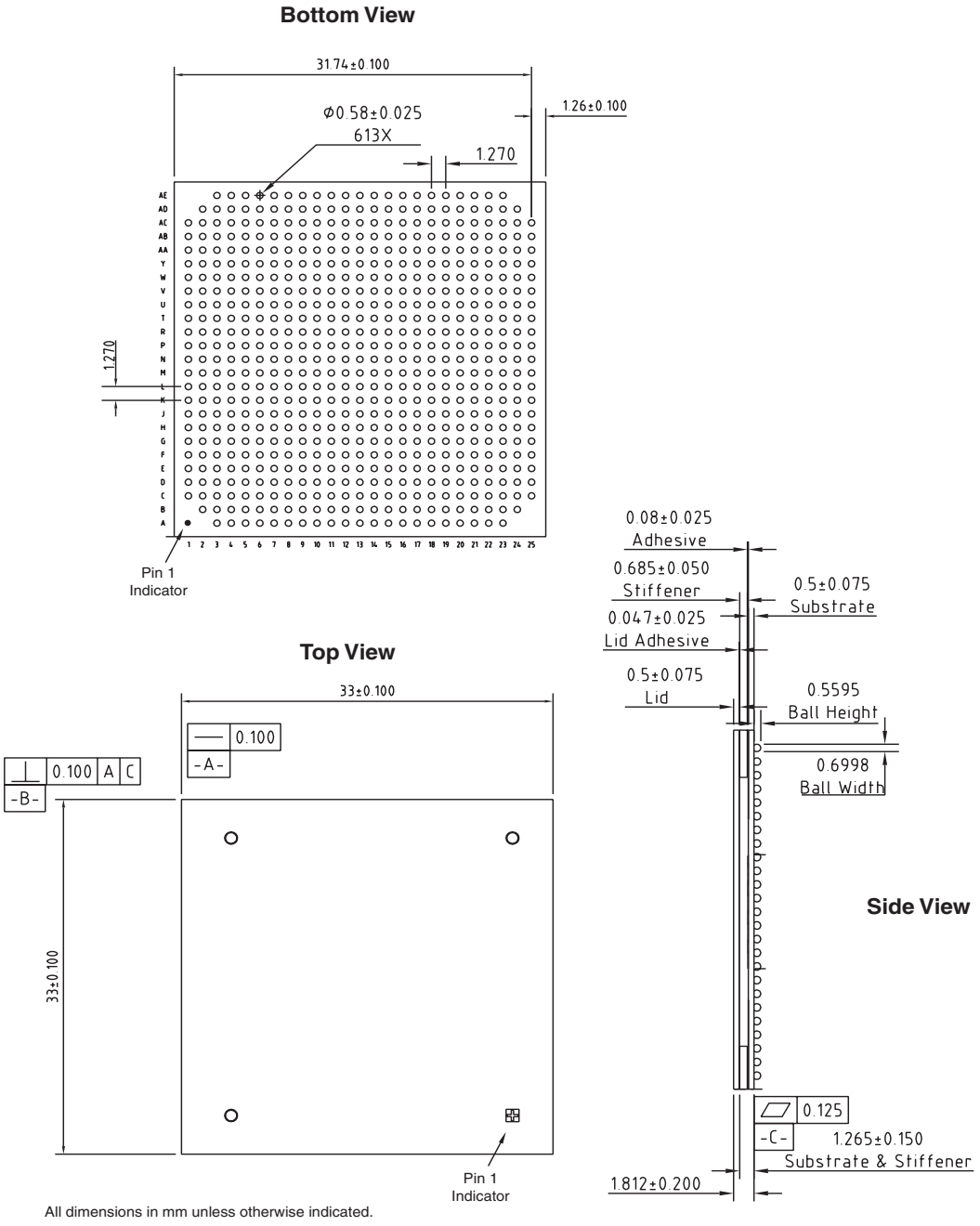


Figure 17. Package Drawing

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 20. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC3138SH	0.5	12	11	9.6
VSC3138XSH	0.5	12	11	9.6

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

VSC3138 4.25 Gbps 40 x 40 Asynchronous Crosspoint Switch

Part Number	Description
VSC3138SH	613-pin BGA, 33 mm x 33 mm body, 1.27 mm ball pitch
VSC3138XSH	Lead-free, 613-pin BGA, 33 mm × 33 mm body, 1.27 mm ball pitch

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