Advance Product Information

64x64 Crosspoint Switch

VSC6464

Features

- Synchronous or Asynchronous Operation
- 500Mb/s Asynchronous Operation
- 250Mb/s Synchronous Operation
- ≤750ps Output to Output Skew (Synchronous)
- ≤1.5ns Skew Input to Output (Asynchronous)
- Single Ended ECL I/O
- Separate Input and Output Register Clocks
- Single Supply: -2V ± 5% @ 8 Watts (Max.)
- Commercial (0^{o} to $+70^{o}$C) Temperature Range
- Package: 208PQFP

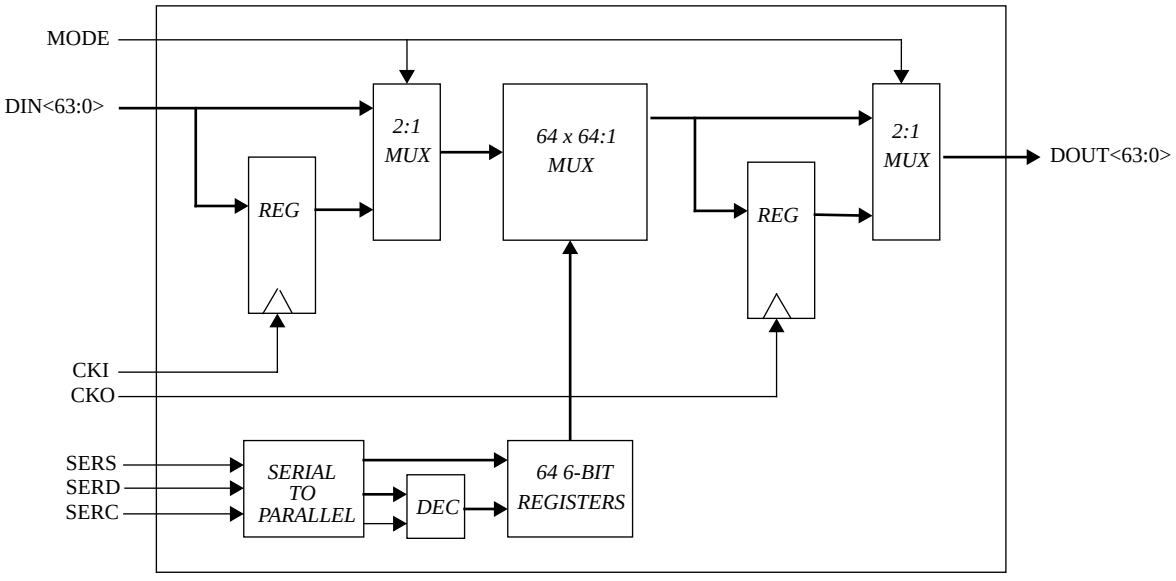
General Description

The VSC6464 is a 64x64 asynchronous (flow-through) or synchronous (clocked) high-speed crosspoint switch. Any input can be multiplexed to any, some, or all outputs. The switch is fully non-blocking. All I/Os are single-ended ECL. The part is packaged in a 208-pin plastic quad flat pack and consumes less than 8 Watts from a single -2V power supply.

In the asynchronous mode, high speed digital data up to 500Mb/s can be switched with less than 25% pulse width distortion. Skew is less than 1.5 ns between any two paths through the switch. In broadcast operation (one input routed to two or more outputs), any two outputs will exhibit less than 750ps of skew.

In the synchronous mode, high-speed digital data up to 250 Mb/s can be switched with less than 750ps output-to-output skew. The input and output registers have separate clock inputs.

VSC6464 Functional Block Diagram



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Functional Description

This Crosspoint Switch connects any of the 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control register.

Signals from the 64 inputs (DIN_0 through DIN_63) are connected to the 64 output channels (DOUT_0 through DOUT_63) through sixty-four 64:1 multiplexers. The traffic pattern is controllable by data stored in sixty-four 6-bit control registers with each register corresponding to an output channel. The six bits are a binary numerical representation of the input channel selected (i.e.: 000000 corresponds to DIN_0, 000001 corresponds to DIN_1, etc.). An additional six bit register is used to address the output channel being programmed. These six bits are a binary numerical representation of the output channel (ie.: 000000 corresponds to DOUT_0, 000001 corresponds to DOUT_1, etc.). All twelve configuration bits are loaded through a three-pin serial port.

The crosspoint is configured through a serial data port consisting of three pins: SERS, SERC, and SERD. SERS is used to select the crosspoint for configuration. SERC is a serial clock signal whose rising edge samples the serial data on SERD when SERS is active (HI). The serial data stream applied to SERD consists of the six bits of address, followed by the six bits of data. Address information is used to identify one of the 64 output channels, a valid value is between 0 and 63. Data information selects a specific input to be directed to the addressed output, valid values are between 0 and 63. Both address and data information are received MSB first. A serial load cycle consists of activating serial select (SERS), pulsing serial clock 12 times (with valid data surrounding each rising edge), then deactivating serial select (SERS). Deactivating serial select before the twelfth rising edge of SERC will abort the load cycle. Serial select (SERS) must be deactivated for 10ns following a power up. Any additional clocking of SERC during a load cycle, beyond that described above, is ignored.

The MODE pin determines the operating mode of the Crosspoint: synchronous or asynchronous, as shown in Table 1.

A test output (TESTO) is provided for internal visibility, this signal will go high when a thirteenth rising edge is applied during a load cycle; TESTO goes low when either SERS is lowered, or a fourteenth SERC edge is received during a load cycle. This output can be left unconnected if desired, to reduce noise and power dissipation.

Table 1: Crosspoint Mode (MODE)

Function	*MODE*
Asynchronous 64x64	0
Synchronous 64x64	1

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AC Characteristics *(Over recommended operating conditions)*

Figure 1 Output Loading

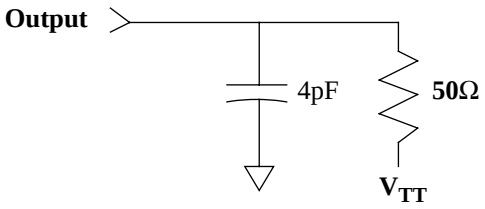
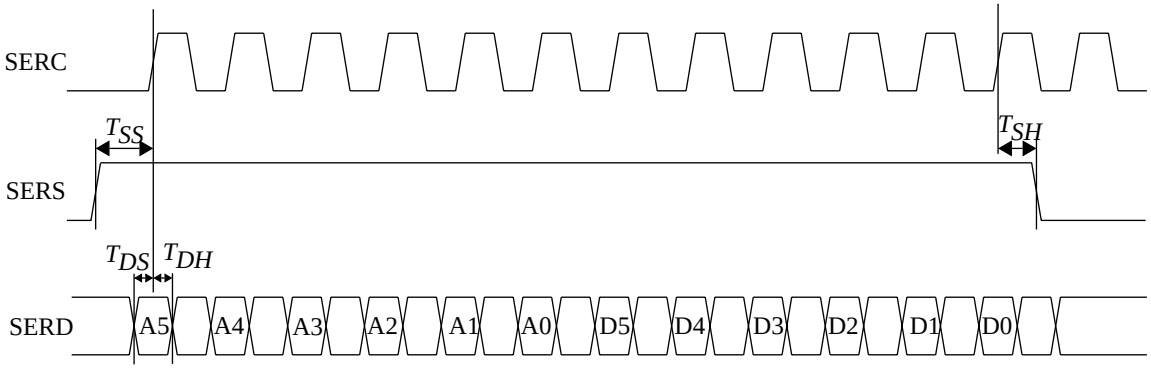


Figure 2 VSC6464 Configuration Timing Diagram



Note: A5 is MSB of A<5:0>, D5 is MSB of D<5:0>.

Table 2: VSC6464 Asynchronous Timing Table

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{SS}	SERS setup time with respect to SERC	10	-	-	ns
T_{SH}	SERS hold time with respect to SERC	10	-	-	ns
T_{DS}	SERD setup time with respect to SERC	10	-	-	ns
T_{DH}	SERD setup time with respect to SERC	10	-	-	ns

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Figure 3 VSC6464 Asynchronous Timing Diagram

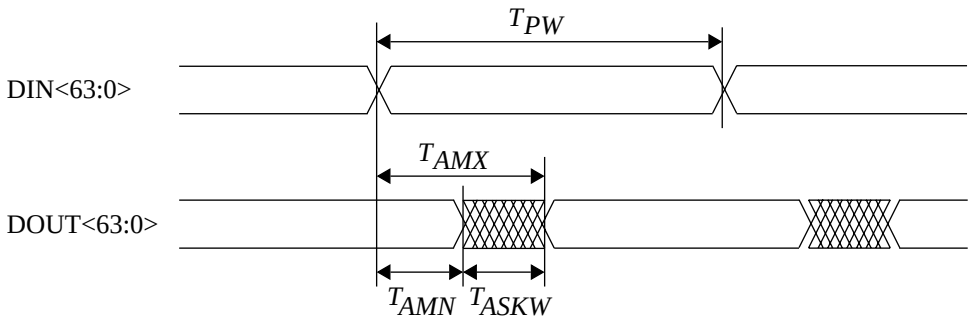

Table 3: VSC6464 Asynchronous Timing Table

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{PW}	Minimum DIN<63:0> pulse width, 50% input	1.25	-	-	ns
T_{AMX}	DIN<63:0> to DOUT<63:0> propagation delay	-	-	6.5	ns
T_{AMN}	DIN<63:0> to DOUT<63:0> propagation delay	2.2	-	-	ns
T_{ASKW}	DOUT<63:0> asynchronous mode data skew (any input to any output, add 0.1 for SSO)	-	-	1.4	ns
T_{ASKW}	DOUT<63:0> asynchronous mode data skew (broadcast, add 0.1 for SSO)	-	-	0.75	ns
-	Duty Cycle Distortion, @500Mb/s(1)	-	-	25	%

*Note: 1.) Duty cycle distortion = (duty cycle in - duty cyle out)/duty cycle in * 100%, measured with a 2ns pulse width.*

Figure 4 VSC6464 Synchronous Data Input Timing Diagram

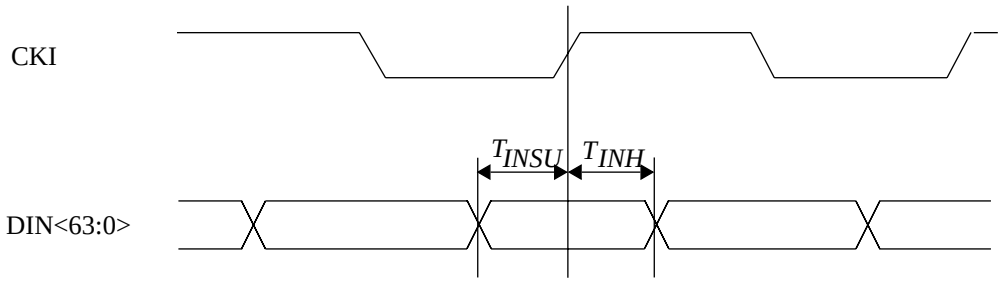

Table 4: VSC6464 Synchronous Data Input Timing Table

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*
F_{MAX}	Maximum CKI frequency, 50% input	-	-	250	MHz
T_{INSU}	DIN<63:0> data setup time with respect to CKI	0.5	-	-	ns
T_{INH}	DIN<63:0> data hold time with respect to CKI	0.4	-	-	ns

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Figure 5 VSC6464 Synchronous Data Output Timing Diagram

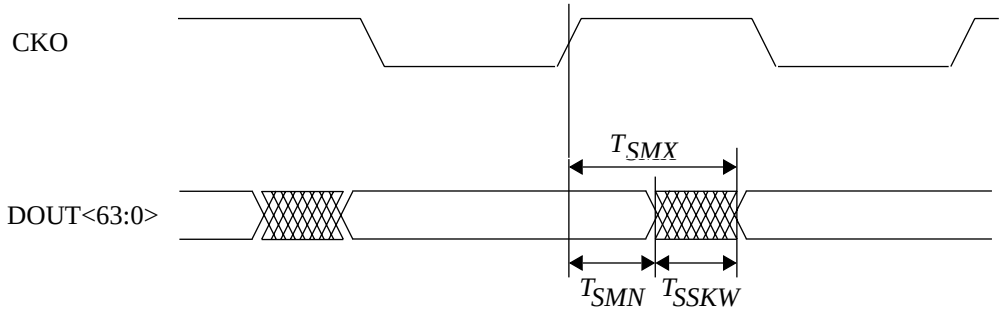

Table 5: VSC6464 Synchronous Data Output Timing Table

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*
F_{MAX}	Maximum CKO frequency, 50% input	-	-	250	MHz
T_{SMX}	Maximum propagation delay CKO toDOUT<63:0>	-	-	3.7	ns
T_{SMN}	Minimum propagation delay CKO to DOUT<63:0>	1.4	-	-	ns
T_{SSKW}	DOUT<63:0> synchronous mode data skew (add 0.1 for SSO)	-	-	0.75	ns

Figure 6 VSC6464 Synchronous Mode Clock Relationship

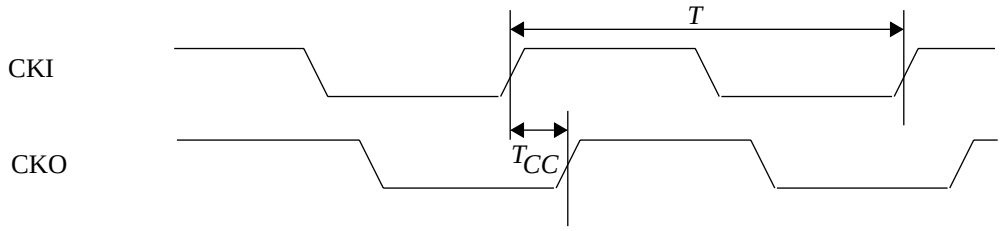

Table 6: VSC6464 Synchronous Data Output Timing Table

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CC}	CKO relative to CKI, 50% input	0.1	-	0.8	ns

Note: A nominal delay of 0.25 ns between input and output clocks can be achieved by a trace on the pc board run directly from the input clock pin to the output clock pin. In this case, the clock signal should be connected to the input pin with the delay supplied by the pc board trace.

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DC Characteristics

Table 7: ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	-
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	-
V_{IH}	Input HIGH voltage	-1100	-	-700	mV	-
V_{IL}	Input LOW voltage	-2000	-	-1540	mV	-
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN}=V_{IL}$ (min)

Power Dissipation

Table 8: VSC6464 Power Supply Currents

Parameter	Description	(Max)	Units
I_{TT}	Power supply current from V_{TT}	3.8	A
P_D	Power dissipation (*Note: Specified with outputs open circuit.*)	8	W

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0 V±0.1V
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC6464 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

Notes: 1) Load=50Ω to -2.0V.

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Pin Descriptions

Table 9: Pin Identification

Signal	*Pin*	*I/O*	*Description*
VCC	2-5, 15, 18, 24, 28, 29, 35, 38, 48-51, 61-63, 69, 72, 75, 79, 82, 85, 88, 94-96, 106-109, 119, 122, 128, 132, 133, 139, 142, 152-155, 165-167, 173, 176, 179, 183, 186, 189, 192, 198-200		0V Ground Connection.
VTT	8, 21, 27, 32, 45, 57, 78, 100, 112, 125, 131, 136, 149, 161, 182, 204		-2V Supply Connection.
DIN_0-DIN_63	156-160, 162-164, 201-203, 205-207, 1, 12-14, 16-17, 19-20, 22-23, 25, 30-31, 33-34, 36-37, 39-40, 52-56, 58-60, 97-99, 101-105, 118, 120-121, 123-124, 126-127, 129, 134-135, 137-138, 140-141, 143	I	The 64 ECL Signal Inputs.
DOUT_0-DOUT_63	10-9, 7-6, 197-193, 191-190, 188-187, 185-184, 181-180, 178-177, 175-174, 172-168, 151-150, 148-145, 116-113, 111, 93-89, 87-86, 84-83, 81-80, 77-76, 74-73, 71-70, 68-64, 47-46, 44-42	O	The 64 ECL Signal Outputs.
SERS	117	I	ECL Serial Select Signal
SERC	11	I	ECL Serial Clock Signal.
SERD	41	I	ECL Serial Data Signal.
CKI	26	I	ECL Synchronous Mode Input Register Clock Signal.
CKO	130	I	ECL Synchronous Mode Output Register Clock Signal.
MODE	144	I	ECL Synchronous Mode Enable Signal.
TESTO	110	O	do not use.
VSCTE	208	I	test input, connect to -2V for normal operation

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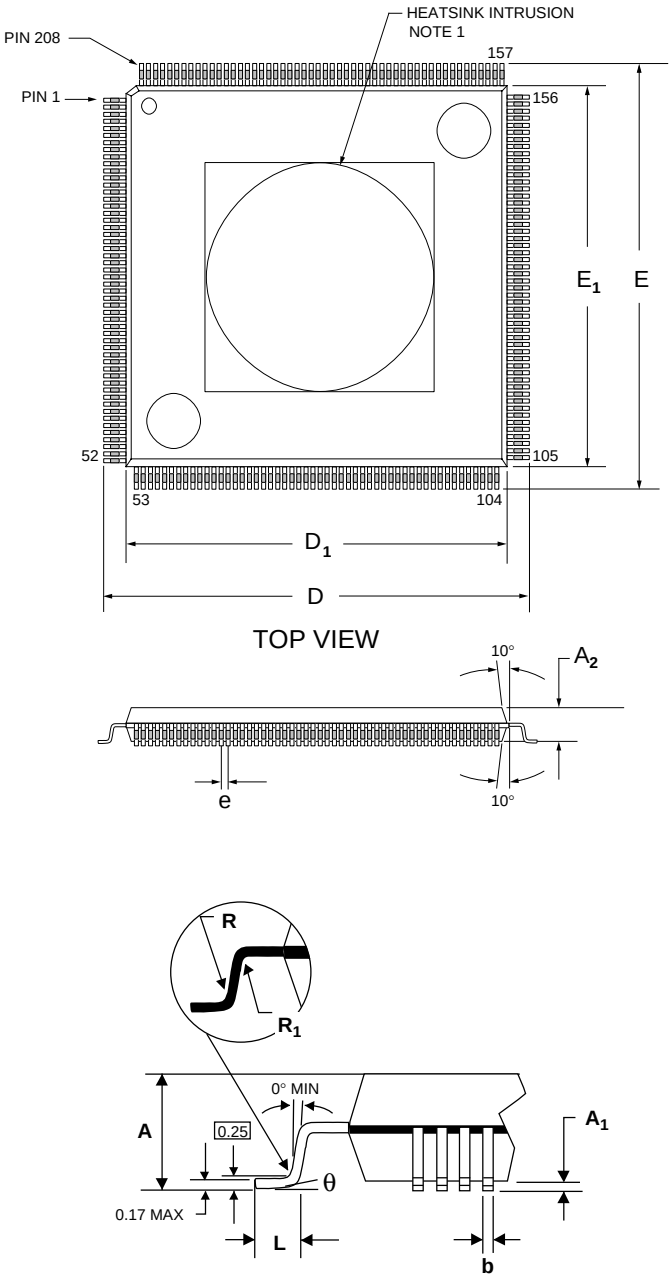
Package Information

The VSC6464 is packaged in a 208 PQFP with an integral heat sink as shown in the figure below.

208 PQFP Package Drawing



Key	*mm*	*Tolerances*
A	4.07	MAX
A_1	0.25	MIN
A_2	3.49	±.10
D	30.60	±.4
D_1	28.00	±.10
E	30.60	±.4
E_1	28.00	±.10
L	0.60	+.15/-.10
e	0.50	BASIC
b	0.22	±.05
θ	0° - 10°	
R_1	.15	TYP
R	.25	MAX

NOTES:

(1) Exposed Heatspreader will be either 20.32 ±.50 round or 12.0 ± .50 square

(2) Drawing not to scale.
Package #: 101-228-6, Issue #:1

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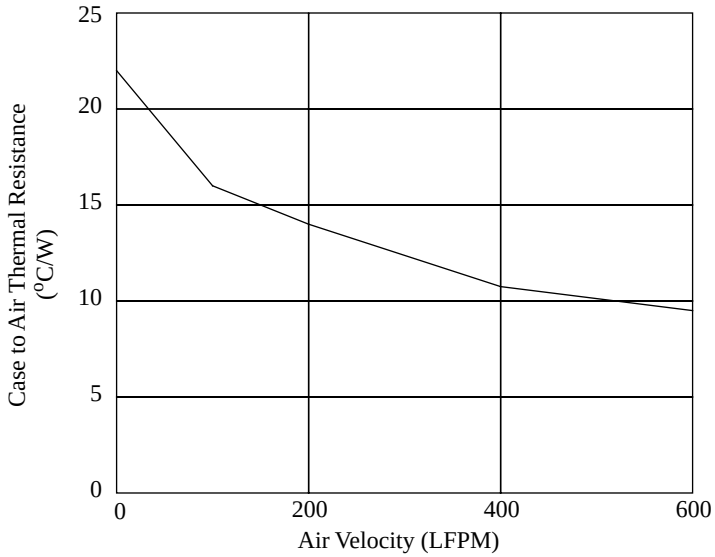
Thermal Information

Figure 7 ΘCA vs Air Velocity for the 208 PQFP (28mmx28mmx3.2mm)



Air Vel. LFPM	*Theta(ca) °C/W*
0	21.8
100	15.8
200	13.8
400	10.7
600	9.5

Θ_{CA} measurement method: Semi-standard G38-87, in a wind tunnel
Semi-standard G42-88/JEDEC JC 15.1 #1 FR4 PCB 3”x4.5”x0.62”

Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation’s product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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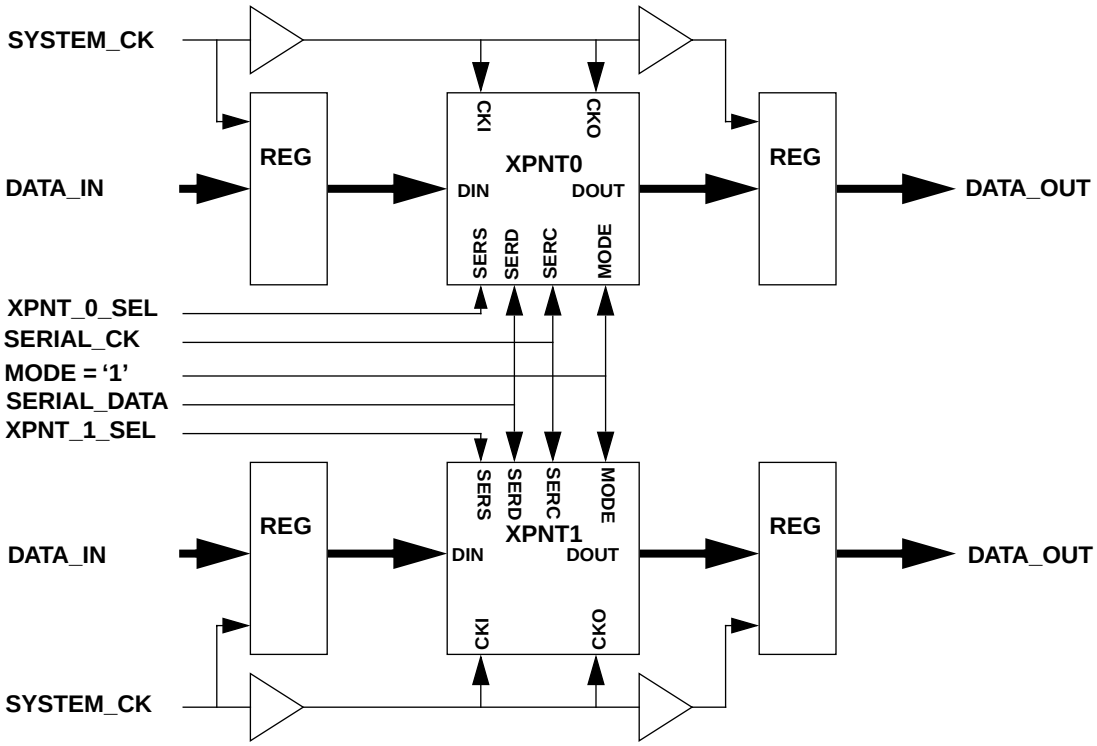
Application Notes

Figure 8 Multiple-Crosspoint Synchronous System Configuration



High-speed designs using single-ended ECL signals need careful design to avoid noise and crosstalk problems. The following suggestions can aid obtaining a reliable system:

1. Wide noise margins on input signals.

2. Avoid SSOs. Simultaneous switching outputs will degrade timing margins by increasing AC delay values, and reducing noisethresholds.

3. Provide good signal terminations and well-matched board traces in addition to well-controlled power supplies.

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