

8-Bit ADCs with Serial Interface and Differential or Dual Inputs

Description

WM0831 and WM0832 are 8-bit analogue to digital converters (ADC) with serial I/O interfaces, providing a choice of input configurations in 8-pin SO or DIP packages. WM0831 has a differential input, also configurable as a single ended input. A-D conversion results are serially output on Data Out (DO) under the control of clock and chip select inputs. The device has a separate voltage reference input.

WM0832's two input multiplexer is configurable via the Data In (DI) serial input, as two single ended inputs or a single differential input. The voltage reference operates ratiometrically and is internally connected to the VCC pin. Conversion is initiated by bringing and holding chip select low while providing a clock input. With WM0831's fixed input configuration, the conversion result is output at DO on the clock's falling edges in MSB to LSB order.

With WM0832's configurable input multiplexer, data is input to DI on the rising edges of the clock to setup the Mux and initiate conversion. Conversion results appear serially at DO on the falling edges of the clock, first in MSB to LSB order, and then repeated in LSB to MSB order.

WM0831/2 operate on 5V or 3.3V supply voltages and are available in small outline and DIP packages for commercial (0 to 70°C) and industrial (-40 to 85°C) temperature ranges.

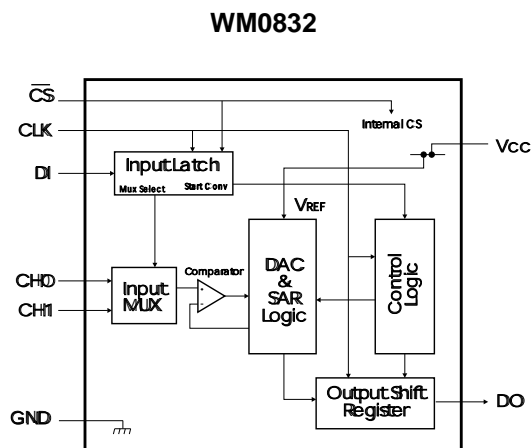
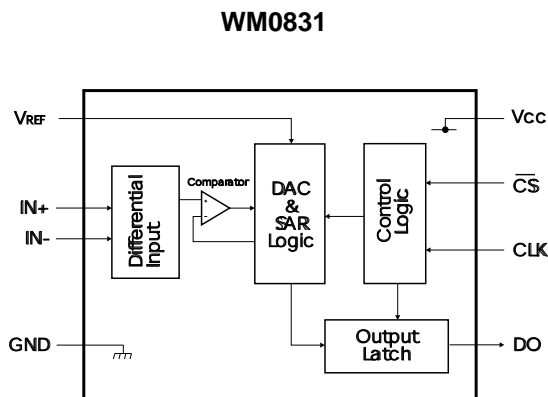
Features

- Functionally Equivalent to National Semiconductor ADC0831 and ADC0832
- **WM0831: Differential or single ended input**
- **WM0832: Two single ended inputs or a single differential input**
- **Ratiometric reference input (fixed for WM0832)**
- **Serial I/O interface**
- **Input range 0 to Vcc with Vcc Reference**
- **8 pin package, SO or DIP**
- **5V and 3.3V variants**
- **Total Unadjusted Error: ± 1 LSB**
- **8-bit resolution**
- **32 μ s conversion time at fclock = 250 kHz**

Applications

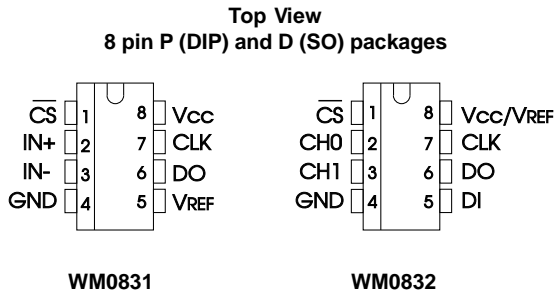
- Embedding with remote sensors
- Equipment health monitoring
- Automotive
- Industrial control

Block Diagrams



WM0831, WM0832

Pin Configuration



Ordering Information

5V devices

DEVICE	TEMP RANGE	PACKAGE
WM0831CP	0°C to 70°C	8 pin plastic DIP
WM0831CD	0°C to 70°C	8 pin plastic SO
WM0831IP	-40°C to 85°C	8 pin plastic DIP
WM0831ID	-40°C to 85°C	8 pin plastic SO
WM0832CP	0°C to 70°C	8 pin plastic DIP
WM0832CD	0°C to 70°C	8 pin plastic SO
WM0832IP	-40°C to 85°C	8 pin plastic DIP
WM0832ID	-40°C to 85°C	8 pin plastic SO

3.3V devices

DEVICE	TEMP. RANGE	PACKAGE
WM0831LCP	0°C to 70°C	8 pin plastic DIP
WM0831LCD	0°C to 70°C	8 pin plastic SO
WM0831LIP	-40°C to 85°C	8 pin plastic DIP
WM0831LID	-40°C to 85°C	8 pin plastic SO
WM0832LCP	0°C to 70°C	8 pin plastic DIP
WM0832LCD	0°C to 70°C	8 pin plastic SO
WM0832LIP	-40°C to 85°C	8 pin plastic DIP
WM0832LID	-40°C to 85°C	8 pin plastic SO

Absolute Maximum Ratings (note 1)

Supply Voltage, V_{CC} (note 2) 6.5 V
 Input voltage range:
 Digital Inputs GND - 0.3 V, V_{CC} + 0.3 V
 Analogue inputs GND - 0.3 V, V_{CC} + 0.3 V
 Input current, any pin (note 3) ± 5 mA
 Total Input current for package ± 20 mA

Operating temperature range, T_A T_{MIN} to T_{MAX}
 WM083_C_ (C suffix) 0°C to +70°C
 WM083_I_ (I suffix) -40°C to +85°C
 Storage Temperature - 65°C to +150°C
 Soldering Information:
 Lead Temperature 1.6 mm (1/16) from case
 for 10 seconds: D or P package 260°C

Recommended Operating Conditions (5V)

		SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage		V _{CC}	4.5	5	5.5	V
High level input voltage		V _{IH}	2			V
Low level input voltage		V _{IL}			0.8	V
Clock frequency		f _{clock}	10		600	KHz
Clock duty cycle (see Note 4)		D _{clk}	40		60	%
Pulse duration \overline{CS} high		t _{wH} (CS)		220		ns
Operating free-air temperature	C suffix	T _A	0		70	°C
	I Suffix	T _A	-40		85	

Electrical Characteristics (5V)

V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 250KHz, T_A = T_{MIN} to T_{MAX}, t_r = t_f = 20 ns, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level output voltage	V _{OH}	V _{CC} = 4.75 V, I _{OH} = -360 μA	2.4			V
		V _{CC} = 4.75 V, I _{OH} = -10 μA	4.5			V
Low level output voltage	V _{OL}	V _{CC} = 5.25 V, I _{OH} = 1.6 mA			0.4	V
High level input current	I _{IH}	V _{IH} = 5 V		0.005	1	μA
Low level input current	I _{IL}	V _{IL} = 0 V		-0.005	-1	μA
High level output (source) current	I _{OH}	V _{OH} = 0 V	-6.5	-24		mA
Low level output (sink) current	I _{OL}	V _{OL} = V _{CC}	8	26		mA
High impedance-state output current (DO)	I _{OZ}	V _O = 5 V		0.01	3	μA
		V _O = 0 V		-0.01	-3	μA
Input capacitance	C _I		5			pF
Output capacitance	C _O		5			pF
Converter and Multiplexer						
Total unadjusted error	TUE	V _{REF} = 5 V. (note 7)			±1	LSB
Differential Linearity		(note 8)	8			Bits
Supply voltage variation error	V _{s(error)}	V _{CC} = 4.75 V to 5.25 V		±1/16	±1/4	LSB
Common mode error		Differential mode		±1/16	±1/4	LSB
Common mode input voltage range	V _{ICR}	(note 9)	GND-0.05 V _{CC} +0.05			V
Standby input leakage current (note 10)	I _{I(stdby)}	On-channel	V _I = 5 V at ON ch.		1	μA
		Off-channel	V _I = 0 V at OFF ch.		-1	μA
		On-channel	V _I = 0 V at ON ch.		-1	μA
		Off-channel	V _I = 5 V at OFF ch.		1	μA
Conversion time	t _{conv}	Excluding MUX addressing time			8	clock periods
Reference Inputs						
Input resistance to reference ladder	R _{i(REF)}	Can only be tested for WM0831	1.3	2.4	5.9	kΩ
Total device						
Supply current WM0831	I _{CC}			0.6	1.25	mA
Supply current WM0832	I _{CC}	(note 11)		2.5	4.7	mA
Timing Parameters						
Setup time, \overline{CS} low or WM0832 data valid before clock ↑	t _{su}		350			ns
Hold time, WM0832 data valid after clock ↑	t _h		90			ns
Propagation delay time, output data after clock ↓	t _{pd}	MSB data first. C _L = 100 pF			1500	ns
		LSB data first. C _L = 100 pF			600	ns
Output disable time, DO after CS ↑	t _{dis}	C _L = 10 pF, R _L = 10 kΩ		125	250	ns
		C _L = 100 pF, R _L = 2 kΩ			500	ns

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Recommended Operating Conditions (3.3V)

	SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage	V _{CC}	2.7	3.3	3.6	V
High level input voltage	V _{IH}	2			V
Low level input voltage	V _{IL}			0.8	V
Clock frequency (V _{CC} = 3.3V)	f _{clock}	10		600	KHz
Clock duty cycle (see Note 4)	D _{clk}	40		60	%
Pulse duration \overline{CS} high	t _{wH(CS)}	220			ns
Operating free-air temperature	C suffix	T _A	0	70	°C
	I Suffix	T _A	-40	85	

Electrical Characteristics (3.3V)

V_{CC} = 3.3V, f_{CLK} = 250KHz, T_A = T_{MIN} to T_{MAX}, tr = tf = 20 ns, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level output voltage	VOH	VCC = 3V, IOH = -360 μA	2.4			V
		VCC = 3V, IOH = -10 μA	2.8			V
Low level output voltage	VOL	VCC = 3V, IOH = 1.6 mA			0.4	V
High level input current	I _{IH}	V _{IH} = 3.6 V		0.005	1	μA
Low level input current	I _{IL}	V _{IL} = 0 V		-0.005	-1	μA
High level output (source) current	IOH	VOH = 0 V, T _A = 25°C	6.5	15		mA
Low level output (sink) current	IOL	VOL = 0V, T _A = 25°C	8	16		mA
High impedance-state output current (DO)	IOZ	VO = 3.3V, T _A = 25°C		0.01	3	μA
		VO = 0 V, T _A = 25°C		-0.01	-3	μA
Input capacitance	CI			5		pF
Output capacitance	CO			5		pF
Converter and Multiplexer						
Total unadjusted error	TUE	VREF = 3.3 V. (note 7)			±1	LSB
Differential Linearity		(note 8)	8			Bits
Supply voltage variation error	V _{S(error)}	VCC = 3 V to 3.6 V		±1/16	±1/4	LSB
Common mode error		Differential mode		±1/16	±1/4	LSB
Common mode input voltage range	V _{ICR}	(note 9)	GND-0.05 VCC+0.05			V
Standby input leakage current (note 10)	I _{I(stbby)}	On-channel	V _I = 3.3V at ON ch.		1	μA
		Off-channel	V _I = 0 V at OFF ch.		-1	μA
		On-channel	V _I = 0 V at ON ch.		-1	μA
		Off-channel	V _I = 3.3V at OFF ch.		1	μA
Conversion time	t _{conv}	Excluding MUX addressing time			8	clock periods
Reference Inputs						
Input resistance to reference ladder	R _{I(REF)}	Can only be tested for WM0831	1.3	2.4	5.9	kΩ
Total device						
Supply current WM0831	I _{CC}			0.2	0.75	mA
Supply current WM0832	I _{CC}	(note 11)		1.5	2.5	mA
Timing Parameters						
Setup time, \overline{CS} low or WM0832 data valid before clock ↑	t _{su}		350			ns
Hold time, WM0832 data valid after clock ↑	t _h		90			ns
Propagation delay time, output data after clock ↓	t _{pd}	MSB data first. CL = 100 pF		200	500	ns
		LSB data first. CL = 100 pF		80	200	ns
Output disable time, DO after CS ↑	t _{dis}	CL = 10 pF, RL = 10 kΩ		80	125	ns
		CL = 100 pF, RL = 2 kΩ			250	ns

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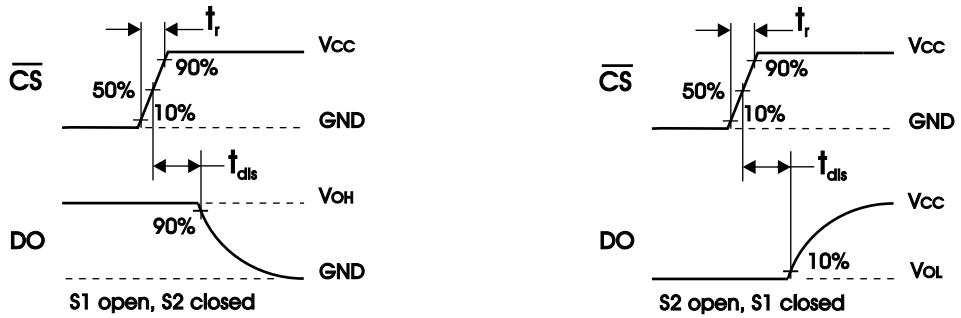
Electrical Characteristics (continued)

Notes:

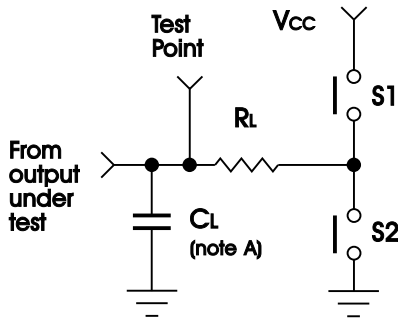
1. Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits are given under Recommended Operating Conditions. Guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.
2. All voltage values, except differential voltages are with respect to the ground.
3. When the input voltage V_{IN} at any pin exceeds the power supply rails ($GND > V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA supply current to four.
4. A clock duty cycle range of 40% to 60% ensures correct operation at all clock frequencies. For a clock with a duty cycle outside these limits, the minimum time the clock is high or low must be at least 666 ns, with the maximum time for clock high or low being 60 ms.
5. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ for 5V devices and $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$.
6. All parameters are measured under open-loop conditions with zero common mode input voltage (unless otherwise stated).
7. Total Unadjusted Error (TUE) is the sum of integral linearity error, zero code error and full scale error over the output code range.
8. A Differential linearity of "n" bits ensures a code width exists to "n" bits. Hence a Differential Linearity of 8 bits for an 8 bit ADC guarantees no missing codes.
9. For $V_{IN}(-)$ greater than or equal to $V_{IN}(+)$ the digital output code will be 00 Hex. Connected to each analogue input are two diodes which will forward conduct for a diode drop outside the supply rails, V_{CC} and GND. If an analogue input voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To use an absolute input voltage range of 0 to V_{CC} a minimum $V_{CC} - 0.05\text{ V}$ is required for all variations of temperature. Care should be exercised when testing at low V_{CC} levels with a maximum analogue voltage as this can cause the input diode to conduct, especially at high temperature, and cause errors for analogue inputs near full scale.
10. Standby input leakage currents, are currents going in or out of the on or off channels when the ADC is not performing conversion and the clock input is in a high or low steady-state condition.
11. For WM0832 the reference current is included in the supply current as V_{REF} is internally connected to V_{CC} .

Test Circuits and Waveforms

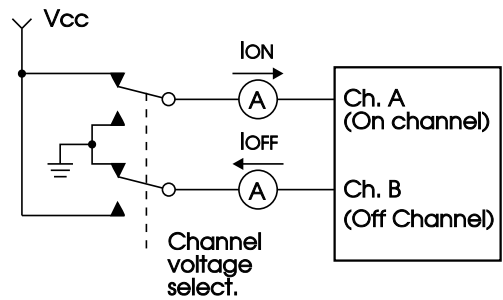
Output Disable Time Voltage Waveforms and Test Circuits



Standby Leakage Current Test Circuit

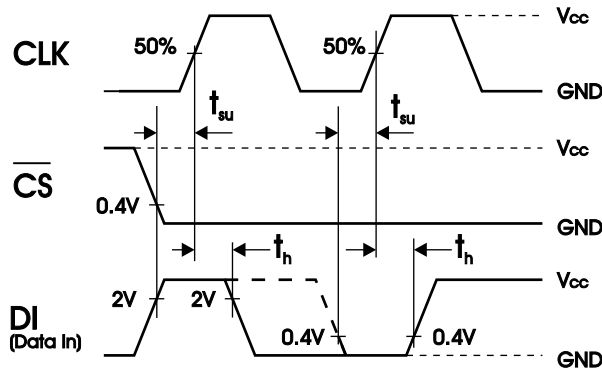


Note A: C_L includes jig and probe capacitance

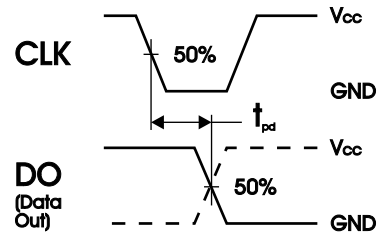


Detailed Timing Diagrams

WM0832 Data Input Timing

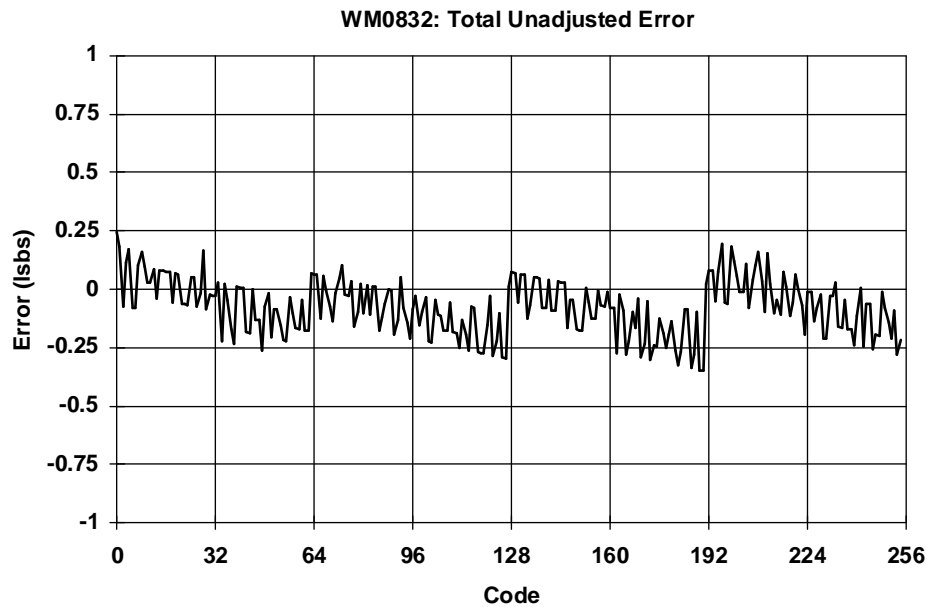
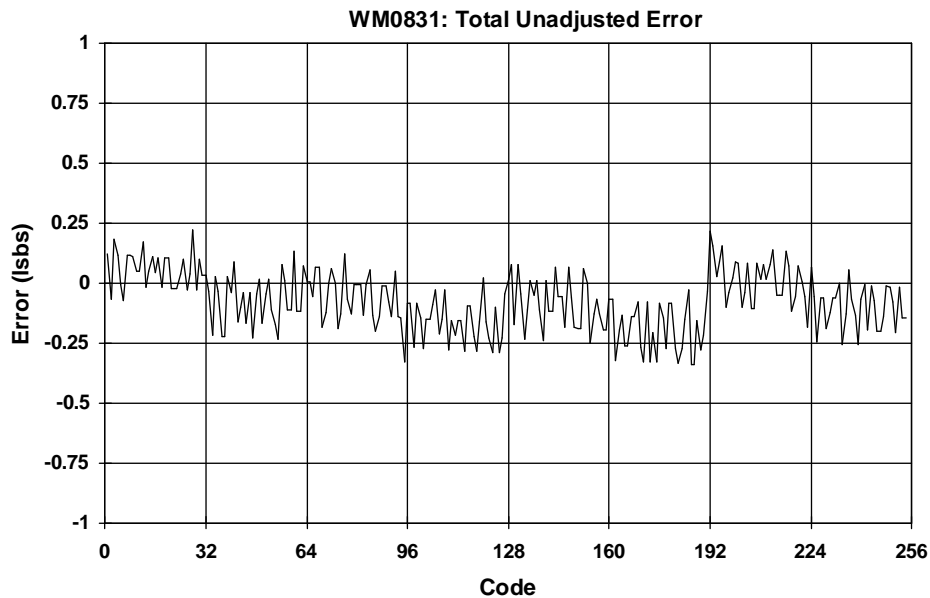


Data Output Timing



WM0831, WM0832

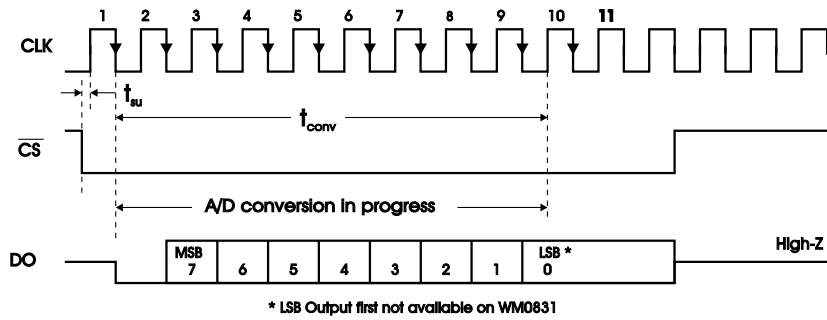
Performance Data (typical)



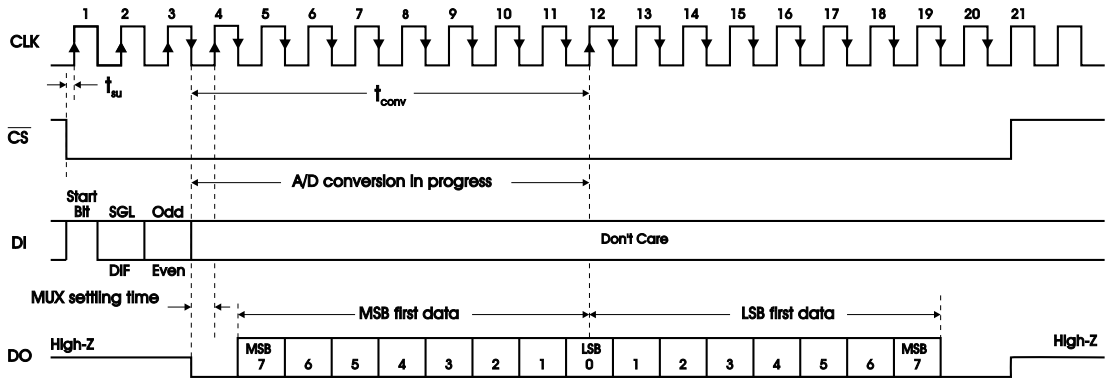
Test conditions: $V_{CC} = 5V$, $V_{REF} = 5V$, Temp = 25°C, $F_{CLK} = 250KHz$

Functional Timing Diagrams

WM0831 Timing



WM0832 Timing



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Pin Descriptions

WM0831			
Pin	Name	Type	Function
1	CS	Digital	Chip Select (active low)
2	IN+	Analogue input	Positive differential input
3	IN-	Analogue input	Negative differential input
4	GND	Supply	Analogue and digital ground
5	VREF	Analogue input	Voltage reference input
6	DO	Digital input	Data Output
7	CLK	Digital input	Clock input
8	VCC	Supply	Positive supply voltage

WM0832			
Pin	Name	Type	Function
1	CS	Digital	Chip Select (active low)
2	CH0	Analogue input	Channel 0 input to multiplexer (MUX)
3	CH1	Analogue input	Channel 1 input to multiplexer (MUX)
4	GND	Supply	Analogue and digital ground
5	DI	Digital input	Data input
6	DO	Digital input	Data Output
7	CLK	Digital input	Clock input
8	VCC/VREF	Supply/Analogue I/P	Positive supply voltage and voltage(ratiometric) reference input

Multiplexer / Package Options			
Device No	Number of Analogue Channels		Number of Package Pins
	Single Ended	Differential	
WM0831	1	1	8
WM0832	2	1	8

Functional Description

Input and Multiplexer Operation and Addressing

WM0831 has two inputs IN+ and IN- configured for differential operation, single ended operation is achieved by grounding IN- to an analogue common or GND. WM0832 uses an input multiplexer scheme with two input channels, configurable for single-ended or differential operation. The single ended input uses the GND pin as its analogue ground reference.

WM0831/2 uses a successive approximation routine to perform A/D conversion and employs a sample data comparator structure which always performs conversion on a differential voltage. Conversion takes place on the voltage difference between assigned "+" and "-" inputs and the converter expects the "+" input to be the most positive, if the "+" input is more negative than "-" then the converter gives an all zeros output. Assignment of WM0832 inputs is made for a single-ended signal between an "+" input and (analogue) ground (GND), or for a differential input between CH0 and CH1 inputs of either polarity.

For WM0832 prior to the start of every conversion the input configuration is assigned during the MUX addressing sequence by serially shifting data into the Data Input (DI) on the second and third rising edges of the clock input. The MUX address selects which analogue inputs are enabled, either single-ended or differential. For differential inputs the polarity of the inputs are also assigned. The MUX addressing table gives full details of input assignments. Because WM0831 has only one differential input of fixed polarity it does not require addressing.

WM0832 MUX Addressing			
MUX Address		Channel Number	
SGL/DIF	ODD/EVEN	0	1
Differential MUX Mode			
0	0	+	-
0	1	-	+
Single Ended MUX Mode			
1	0	+	
1	1		+

Functional Description (continued)**Initiating Conversion and the Digital Interface**

WM0831 and WM0832 are controlled from a processor via a Chip Select (\overline{CS}) input and a serial interface comprising Data Out (DO) and additionally for WM0832 a Data In (DI) input.

For WM0831 conversion is initiated by pulling chip select low and inputting a clock signal. On the clock's first falling edge after \overline{CS} is brought low, DO output comes out of high impedance mode. On the second and subsequent clock falling edges, to a total of nine, the conversion result is output on DO in MSB to LSB order. WM0831 only provides output data in MSB first order.

For WM0832 conversion is also initiated by pulling the chip select (\overline{CS}) line low and inputting a clock signal but MUX addressing information has also to be input on DI. The start bit and the MUX assignment bits on DI are clocked in on the first three rising edges of the clock input which may be generated by the processor or run continuously. WM0832 uses two MUX assignment bits.

When the logic "1" start bit is clocked into the start conversion location of the multiplexer input register the analogue MUX inputs are selected. After 1/2 a clock period delay to allow for the selected MUX output to settle the conversion commences using the successive approximation technique.

When conversion begins the A/D conversion result from the output of the SARS comparator appears at the DO output on each falling edge of the clock (see Functional Timing Diagrams).

With the successive approximation A/D conversion routine the analogue input is compared with the output of a digital to analogue converter (DAC) for each bit by the SARS comparator and a decision made on whether the analogue input is higher or lower than the DAC output. Successive bits, MSB to LSB, are input to the DAC and remain in its input if the analogue comparison decides the analogue input is higher than the DAC output, if not the bit is removed from the DAC input. There is no sample and hold. The input needs to be stable during T_{conv} period (see Functional Timing Diagrams).

The output from the SARS comparator forms the resulting input to the DAC and the A/D conversion output on DO, and is read by the processor as conversion takes place in MSB to LSB order. After 8 clock periods the conversion is complete.

For WM0832 the 8 bits of the conversion are stored in an output shift register, after a conversion has completed and MSB first data has been output WM0832 automatically shifts out LSB first data on the DO output.

\overline{CS} must be held low through an entire conversion, all internal registers are cleared when \overline{CS} is high. To initiate another conversion \overline{CS} must make a high to low transition and for WM0832 MUX address assignments input to DI.

For WM0832 the DI input and DO output can be tied together and controlled via a bidirectional processor I/O bit line.

Reference Input

The analogue input voltage range, V_{max} to V_{min} for differential inputs is defined by the voltage applied to the reference input with respect to GND. WM0832 is fixed in a ratiometric mode with VREF internally tied to V_{cc} , WM0832 has a separate VREF pin and can be used in either ratiometric applications or those requiring absolute accuracy.

A ratiometric reference input, typically the V_{cc} , is the same supply used to power analogue input circuitry and sensors. In such systems under a given input condition the same code will be output with variations in supply voltage because the same ratio change occurs in both the analogue and reference input to the A/D. When used in applications requiring absolute accuracy a suitable time and temperature stable voltage reference source should be used.

The voltage source used to drive the reference input should be capable of driving the 2.4 k Ω typical of the SAR resistor ladder. The maximum input voltage to the reference input is the V_{cc} supply voltage. The minimum for WM0832 can be at least as low as 1 V to allow for direct conversion of sensor outputs with output voltage ranges less than 5 V.

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Functional Description (continued)

Analogue Inputs.

While sampling the analogue inputs short spikes of current enter a "+" input and flow out of the corresponding "-" input at the clock edges during conversion. This current does not cause errors as it decays rapidly and the internal comparator is strobed at the end of a clock period. Care should be exercised if bypass capacitors are used at the inputs, as an apparent offset error can be caused by the capacitor averaging the input current and developing a voltage across the source resistance. Bypass capacitors should not be used with a source resistance greater than 1kΩ.

In considering error sources, input leakage current will also cause a voltage drop across the source resistance and hence high impedance sources should be buffered.

In differential mode there is a 1/2 clock period interval between sampling the "+" and the "-" inputs. If there is a change in common mode voltage during this interval an error could notionally result.

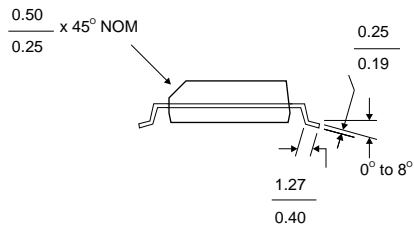
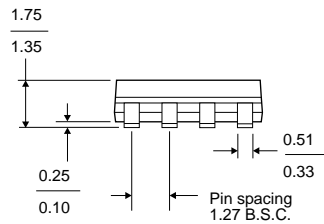
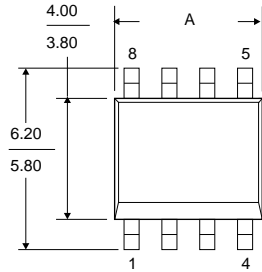
For a sinusoidal common mode signal the error is given by: $V_{ERROR} = V_{PEAK} (2\pi f_{CM}) (1/(2f_{CLK}))$

Where V_{PEAK} = Peak common mode voltage
 f_{CM} = Common mode signal frequency
 f_{CLK} = Clock frequency.

Package Descriptions

Plastic Small-Outline Package

D - 8 pins shown



Dimension 'A' Variations

N	Min	Max
8	4.80	5.00
14	8.55	8.75
16	9.80	10.00

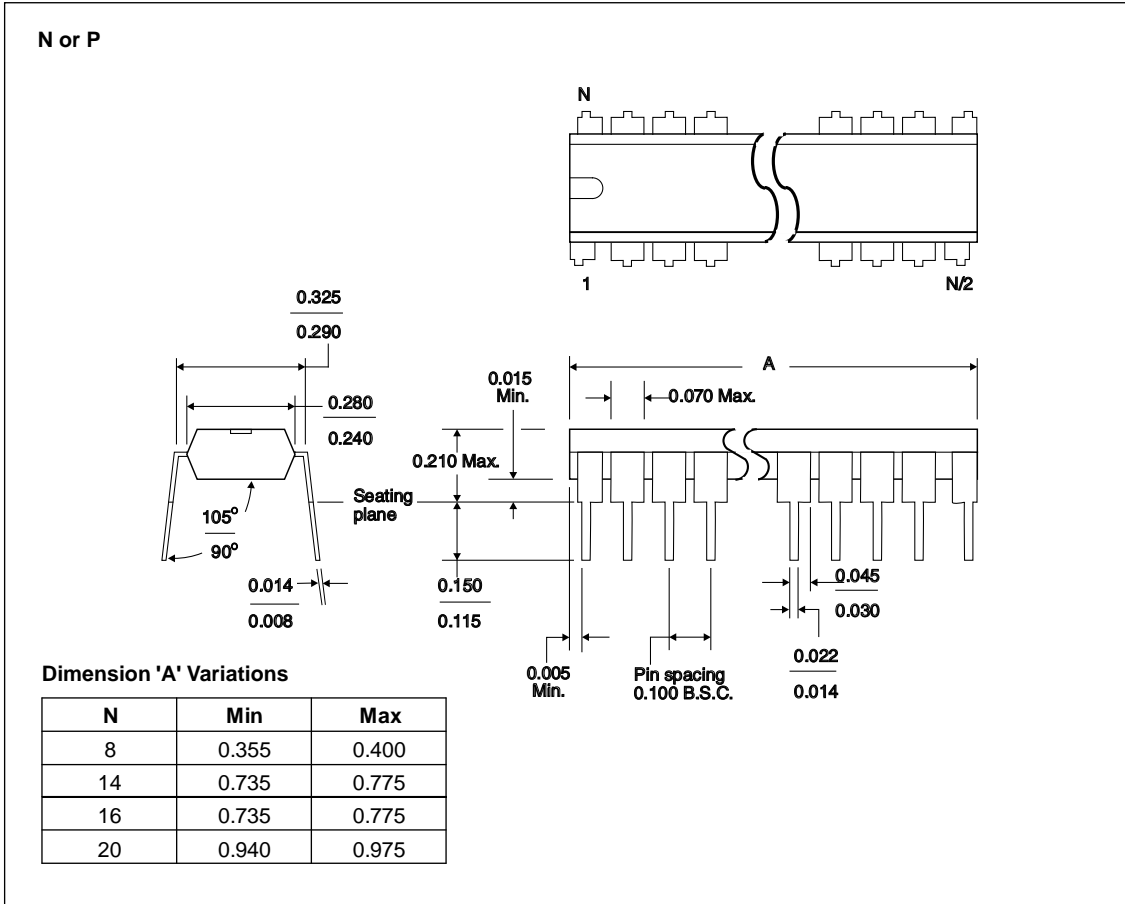
Notes:

- A. Dimensions in millimeters.
- B. Complies with Jedec standard MS-012.
- C. This drawing is subject to change without notice.
- D. Body dimensions do not include mold flash or protrusion.
- E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

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Package Descriptions

Dual-In-Line Package



Notes:

- A. Dimensions are in inches
- B. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001)
- C. N is the maximum number of terminals
- D. All end pins are partial width pins as shown, except the 14 pin package which is full width.

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