1340-Type Lightwave Receiver

Operating at 1.1 µm through 1.6 µm wavelengths and at 155 Mbits/s, 622 Mbits/s, or 1.25 Gbits/s, the versatile 1340-Type Receiver is manufactured in a 20-pin, plastic DIP with a multimode fiber pigtail.

Features

- Backward compatible with 1310 receiver family
- Space-saving, self-contained, 20-pin plastic DIP
- Silicon-based ICs
- Single 5 V power supply operation including photocurrent monitor capability
- Exceeds all SONET (GR-253-CORE) and ITU-T G.958 jitter requirements
- Wide dynamic range
- Qualified to meet the intent of *Telcordia Technologies** reliability practices
- Operates at data rates of 155 Mbits/s, 622 Mbits/s, or 1.25 Gbits/s
- Positive ECL (PECL) data outputs
- CMOS (TTL) link-status flag output
- Operation at 1.3 µm or 1.55 µm wavelengths
- Operating case temperature range of –40 °C to +85 °C

Applications

- Telecommunications:
  - — Inter- and intraoffice SONET/ITU-T SDH
  - — Subscriber loop
  - — Metropolitan area networks
- High-speed data communications

Description

The 1340-Type receiver is designed for use in transmission systems or medium- to high-speed data communications applications at data rates up to 1.25 Gbits/s. Compact packaging, along with wide dynamic range, makes these receivers ideal for both telecommunications and data communications applications.

The following three versions of the receiver are available:

- SONET/SDH compliant with OC-3/STM-1
- SONET/SDH compliant with OC-12/STM-4
- 1.25 Gbits for data applications.

* *Telcordia Technologies* is a trademark of Telcordia Technologies, Inc.

Description (continued)

The SONET/SDH versions of the receiver are fully compliant with the latest issue of *Telcordia Technologies* GR-253- CORE and the most recent issues of ITU recommendations G.957 and G.958. The 1340-Type receiver requires only a single 5 V power supply for operation. All versions of the receiver are characterized for operation over the case operating range of –40 °C to +85 °C at the appropriate data rate for each version.

Manufactured in a 20-pin DIP, the receivers use a planar, rear illuminated InGaAs PIN photodetector that allows these receivers to be used at wavelengths from 1.1 µm to 1.6 µm. The photocurrent output of the PIN detector is amplified and converted to a voltage by a silicon amplifier. A silicon quantizer provides additional signal amplification, data threshold detection, and PECL data outputs. The incoming optical signal is coupled into the receiver through a 62.5 µm core multimode fiber pigtail. The outer jacket diameter of the pigtail is 900 µm. The receiver can be ordered with the pigtail terminated in an FC/PC, SC, or *ST* ® optical connector. Other connectors are available on special order. See your Agere account representative for ordering conditions and information.

The receiver has differential PECL data outputs and, depending on the version selected, either differential PECL link status flag or complementary CMOS link status flag outputs. The link status flag outputs indicate the presence or absence of a minimum acceptable level of optical input signal.

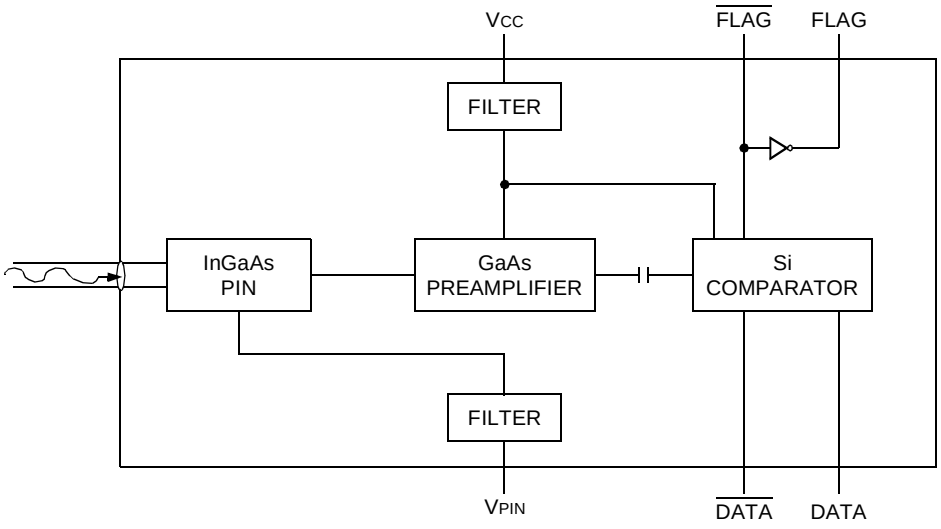

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Figure 1. Block Diagram

Description (continued)

To help ensure high product reliability and customer satisfaction, Agere is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing and shipping process. Optoelectronics subsystems are qualified to Agere internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with *Telcordia Technologies* requirements. The 1340 receiver qualification program meets the intent of *Telcordia Technologies* TR-NWT-000468 andTA-TSY-000983.

Application Information

The 1340 receiver is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (PECL), the device should be thought of as an analog component. When laying out the printed-wiring board (PWB), the 1340 receiver should be given the same type of consideration one would give to a sensitive analog component.

At a minimum, a double-sided printed-wiring board with a large component-side ground plane beneath the receiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground connections on separate layers, which helps minimize the coupling of unwanted signal noise into the power supplies of the receiver.

Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth transimpedance amplifier. The amplifier detects and amplifies signals that are only tens of nA in amplitude. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's loss of signal (FLAG) circuit.

To minimize the coupling of unwanted noise into the receiver, route high-level, high-speed signals such as transmitter inputs and clock lines as far away as possible from the receiver pins. If this is not possible, then the PWB layout engineer should consider interleaving the receiver signal and flag traces with ground traces in order to provide the required isolation.

Noise that couples into the receiver through the power supply pins can also degrade device performance. The application schematics, Figures 3—5, show recommended power supply filtering that helps minimize noise coupling into the receiver. The bypass capacitors should be high-quality ceramic devices rated for RF applications. They should be surface-mount components placed as close as possible to the receiver power supply pins. The ferrite bead should have as high an impedance as possible in the frequency range that is most likely to cause problems. This will vary for each application and is dependent on the signaling frequencies present on the application circuit card. Surface-mount, high-impedance beads are available from several manufacturers.

Data and Flag Outputs

The data outputs of the 1340 receiver are driven by open-emitter NPN transistors which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum output current. Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (DATA and $\overline{\text{DATA}}$) should be terminated identically. The signal lines connecting the data outputs to the next device should be equal in length and should have matched impedances.

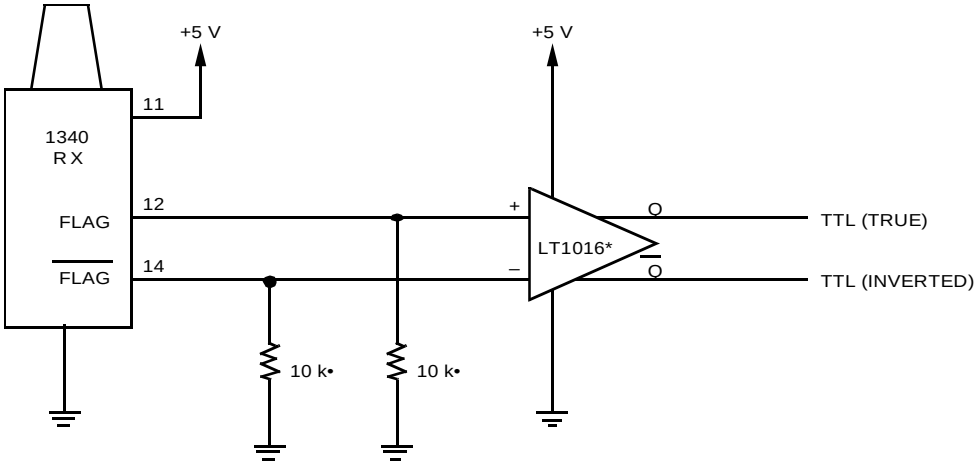
Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and may cause transitions to occur where none were intended. Also, by minimizing high frequency ringing due to reflections caused by improperly designed and terminated signal lines, possible EMI problems can be avoided. The applications sections in the Signetics* *ECL 10K/100K* Data Manual or the National Semiconductor† *ECL Logic Databook and Design Guide* provide excellent design information on ECL interfacing.

* *Signetics* is a registered trademark of Signetics Corp.
† *National Semiconductor* is a registered trademark of National Semiconductor Corporation.

Data and Flag Outputs (continued)

The FLAG and $\overline{\text{FLAG}}$ outputs of the OC-3/STM-1 155 Mbits/s version of the 1340 receiver are PECL logic levels driven by open emitter transistors with the same characteristics as the data outputs. These outputs must be properly terminated in order to obtain the correct logic levels. Since the FLAG function is basically a dc switch that indicates the loss of optical input signal, it can be interfaced to much slower TTL or CMOS logic circuits.

The circuit shown in Figure 2 provides one example of how to create a TTL logic output from the PECL FLAG output signal. The outputs of the LT1016 are TTL-compatible and provide both true and inverted logic levels. The Q output of this circuit will be a TTL high (>2.5 V) when the 1340 is receiving an optical signal greater than the FLAG switching threshold and will be a TTL low (<0.4 V) whenever the optical signal is absent or is below the FLAG switching threshold. The FLAG and $\overline{\text{FLAG}}$ outputs of the OC-12/STM-4 and 1.25 Gbits/s receivers are 5 V TTL logic level compatible. The FLAG output is provided directly by the comparator IC. However, the FLAG output is derived from the $\overline{\text{FLAG}}$ output through an inverter. Excessive loading of the $\overline{\text{FLAG}}$ output can cause the FLAG output to malfunction.



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* Part available from Linear Technology Corporation of Milpitas, CA 95035.

Figure 2. Converting PECL FLAG Outputs to TTL

Pin 10

Pin 10 on the 1340-Type receiver is a not internally connected (NIC) pin. This definition allows the 1340 to be used in most customer 20-pin receiver module applications. Customer's printed-wiring boards that are designed with ground, +5V, –5V, or no connection to this pin are all acceptable options. For those applications that require monitoring the photocurrent of the PIN photodetector for power monitoring purposes, there are versions of the 1340 that require +5 V or –5 V applied to Pin 10. CheckTables 4 and 5 for ordering information.

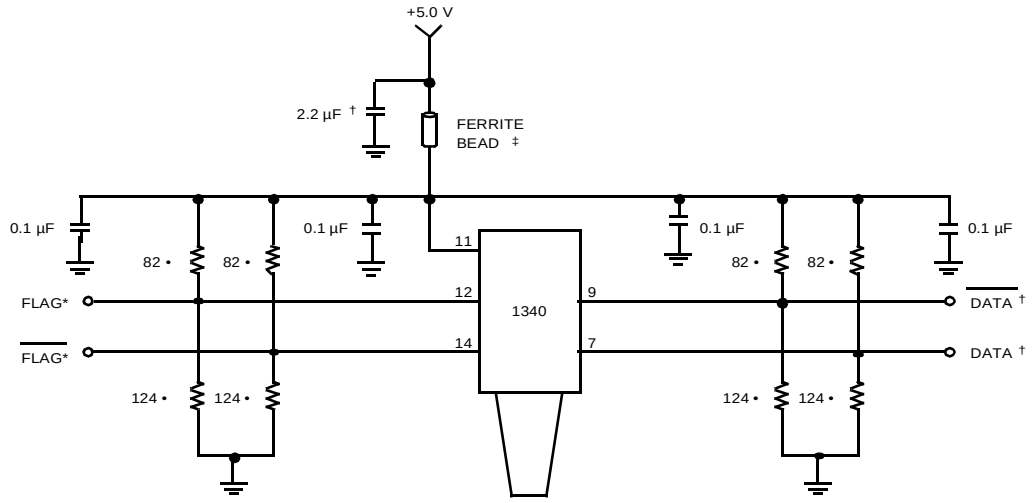
Recommended User Interface

The 1340 receiver is designed to be operated from a 5 V power supply and provides raised or pseudo-ECL (PECL) data outputs. Figures 3 and 4 show two possible application circuits for the 1340 receiver. Figure 3 represents an application for the version with PECL FLAG outputs while Figure 4 shows a possible application for the version with the TTL-compatible FLAG outputs.

In both instances, the DATA outputs are terminated with a Thévenin equivalent circuit, which provides the equivalent of a 50 Ω load terminated to (V_{CC} – 2 V).

A single 50 Ω resistor terminated to (V_{CC} – 2 V) could also be used, but this requires a second power supply. Other methods of terminating ECL-type outputs are discussed in the references previously mentioned.

Figure 5 shows an example of a circuit that can be used to interface the PECL outputs of the 1340 receiver with a device which requires true, negative voltage ECL inputs. The 100314 is an ECL line receiver and is shown here only as an example to demonstrate this coupling procedure. The DATA lines are terminated in a 50 Ω equivalent impedance but are ac-coupled to the 100314. The capacitive coupling isolates and permits level shifting of the positive DATA outputs of the receiver to the proper negative level required by the inputs of the 100314. The V_{BB} output of the 100314 provides the reference voltage required to center the voltage swing of the DATA signals around the input switching threshold of the 100314. The Thévenin equivalent of the 166 Ω and 250 Ω resistor pair is 100 Ω, which, in parallel with the 100 Ω resistor connected to V_{BB}, results in a 50 Ω equivalent impedance for the load on each of the data lines. Alternatively, if there is no V_{BB} reference available, a second pair of 166 Ω/250 Ω resistor networks could be used on the data lines on the 100314 side of the coupling capacitor.

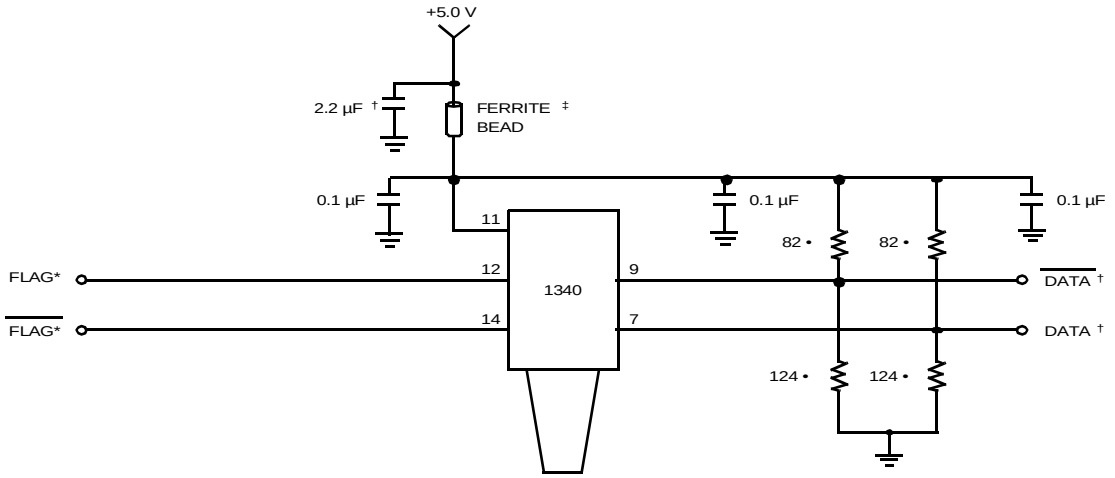


* 50 Ω to (V_{CC} – 2)V.
† DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines; both lines can be ac- or dc-coupled into the next device.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.

Note: All unused outputs must be terminated as shown. All resistors are 1/8 W, thin-film, ceramic chips. All capacitors are 25 Vdc, ceramic X7R, or equivalent.

Figure 3. Interfacing to the 155 Mbits/s 1340 Receiver

Recommended User Interfaces (continued)



* TTL (CMOS) compatible level.
† DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines; both lines can be ac- or dc-coupled into the next device.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.

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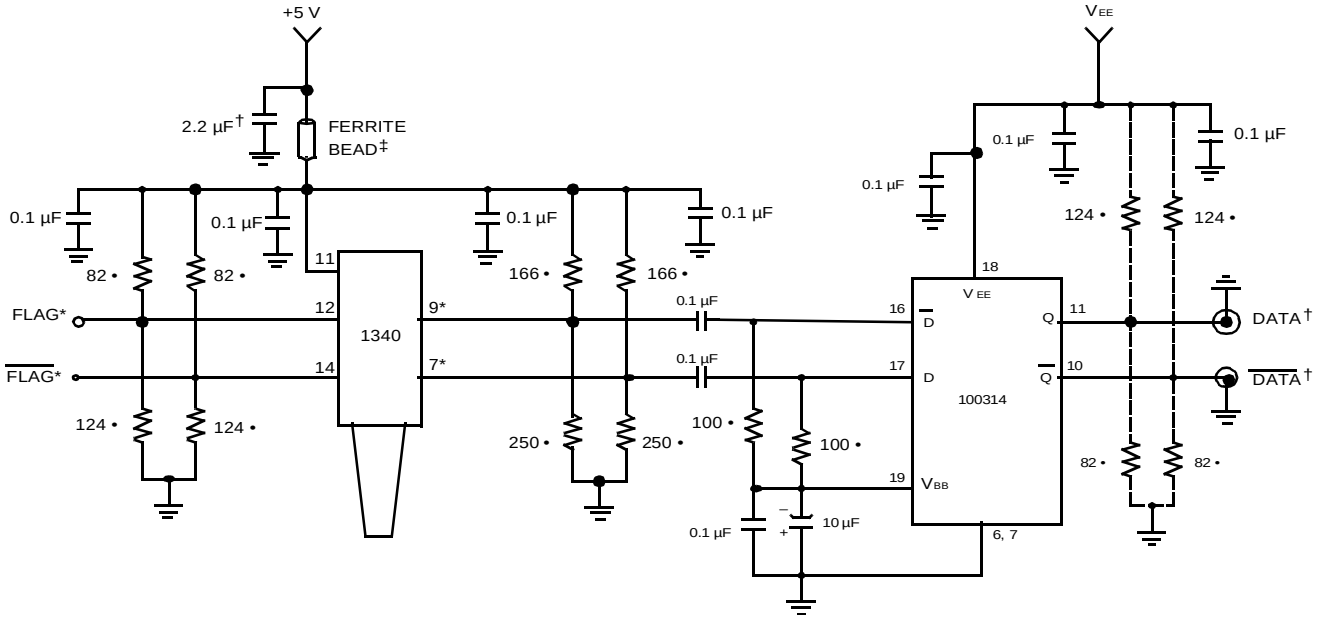
Figure 4. Interfacing to the 622 Mbits/s and 1.25 Gbits/s 1340 Receivers



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* 50 Ω to (V_{CC} – 2) V.
† 50 Ω to –2 V. DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.

Figure 5. Interfacing the 155 Mbits/s 1340 Receiver to a True ECL Circuit

Pin Information

Table 1. Pin Descriptions

Pin Number	Description
1	Ground
2	Ground
3	Ground
4	Ground
5	No User Connection*
6	Ground
7	DATA
8	Ground
9	$\overline{\text{DATA}}$
10	NIC or Optional V_{PIN}
11	Vcc (5 V)
12	FLAG†
13	Ground
14	$\overline{\text{FLAG}}$
15	Ground
16	Ground
17	No User Connection*
18	No User Connection*
19	No User Connection*
20	No User Connection*

* Pins designated as no user connection are not connected internally within the receiver. However, to allow for future functional upgrades, it is recommended that the user not make any connections to these pin positions.

† The link-status flag is a logic output that indicates the presence or absence of a minimum acceptable level of optical input. A logic high on FLAG indicates the presence of a valid optical signal.

Handling Precautions

Mounting and Connections

The pigtail consists of a 39 in. ± 4 in. (1 m ± 10 cm), 62.5 µm core/125 µm cladding multimode fiber. The standard fiber has a 0.036 in. (914 µm) diameter tight-buffered outer jacket. The minimum fiber bending radius during operation is 1.0 in. (25.4 mm).

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow *EIA Standard *EIA*-625.**

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Agere employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1340 receiver is ±1000 V.

Receiver Processing

The 1340-type receiver devices can withstand normal wave-soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in or sprayed with any cleaning solution or solvents. The process cap and fiber pigtail jacket deformation temperature is 85 °C. The receiver pins can be wave-soldered at maximum temperature of 250 °C for 10 seconds.

Installation Considerations

Although the receiver features a robust design, care should be used during handling. The optical connector should be kept free from dust, and the process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present on the optical connector, the use of canned air with an extension tube should remove any debris. Other cleaning procedures are identified in the technical note, *Cleaning Fiber-Optic Assemblies* (TN95-010LWP).

* *EIA* is a registered trademark of Electronic Industries Association.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations section of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	—	5.5	V
Operating Case Temperature Range	T_C	–40	85	°C
Storage Case Temperature Range	T_{stg}	–40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	µm
Minimum Fiber Bend Radius	—	1.0 (25.4)	—	in. (mm)

Operating Characteristics

Minimum and maximum values specified over operating case temperature range and end-of-life (EOL).
Typical values are measured at beginning-of-life (BOL) room temperature unless otherwise noted.

Table 2. Optical Characteristics

Parameter	Symbol	Data Rate (Mbits/s)	Min	Typ*	Max	Unit
Measured Average Sensitivity*	P_R	155	—	–38	–36	dBm
		622	—	–32	–29	dBm
		1250	—	–28	–24	dBm
Maximum Input Power*	P_{MAX}	155	–3.0	0	—	dBm
		622	–6.0	–3.0	—	dBm
		1250	–3.0	–2.0	—	dBm
Link Status Switching Threshold:						
Decreasing Light Input	LST_D	155	–53.0	–40	–36.0	dBm
		622	–45.0	–34	–28.0	dBm
		1250	–36.0	–31.0	–26.0	dBm
Increasing Light Input	LST_I	155	–52.5	–38	–35.5	dBm
		622	–45.5	–31	–27.5	dBm
		1250	–35.5	–29.0	–25.5	dBm
Hysteresis	HYS	All Data Rates	0.5	3.0	6.0	dBm
Detector Responsivity	R	All Data Rates	0.7	0.8	1.2	A/W

* For 1 x 10^{-10} BER with an optical input using a $2^{23} – 1$ pseudorandom word having a 50% average duty cycle.

Operating Characteristics (continued)

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
dc Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
PIN Photodetector Supply Voltage (Pin 10)*	V_{PIN} V_{PIN}	4.75 –5.25	5.0 –5.0	5.25 –4.75	V V
Power Supply Current	I_{CC} I_{PIN}	— —	80 —	150 1	mA mA
Output Data Voltage:† Low High	 V_{OL} V_{OH}	 V_{CC} – 1.81 V_{CC} –1.025	 V_{CC} – 1.70 V_{CC} – 0.95	 V_{CC} – 1.62 V_{CC} – 0.88	 V V
Output Rise Time/Fall Time: OC-3/STM-1 Versions OC-12/STM-4 Versions	 t_R/t_F t_R/t_F	 — —	 700 350	 1400 400	 ps ps
Output Flag Voltage: OC-3/STM-1 Versions:‡ Low High OC-12/STM-4 Versions:‡ Low High	 V_{FL} V_{FH} V_{FL} V_{FH}	 — V_{CC} – 1.025 0 V_{CC} – 0.5	 V_{CC} – 1.90 V_{CC} – 1.0 — —	 V_{CC} – 1.65 — 0.5 V_{CC}	 V V V V
Output Data Current:† Low High	 I_{OL} I_{OH}	 — —	 5 20	 50 50	 mA mA
Output Flag Current: OC-3/STM-1 Versions: Low High OC-12/STM-4 Versions: Low High	 I_{OL} I_{OH} I_{OL} I_{OH}	 — — 0 0	 5 20 10 10	 50 50 15 15	 mA mA mA mA

* Customers have the option for either a +5 V or –5 V supply.
† Measured from V_{CC} with a 50 Ω load to (V_{CC} – 2) V.
‡ Internally terminated CMOS output.

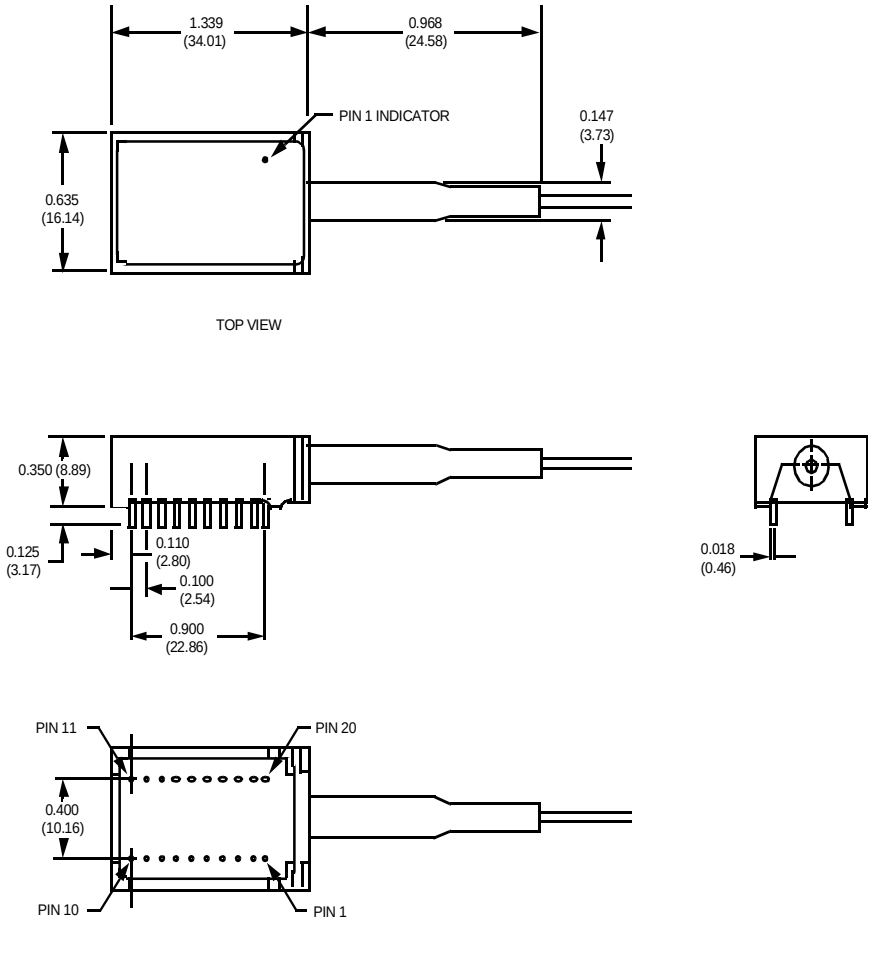
Qualification Tests and Reliability

To help ensure high product reliability and customer satisfaction, Agere is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to Agere internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* requirements. The 1340-Type receivers have undergone an extensive and rigorous set of qualification tests. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 and TA-NWT-000983. In addition, the design, development, and manufacturing facility of Agere's Optoelectronics unit has been certified to be in full compliance with the latest *ISO**-9001 Quality System Standards.

* *ISO* is a registered trademark of The International Organization for Standardization.

Outline Diagram

Dimensions are in inches and (millimeters). Unless noted otherwise, tolerances are 0.005 in. (0.127 mm).



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Ordering Information

Table 4. OC-3/STM-1 Receiver Versions

Device Code	Connector	Pin 10 Requirements	Comcode
1340FMPC	FC-PC	No Internal Connection	108162322
1340CMPC	SC		108354408
1340TMPC	*ST*		108572264
1340FAPC	FC-PC	Requires +5 V or –5 V (Used for photocurrent monitoring)	108468687
1340CAPC	SC		108359175
1340TAPC	*ST*		108572249

Table 5. OC-12/STM-4 Receiver Versions

Device Code	Connector	Pin 10 Requirements	Comcode
1340FNPC	FC-PC	No Internal Connection	108155680
1340CNPC	SC		108354416
1340TNPC	*ST*		108155755
1340FBPC	FC-PC	Requires +5 V or –5 V (Used for photocurrent monitoring)	108155672
1340CBPC	SC		108468679
1340TBPC	*ST*		108572256

Table 6. 1.25 Gbits/s Receiver Versions

Device Code	Connector	Pin 10 Requirements	Comcode
1340FCPC	FC-PC	Requires +5 V or –5 V	108400342
1340CCPC	SC		108400334

Table 7. Related Products

Description	Document Number
1241/1243/1245-Type Receivers for SONET/SDH Applications	DS99-073LWP
1345-Type Receiver with Clock Recovery and Data Retiming	DS00-099OPTO

For additional information, contact your Agere Systems Account Manager or the following:
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JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)
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