MS8512RKX/XA

512K x 8 CMOS SRAM Module

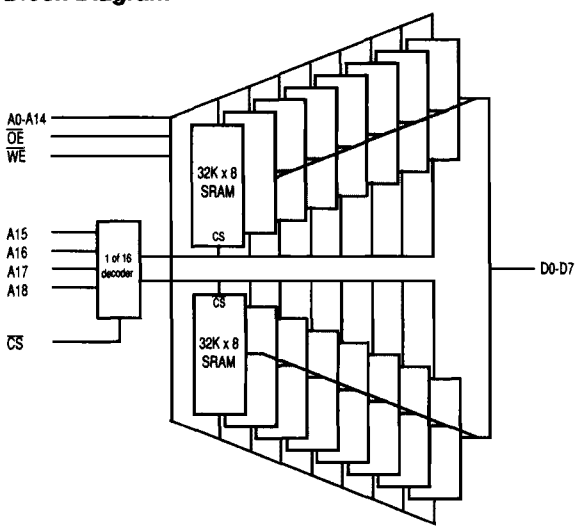
524,288 x 8 CMOS High Speed Static RAM

ADVANCE PRODUCT INFORMATION

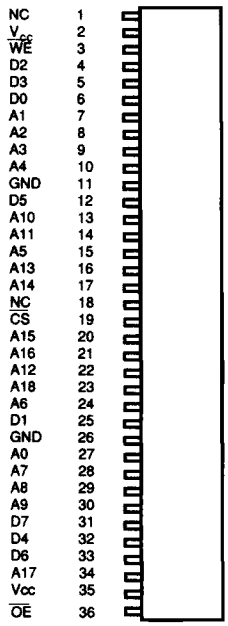
Features

- Fast Access Times of 100/120/150 ns
- Low Power Standby 32mW (typ.)
  175µW (typ.) - L Version
- Low Power Operation 80mW at 1MHz (typ.)
- Completely Static Operation
- Equal Access and Cycle Times
- Battery Back-up Capability
- Directly TTL Compatible
- Common Data Inputs & Outputs
- Onboard Decoupling Capacitors

Block Diagram



Pin Definition



Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{CC}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Leadframe
36	800 mil Single-in-Line (SIP)-X Version	Straight
36	800 mil Single-in-Line (SIP)-XA Version	90°

Package details and dimensions on page 4-13.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_t	-0.5V to +7	V
Power Dissipation	P_t	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

Note: V_t can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (8512RKXAI)

Capacitance (V_{CC}=5V±10%,T_a=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance ($CS:A_{15}$-A_{18})	C_{ICS}	V_{IN}=0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	128	pF

Note: Capacitance calculated, not measured.

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=Gnd to V_{CC}	-	-	32.0	µA
I/O Leakage Current	I_{LIO}	$\overline{CS}$=V_{IH},V_{OUT}=Gnd to V_{CC}	-	-	2.0	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL},I_{OUT}=0mA	-	16.0	60.0	mA
Average Power Supply Current	I_{CC1}	Min. Cycle,duty=100%,	-	95.0	115.0	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	-	8.0	48.0	mA
	I_{SB1}	$\overline{CS}$>=V_{CC}-0.2V	-	6.4	32.0	mA
Standby Current (L Part)	I_{SB2}	As I_{SB1}	-	35.0	1620.0	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Note 1: Typical values are at V_{CC}=5.0V,T_a=25°C and specified loading.

AC Test Conditions

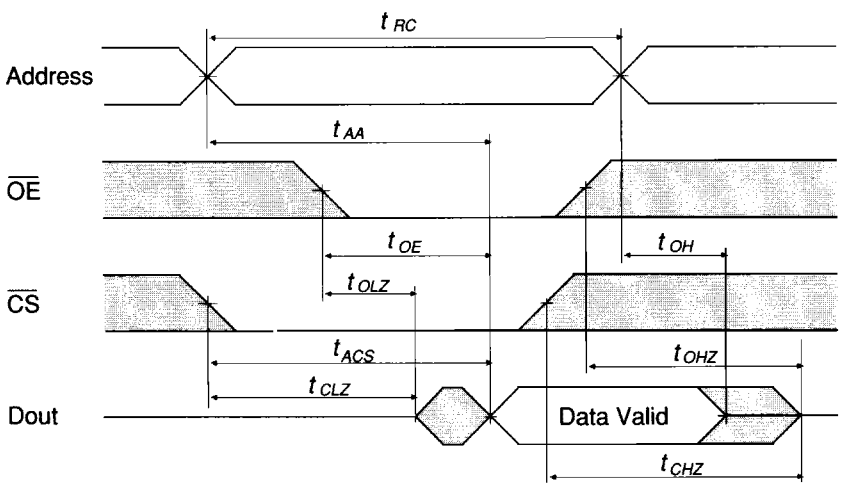
* Input pulse levels: Gnd to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

Read Cycle Timing Waveform (1,2)



Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

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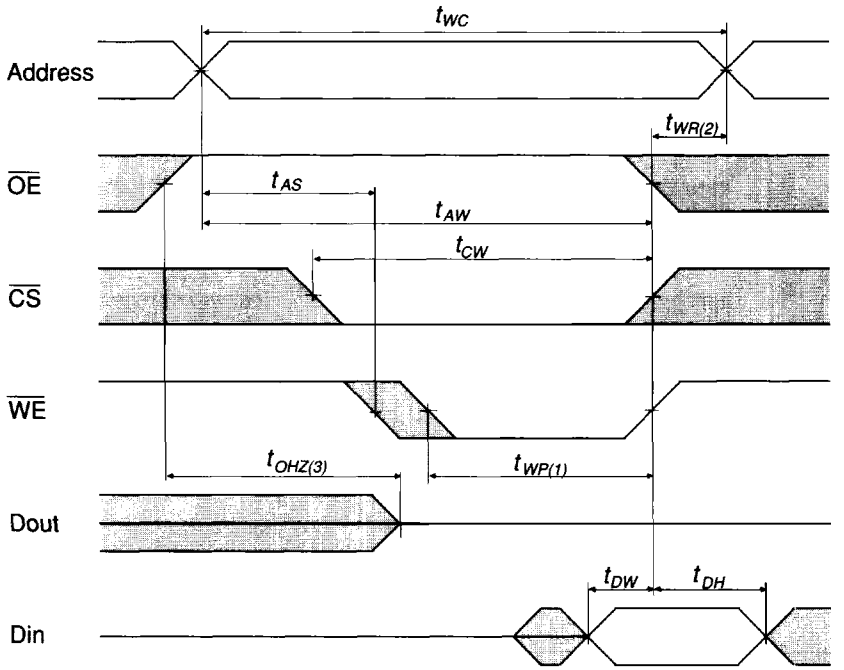
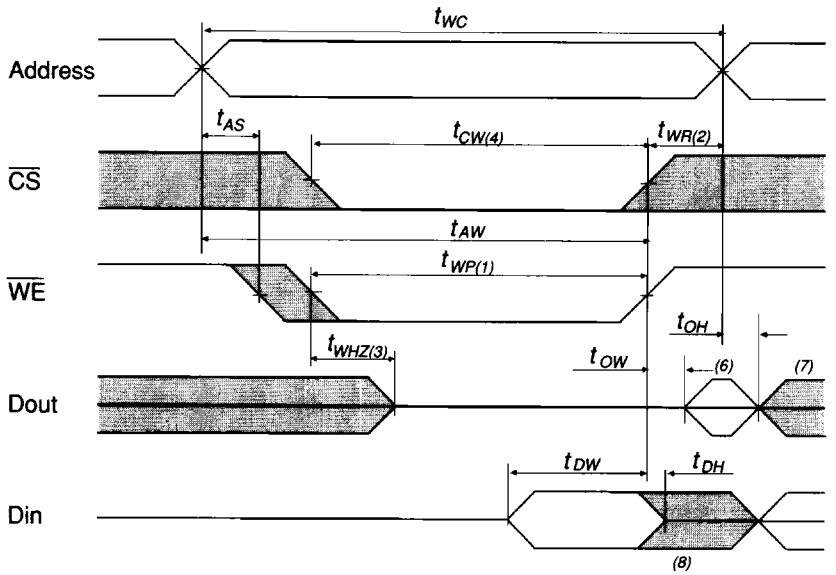
Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	70	-	80	-	90	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



Notes:

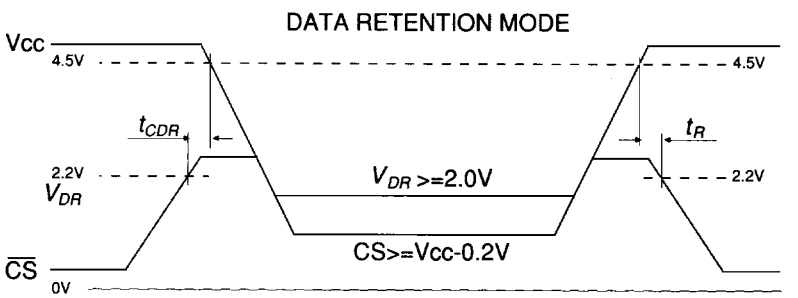
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}=V_{IL}$)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

Low V_{cc} Data Retention Characteristics - L Version Only (T_a=0 to +70°C)

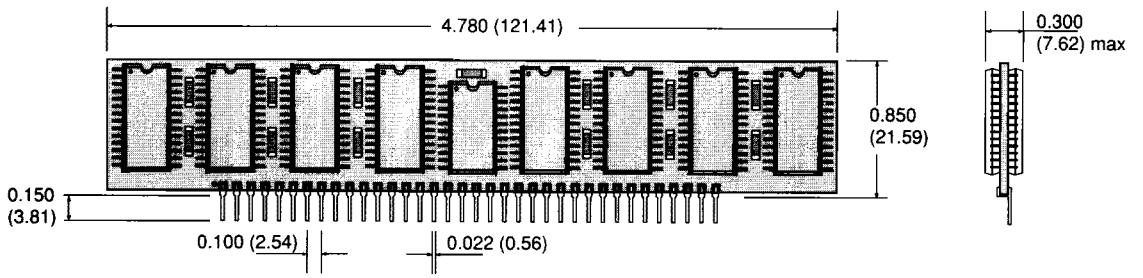
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Vcc for Data Retention	V_{DR}	$\overline{CS}$>=V_{cc}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	Vcc=3.0V,$\overline{CS}$>=2.8V I/P's<=0.2V or >=2.8V	-	-	880*	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}**	-	-	ns

* V_{il} min. = 0.3V, 340µA max at T_a=0-40°C
** t_{RC}=Read Cycle Time

Data Retention Timing Waveform

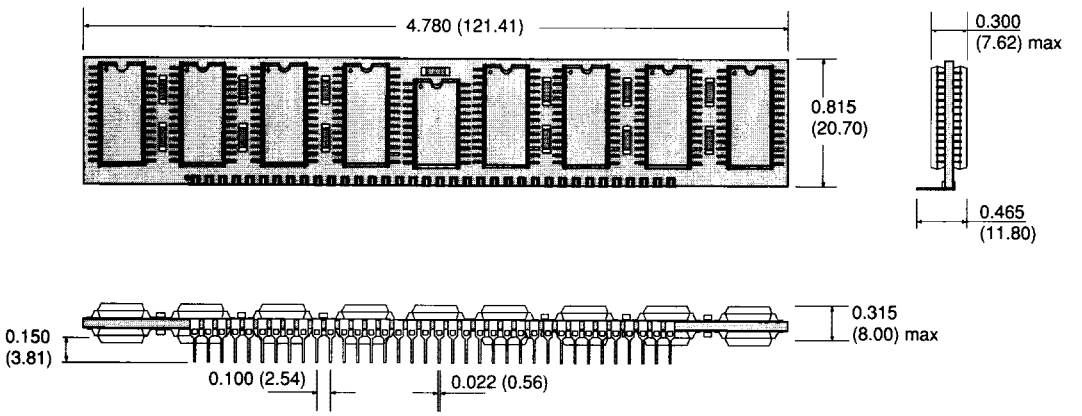


36 Pin Straight Leadframe SIP (X Version)



Dimensions in inches (mm).
Tolerance on all dimensions ±0.010 (0.254)

36 Pin 90°Leadframe SIP (XA Version)



Dimensions in inches (mm).
Tolerance on all dimensions ±0.010 (0.254)

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Ordering Information

MS8512RKXLI-10

Speed	100,120,150 ns	
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Pinout	X	= ASIC-Straight Leadframe
	XA	= ASIC-90°Leadframe
Package	RK	= 36 Pin SIP