

K1525C Series

14 pin DIP, 5.0 Volt, CMOS/TTL, VCXO

**THIS PRODUCT IS NOT RECOMMENDED FOR NEW DESIGNS.
PLEASE REFER TO THE MV PRODUCT SERIES.**



- Former **Champion Technologies, Inc.** Product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Division/Division

OBSOLETE

Ordering Information

00.0000 MHz

K1525C X X X -R

Product Series _____

Model Selection _____

A: ±100 - ±150 ppm Pull

D: ±80 - ±120 ppm Pull

Temperature Range _____

Blank: 0°C to +70°C

M: _____

Symmetry (Duty Cycle) _____

Blank: HCMOS 40%/60%

C: _____ /55%

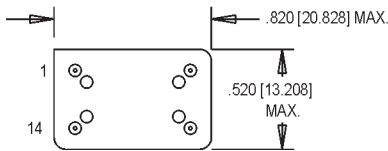
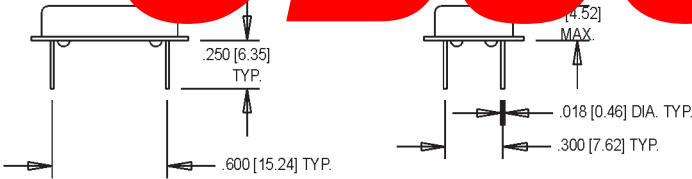
T: _____ L 45%/55%

S _____

Blank: _____

-R: RoHS compliant part

Frequency (customer specified) _____



All dimensions in inches [mm].

Pin Connections

| PIN | FUNCTION |
|-----|--------------------|
| 1 | Voltage Control |
| 7 | Ground/Case Ground |
| 8 | Output |
| 14 | +Vdd |

| PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes |
|--------------------------------|--------------------------------|---|-------|--------|---------|----------------------------|
| Frequency Range | F | 2 | | 55 | MHz | |
| Operating Temperature | T _A | (See Ordering Information) | | | | |
| Storage Temperature | T _s | -40 | | +125 | °C | |
| Frequency Stability Overall | ΔF/F | Inclusive of Calibration, Temperature, Voltage, Load, and Aging | | | | |
| 0°C to +70°C | | | | ±25 | ppm | |
| -40°C to +85°C | | | | ±50 | ppm | |
| Aging 1st Year | | -3 | | +3 | ppm | |
| Thereafter (per year) | | -1 | | +1 | ppm | |
| Pullability/APR | | (See Ordering Information) | | | | |
| Control Voltage | V _c | 0.5 | 2.5 | 4.5 | V | |
| Linearity | | | | 10 | % | Positive Monotonic Slope |
| Modulation Bandwidth | f _m | 20 | | | kHz | ±3dB |
| Input Impedance | Z _{in} | 50k | | | Ohms | @ 10 kHz |
| Input Voltage | V _{dd} | 4.5 | 5.0 | 5.5 | V | |
| Input Current | I _{dd} | | | 26 | mA | |
| Output Type | | | | | | HCMOS/TTL |
| Load | | 5 TTL or 15 pF HCMOS | | | | See Note 1 |
| Symmetry (Duty Cycle) | | (See Ordering Information) | | | | See Note 2 |
| Logic "1" Level | V _{oh} | 4.5 | | | V | |
| Logic "0" Level | V _{ol} | | | 0.5 | V | |
| Output Current | | | | ±16 | mA | |
| Rise/Fall Time | T _r /T _f | | | 4 | ns | |
| Start up Time | | | | 10 | ms | |
| Phase Jitter@ 26 MHz | φ _J | | 4 | | ps RMS | Integrated 12 kHz - 20 MHz |
| Phase Noise (Typical) @ 26 MHz | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz | Offset from carrier |
| | -65 | -95 | -120 | -130 | -140 | dBc/Hz |

- TTL load - see load circuit diagram #1. HCMOS load - see load circuit diagram #2.2
- Maximum Wave Soldering Conditions: +260 °C for 10 secs.

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